DLPC410 DLP Digital Controller

1 Features

- Operates the Following DLP® Chipset Components:
  - DMD: DLP7000 / DLP7000UV and DLP9500 / DLP9500UV
  - DMD Micromirror Driver: DLPA200
  - PROM: DLPR410
- Enables Highest Speed DMD Pattern Rates
  - 1-Bit Binary Pattern Rates up to 32 kHz
  - 8-Bit Monochrome Pattern Rates up to 1.9 kHz
- Allows Input Clock Rates Between 200 MHz and 400 MHz
- Provides up to a 64-Bit LVDS Data Bus Interface
- Supports Random DMD Row Addressing
- Compatible With a Variety of User Defined Processors or FPGAs
- 676-Pin, 27-mm × 27-mm PBGA Package

2 Applications

- Industrial:
  - Direct Imaging Lithography
  - Laser Marking and Repair Systems
  - Computer-to-Plate Printers
  - Rapid Prototyping Machines and 3D Printers
  - 3D Scanners for Machine Vision and Quality Control
- Medical:
  - Phototherapy Devices
  - Ophthalmology
  - Vascular Imaging
  - Hyperspectral Imaging
  - 3D Scanners for Limb and Skin Measurement
  - Confocal Microscopes
- Display:
  - 3D Imaging Microscopes
  - Intelligent and Adaptive Lighting
  - Augmented Reality and Information Overlay

3 Description

The DLPC410 offers the highest speed pattern rates in the DLP Advanced Light Control portfolio with the option for random row addressing. The DLPC410 is a digital controller that supports both the 0.7 XGA chipset and 0.95 1080p chipset. DLPC410 provides reliable operation of two groups of digital micromirror device (DMD) options, DLP7000 / DLP7000UV and DLP9500 / DLP9500UV; reliable operation of the DLPA200 DMD Micromirror Driver; and a convenient, multi-functional interface between user electronics and the DMD.

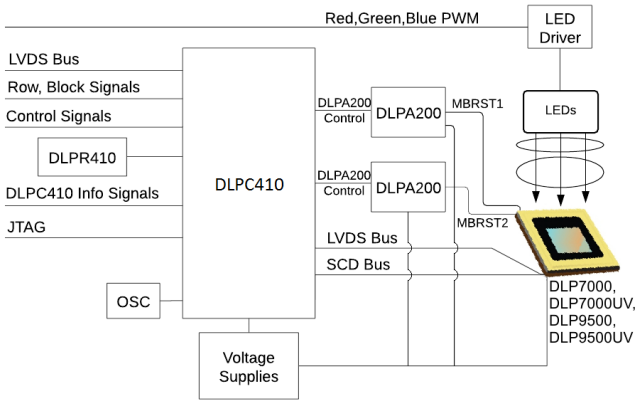
The DLPC410 provides a high-speed data and control interface for the DLP7000 / DLP7000UV DMD and DLP9500 / DLP9500UV DMD enabling binary pattern rates of up to 32 kHz and 23 kHz, respectively. These fast pattern rates set DLP technology apart from other spatial light modulators and offer customers a strategic advantage for equipment needing fast, accurate, and programmable light steering capability. Moreover, the DLPC410 provides the DMD mirror clocking pulse and timing information to the DLPA200 DMD Micromirror Driver. The unique capability and value offered by DLPC410 makes it well suited to support a wide variety of industrial, medical, and advanced display applications.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DLPC410	FCBGA (676)	27.00 mm x 27.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Diagram



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (June 2013) to Revision C **Page**

- Added *ESD Rating* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Removed references to Discovery 4100 and deleted DLPR4101 throughout document ... 1
- Added DLP7000UV and DLP9500UV to *Features* and *Description* ... 1
- Added note - Xlilinx System Monitor analog supply & ground - "must be connected to ground" (AVDD_0 & AVSS_0) ... 6
- Changed "DAD A" descriptions to "DLPA200 number 1" and "DAD B" descriptions to "DLPA200 number 2" ... 6
- Reversed DDC_B*nn*_VR pairs pullups / pulldowns (for *nn* =12, 15, and 16)) ... 7
- Changed Pin # C22 name from DDC_B11_VRP (duplicate) to DDC_B15_VRP ... 7
- Added "Not used" to description for DMD_B_RESET and $\overline{\text{DMD\_B\_SCPEN}}$ ... 13
- Added TP14 and TP17 note - Xilinx Temperature Diode ... 13
- Added "in Reference Design" to ECP2 Mictor pin notes ... 13
- Changed ECP2 pin description from "Not Defined" to "Not Used" ... 13
- Added ECP2_M_TP[3:29] descriptions and active state ... 14
- Deleted duplicate pin numbers M13 and M14 ... 15
- Changed Description from "DMD Power" to "DMD Power Good indicator" ... 15
- Changed duplicate pin name from RSVD_0 to RSVD_1 ... 16
- Updated pin description for SCPDI and SCPDO ... 16
- Changed STEPVCC to connect to ground, active "Hi" to "-", and clock to "-" ... 16
- Changed Description from "JTAG Data Clock" to "JTAG Data" ... 16
- Changed pin names for VCCO_*n*_*n* pins to list each pin separately ... 17
- Added note about Xilinx System Monitor differential pins (VN_0 & VP_0) and reference voltage (VREFN_0 & VREFP_0) ... 17
- Changed Description from "DMD Reset Watchdog" to "DMD Mirror Clocking Pulse Watchdog" ... 18

Revision History (continued)

- Deleted duplicate pin numbers in "UNUSED" pin list 18
- Updated the functional block diagrams 22
- Moved DLP7000 / DLP7000UV and DLP9500 / DLP9500UV Example Block Diagrams from Functional Block Diagram section to Typical Application Section 23
- Deleted the "Step DMD SRAM Memory Voltage" and "Load 4" Enhanced Functionality (with DLPR4101 PROM only)" sections 39
- Updated the embedded example block diagrams 42
- Added DLP7000UV and DLP9500UV well suited for direct imaging lithography, 3D printing, and UV applications 43
- Added Debugging Guidelines section 43
- Changed maximum differential trace length from 100 to 150 matching Table 13 48
- Added DLP7000UV and DLP9500UV Related Documentation 59

Changes from Revision A (September 2012) to Revision B **Page**

- Changed Feature From: 1-Bit Binary Pattern Rates up to 32-kHz To: 1-Bit Binary Pattern Rates up to 32-kHz (up to 48-kHz when used with DLPR4101) 1
- Added Section "Load 4" Enhanced Functionality (with DLPR4101 PROM only) 39
- Added DLPR4101 to DLPR410 59

Changes from Original (August 2012) to Revision A **Page**

5 Description (continued)

In DLP-based electronics solutions, image data is 100% digital from the DLPC410 input port to the projected image. The image stays in digital form and is never converted into an analog signal. The DLPC410 processes the digital input image and converts the data into a format needed by the image on the DMD. The DMD then steers the light using binary pulse-width modulation (PWM) for each pixel mirror.

6 Device Options

The DLPC410 is the DMD controller for the DLP7000 / DLP7000UV and DLP9500 / DLP9500UV Chipsets (see Figure 4 and Figure 5). A dedicated chipset provides developers easy access to the DMD as well as high speed, independent micromirror control. See the list of required chipset components in Table 1:

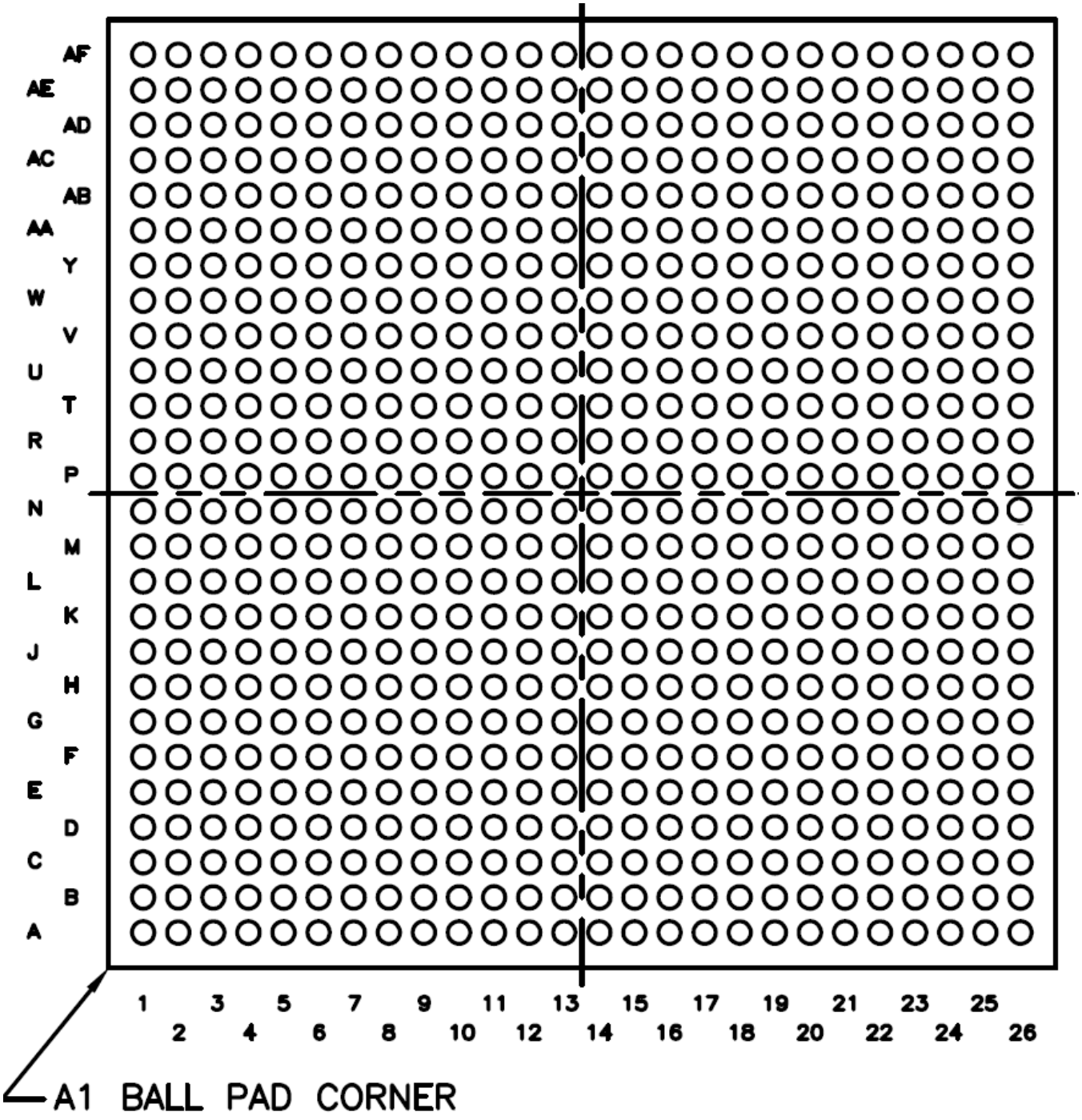
Table 1. DLPC410 Chipset Configurations

0.7 XGA CHIPSET				0.95 1080p CHIPSET		
QTY	TI PART	DESCRIPTION		QTY	TI PART	DESCRIPTION
1	DLP7000 or DLP7000UV	0.7 XGA Type A DMD (digital micromirror device)		1	DLP9500 or DLP9500UV	0.95 1080p Type A DMD (digital micromirror device)
1	DLPR410	DLPC410 Configuration PROM		1	DLPR410	DLPC410 Configuration PROM
1	DLPA200	DMD Micromirror Driver		2	DLPA200	DMD Micromirror Driver

Reliable function and operation of the DLPC410 requires that it be used in conjunction with the other components of the chipset in Table 1. For more information on the chipset components, see the data sheets in the *Related Documentation*).

7 Pin Configuration and Functions

ZYR Package
676-Pin FCBGA
Bottom View



Pin Functions

PIN		TYPE	SIGNAL	TERMINATION /NOTES	ACTIVE (Hi or Lo)	CLOCK	DATA RATE	DESCRIPTION
NAME	NO.							
APPS_CNTL_DPN	F7	-	-	This pair connected with 100 Ω resistor between pair.	-	-		Not Used
APPS_CNTL_DPP	E7	-	-		-	-		Not Used
$\overline{ARST}$	AC13	I	LVCMOS25_S_12_I		Lo	-		DLPC410 Reset
AVDD_0	M14	-	-	Not used - connect to Ground (no name in Reference Design)	-	-		Xilinx System Monitor analog supply - (not used - must be connected to ground)
AVSS_0	M13	-	-	Not used - connect to Ground (no name in Reference Design)	-	-		Xilinx System Monitor analog ground - (not used - must be connected to ground)
BLKAD_0	E12	I	LVCMOS25_S_12_I		Hi = 1	DDC_DCLK_[A,B,C,D]		Block Address bit 0
BLKAD_1	D13	I	LVCMOS25_S_12_I		Hi = 1	DDC_DCLK_[A,B,C,D]		Block Address bit 1
BLKAD_2	E13	I	LVCMOS25_S_12_I		Hi = 1	DDC_DCLK_[A,B,C,D]		Block Address bit 2
BLKAD_3	F13	I	LVCMOS25_S_12_I		Hi = 1	DDC_DCLK_[A,B,C,D]		Block Address bit 3
BLKMD_0	H13	I	LVCMOS25_S_12_I		Hi = 1	DDC_DCLK_[A,B,C,D]		Block Mode Bit 0
BLKMD_1	H14	I	LVCMOS25_S_12_I		Hi = 1	DDC_DCLK_[A,B,C,D]		Block Mode Bit 1
CLKIN_R	AD13	I	LVCMOS25_S_12_I		-	Reference Clock		Reference Clock
COMP_DATA	G19	I	LVCMOS25_S_12_I		Hi	DDC_DCLK_[A,B,C,D]		Compliment Data (0 <--> 1)
CS_B_0	N18	-	-	1 kΩ pulldown to ground	Lo	-		Xilinx Config
D_OUT_BUSY_0	W11	-	NC	Do not connect	-	-		Not Used
DAD_A_ADDR0	E1	O	LVCMOS25_F_12_O	Connected to DLPA200 number 1 Address 0 pin	Hi = 1	-		DLPA200 Number 1 Reset Block bit 0
DAD_A_ADDR1	E2	O	LVCMOS25_F_12_O	Connected to DLPA200 Number 1 Address 1 pin	Hi = 1	-		DLPA200 Number 1 Reset Block bit 1
DAD_A_ADDR2	E3	O	LVCMOS25_F_12_O	Connected to DLPA200 Number 1 Address 2 pin	Hi = 1	-		DLPA200 Number 1 Reset Block bit 2
DAD_A_ADDR3	F3	O	LVCMOS25_F_12_O	Connected to DLPA200 Number 1 Address 3 pin	Hi = 1	-		DLPA200 Number 1 Reset Block bit 3
DAD_A_MODE0	C1	O	LVCMOS25_F_12_O	Connected to DLPA200 Number 1 Mode 0 pin	Hi = 1	-		DLPA200 Number 1Mode bit 0
DAD_A_MODE1	D1	O	LVCMOS25_F_12_O	Connected to DLPA200 Number 1 Mode 1 pin	Hi = 1	-		DLPA200 Number 1 Mode bit 1
$\overline{DAD\_A\_SCPEN}$	AE3	O	LVCMOS25_F_12_O	Connected to DLPA200 Number 1 $\overline{SCPEN}$ pin	Lo	-		DLPA200 Number 1 SCP Communication Enable
DAD_A_SEL0	AB12	O	LVCMOS25_F_12_O	Connected to DLPA200 Number 1 SEL 0 pin	Hi = 1	-		DLPA200 Number 1 Address bit 0
DAD_A_SEL1	AC12	O	LVCMOS25_F_12_O	Connected to DLPA200 Number 1 SEL 1 pin	Hi = 1	-		DLPA200 Number 1 Address bit 1
DAD_A_STROBE	AF3	O	LVCMOS25_F_12_O	Connected to DLPA200 Number 1 STROBE pin	Hi	-		DLPA200 Number 1 Transition Strobe
DAD_B_ADDR0	E26	O	LVCMOS25_F_12_O	Connected to DLPA200 Number 2 Address 1 pin	Hi = 1	-		DLPA200 Number 2 Reset Block bit 0
DAD_B_ADDR1	E25	O	LVCMOS25_F_12_O	Connected to DLPA200 Number 2 Address 2 pin	Hi = 1	-		DLPA200 Number 2 Reset Block bit 1
DAD_B_ADDR2	F25	O	LVCMOS25_F_12_O	Connected to DLPA200 Number 2 Address 3 pin	Hi = 1	-		DLPA200 Number 2 Reset Block bit 2
DAD_B_ADDR3	F24	O	LVCMOS25_F_12_O	Connected to DLPA200 Number 2 Address 0 pin	Hi = 1	-		DLPA200 Number 2 Reset Block bit 3
DAD_B_MODE0	D26	O	LVCMOS25_F_12_O	Connected to DLPA200 Number 2 Mode 0 pin	Hi = 1	-		DLPA200 Number 2 Mode bit 0
DAD_B_MODE1	D25	O	LVCMOS25_F_12_O	Connected to DLPA200 Number 2 Mode 1 pin	Hi = 1	-		DLPA200 Number 2 Mode bit 1
$\overline{DAD\_B\_SCPEN}$	AB19	O	LVCMOS25_F_12_O	Connected to DLPA200 Number 2 $\overline{SCPEN}$ pin	Lo	-		DLPA200 Number 2 SCP Communication Enable
DAD_B_SEL0	R22	O	LVCMOS25_F_12_O	Connected to DLPA200 Number 2 SEL 0 pin	Hi = 1	-		DLPA200 Number 2 Address bit 0
DAD_B_SEL1	R23	O	LVCMOS25_F_12_O	Connected to DLPA200 Number 2 SEL 1 pin	Hi = 1	-		DLPA200 Number 2 Address bit 1
DAD_B_STROBE	AB20	O	LVCMOS25_F_12_O	Connected to DLPA200 Number 2 STROBE pin	Hi	-		DLPA200 Number 2 Transition Strobe

Pin Functions (continued)

PIN		TYPE	SIGNAL	TERMINATION /NOTES	ACTIVE (Hi or Lo)	CLOCK	DATA RATE	DESCRIPTION
NAME	NO.							
DAD_INIT	AF4	O	LVCMOS25_F_12_O	Connected to DLPA200 Number 1 and Number 2 $\overline{\text{RESET}}$ pin	Hi	-		DLPA200 Number 1 / Number 2 Init
$\overline{\text{DAD\_OE}}$	AF5	O	LVCMOS25_F_12_O	Connected to DLPA200 Number 1 and Number 2 $\overline{\text{OE}}$ pin	Lo	-		DLPA200 Number 1 / Number 2 Output Enable
DDC_B11_VRN	L23	-	REFERENCE	51.1 Ω pullup to 2.5 V	-	-		Reference Voltage
DDC_B11_VRP	L22	-	REFERENCE	51.1 Ω pulldown to ground	-	-		Reference Ground
DDC_B12_VRN	M5	-	REFERENCE	51.1 Ω pullup to 2.5 V	-	-		Reference Voltage
DDC_B12_VRP	M6	-	REFERENCE	51.1 Ω pulldown to ground	-	-		Reference Ground
DDC_B15_VRN	D23	-	REFERENCE	51.1 Ω pullup to 2.5 V	-	-		Reference Voltage
DDC_B15_VRP	C22	-	REFERENCE	51.1 Ω pulldown to ground	-	-		Reference Ground
DDC_B16_VRN	A4	-	REFERENCE	51.1 Ω pullup to 2.5 V	-	-		Reference Voltage
DDC_B16_VRP	A5	-	REFERENCE	51.1 Ω pulldown to ground	-	-		Reference Ground
DDC_DCLK_A_DPN	B21	I	LVDS_25	100 Ω across pair (not terminated in the DLPC410)	-	-		Bank A Input Clock (Neg)
DDC_DCLK_A_DPP	C21	I	LVDS_25_I		-	-		Bank A Input Clock (Pos)
DDC_DCLK_B_DPN	A7	I	LVDS_25	100 Ω across pair (not terminated in the DLPC410)	-	-		Bank B Input Clock (Neg)
DDC_DCLK_B_DPP	B7	I	LVDS_25_I		-	-		Bank B Input Clock (Pos)
DDC_DCLK_C_DPN	K20	I	LVDS_25	100 Ω across pair (not terminated in the DLPC410)	-	-		Bank C Input Clock (Neg)
DDC_DCLK_C_DPP	K21	I	LVDS_25_I		-	-		Bank C Input Clock (Pos)
DDC_DCLK_D_DPN	L5	I	LVDS_25	100 Ω across pair (not terminated in the DLPC410)	-	-		Bank D Input Clock (Neg)
DDC_DCLK_D_DPP	K5	I	LVDS_25_I		-	-		Bank D Input Clock (Pos)
DDC_DCLKOUT_A_DPN	N1	O	LVDS_25	Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω)	-	-		Bank A Output Clock (Neg)
DDC_DCLKOUT_A_DPP	M1	O	LVDS_25_O		-	-		Bank A Output Clock (Pos)
DDC_DCLKOUT_B_DPN	Y5	O	LVDS_25	Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω)	-	-		Bank B Output Clock (Neg)
DDC_DCLKOUT_B_DPP	Y6	O	LVDS_25_O		-	-		Bank B Output Clock (Pos)
DDC_DCLKOUT_C_DPN	AA22	O	LVDS_25	Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω)	-	-		Bank C Output Clock (Neg)
DDC_DCLKOUT_C_DPP	AB22	O	LVDS_25_O		-	-		Bank C Output Clock (Pos)
DDC_DCLKOUT_D_DPN	M26	O	LVDS_25	Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω)	-	-		Bank D Output Clock (Neg)
DDC_DCLKOUT_D_DPP	M25	O	LVDS_25_O		-	-		Bank D Output Clock (Pos)
DDC_DIN_A0_DPN	A15	I	LVDS_25	100 Ω across pair (not terminated in the DLPC410)	-	DDC_DCLK_A	DDR	Data A bit 0 Input (Neg)
DDC_DIN_A0_DPP	A14	I	LVDS_25_I		-	DDC_DCLK_A	DDR	Data A bit 0 Input (Pos)
DDC_DIN_A1_DPN	B14	I	LVDS_25	100 Ω across pair (not terminated in the DLPC410)	-	DDC_DCLK_A	DDR	Data A bit 1 Input (Neg)
DDC_DIN_A1_DPP	C14	I	LVDS_25_I		-	DDC_DCLK_A	DDR	Data A bit 1 Input (Pos)
DDC_DIN_A2_DPN	B16	I	LVDS_25	100 Ω across pair (not terminated in the DLPC410)	-	DDC_DCLK_A	DDR	Data A bit 2 Input (Neg)
DDC_DIN_A2_DPP	B15	I	LVDS_25_I		-	DDC_DCLK_A	DDR	Data A bit 2 Input (Pos)
DDC_DIN_A3_DPN	C16	I	LVDS_25	100 Ω across pair (not terminated in the DLPC410)	-	DDC_DCLK_A	DDR	Data A bit 3 Input (Neg)
DDC_DIN_A3_DPP	D16	I	LVDS_25_I		-	DDC_DCLK_A	DDR	Data A bit 3 Input (Pos)
DDC_DIN_A4_DPN	A17	I	LVDS_25	100 Ω across pair (not terminated in the DLPC410)	-	DDC_DCLK_A	DDR	Data A bit 4 Input (Neg)
DDC_DIN_A4_DPP	B17	I	LVDS_25_I		-	DDC_DCLK_A	DDR	Data A bit 4 Input (Pos)
DDC_DIN_A5_DPN	C17	I	LVDS_25	100 Ω across pair (not terminated in the DLPC410)	-	DDC_DCLK_A	DDR	Data A bit 5 Input (Neg)
DDC_DIN_A5_DPP	D18	I	LVDS_25_I		-	DDC_DCLK_A	DDR	Data A bit 5 Input (Pos)
DDC_DIN_A6_DPN	A19	I	LVDS_25	100 Ω across pair (not terminated in the DLPC410)	-	DDC_DCLK_A	DDR	Data A bit 6 Input (Neg)
DDC_DIN_A6_DPP	A18	I	LVDS_25_I		-	DDC_DCLK_A	DDR	Data A bit 6 Input (Pos)
DDC_DIN_A7_DPN	C18	I	LVDS_25	100 Ω across pair (not terminated in the DLPC410)	-	DDC_DCLK_A	DDR	Data A bit 7 Input (Neg)
DDC_DIN_A7_DPP	B19	I	LVDS_25_I		-	DDC_DCLK_A	DDR	Data A bit 7 Input (Pos)
DDC_DIN_A8_DPN	D19	I	LVDS_25	100 Ω across pair (not terminated in the DLPC410)	-	DDC_DCLK_A	DDR	Data A bit 8 Input (Neg)
DDC_DIN_A8_DPP	C19	I	LVDS_25_I		-	DDC_DCLK_A	DDR	Data A bit 8 Input (Pos)
DDC_DIN_A9_DPN	B20	I	LVDS_25	100 Ω across pair (not terminated in the DLPC410)	-	DDC_DCLK_A	DDR	Data A bit 9 Input (Neg)
DDC_DIN_A9_DPP	A20	I	LVDS_25_I		-	DDC_DCLK_A	DDR	Data A bit 9 Input (Pos)
DDC_DIN_A10_DPN	A22	I	LVDS_25	100 Ω across pair (not terminated in the DLPC410)	-	DDC_DCLK_A	DDR	Data A bit 10 Input (Neg)
DDC_DIN_A10_DPP	B22	I	LVDS_25_I		-	DDC_DCLK_A	DDR	Data A bit 10 Input (Pos)
DDC_DIN_A11_DPN	A24	I	LVDS_25	100 Ω across pair (not terminated in the DLPC410)	-	DDC_DCLK_A	DDR	Data A bit 11 Input (Neg)
DDC_DIN_A11_DPP	A23	I	LVDS_25_I		-	DDC_DCLK_A	DDR	Data A bit 11 Input (Pos)

Pin Functions (continued)

PIN		TYPE	SIGNAL	TERMINATION /NOTES	ACTIVE (Hi or Lo)	CLOCK	DATA RATE	DESCRIPTION
NAME	NO.							
DDC_DIN_A12_DPN	C23	I	LVDS_25	100 Ω across pair (not terminated in the DLPC410)	-	DDC_DCLK_A	DDR	Data A bit 12 Input (Neg)
DDC_DIN_A12_DPP	B24	I	LVDS_25_I		-	DDC_DCLK_A	DDR	Data A bit 12 Input (Pos)
DDC_DIN_A13_DPN	C24	I	LVDS_25	100 Ω across pair (not terminated in the DLPC410)	-	DDC_DCLK_A	DDR	Data A bit 13 Input (Neg)
DDC_DIN_A13_DPP	D24	I	LVDS_25_I		-	DDC_DCLK_A	DDR	Data A bit 13 Input (Pos)
DDC_DIN_A14_DPN	A25	I	LVDS_25	100 Ω across pair (not terminated in the DLPC410)	-	DDC_DCLK_A	DDR	Data A bit 14 Input (Neg)
DDC_DIN_A14_DPP	B25	I	LVDS_25_I		-	DDC_DCLK_A	DDR	Data A bit 14 Input (Pos)
DDC_DIN_A15_DPN	C26	I	LVDS_25	100 Ω across pair (not terminated in the DLPC410)	-	DDC_DCLK_A	DDR	Data A bit 15 Input (Neg)
DDC_DIN_A15_DPP	B26	I	LVDS_25_I		-	DDC_DCLK_A	DDR	Data A bit 15 Input (Pos)
DDC_DIN_B0_DPN	A12	I	LVDS_25	100 Ω across pair (not terminated in the DLPC410)	-	DDC_DCLK_B	DDR	Data B bit 0 Input (Neg)
DDC_DIN_B0_DPP	A13	I	LVDS_25_I		-	DDC_DCLK_B	DDR	Data B bit 0 Input (Pos)
DDC_DIN_B1_DPN	B12	I	LVDS_25	100 Ω across pair (not terminated in the DLPC410)	-	DDC_DCLK_B	DDR	Data B bit 1 Input (Neg)
DDC_DIN_B1_DPP	C13	I	LVDS_25_I		-	DDC_DCLK_B	DDR	Data B bit 1 Input (Pos)
DDC_DIN_B2_DPN	D10	I	LVDS_25	100 Ω across pair (not terminated in the DLPC410)	-	DDC_DCLK_B	DDR	Data B bit 2 Input (Neg)
DDC_DIN_B2_DPP	D11	I	LVDS_25_I		-	DDC_DCLK_B	DDR	Data B bit 2 Input (Pos)
DDC_DIN_B3_DPN	C12	I	LVDS_25	100 Ω across pair (not terminated in the DLPC410)	-	DDC_DCLK_B	DDR	Data B bit 3 Input (Neg)
DDC_DIN_B3_DPP	C11	I	LVDS_25_I		-	DDC_DCLK_B	DDR	Data B bit 3 Input (Pos)
DDC_DIN_B4_DPN	A10	I	LVDS_25	100 Ω across pair (not terminated in the DLPC410)	-	DDC_DCLK_B	DDR	Data B bit 4 Input (Neg)
DDC_DIN_B4_DPP	B11	I	LVDS_25_I		-	DDC_DCLK_B	DDR	Data B bit 4 Input (Pos)
DDC_DIN_B5_DPN	D9	I	LVDS_25	100 Ω across pair (not terminated in the DLPC410)	-	DDC_DCLK_B	DDR	Data B bit 5 Input (Neg)
DDC_DIN_B5_DPP	C9	I	LVDS_25_I		-	DDC_DCLK_B	DDR	Data B bit 5 Input (Pos)
DDC_DIN_B6_DPN	B10	I	LVDS_25	100 Ω across pair (not terminated in the DLPC410)	-	DDC_DCLK_B	DDR	Data B bit 6 Input (Neg)
DDC_DIN_B6_DPP	B9	I	LVDS_25_I		-	DDC_DCLK_B	DDR	Data B bit 6 Input (Pos)
DDC_DIN_B7_DPN	A8	I	LVDS_25	100 Ω across pair (not terminated in the DLPC410)	-	DDC_DCLK_B	DDR	Data B bit 7 Input (Neg)
DDC_DIN_B7_DPP	A9	I	LVDS_25_I		-	DDC_DCLK_B	DDR	Data B bit 7 Input (Pos)
DDC_DIN_B8_DPN	D6	I	LVDS_25	100 Ω across pair (not terminated in the DLPC410)	-	DDC_DCLK_B	DDR	Data B bit 8 Input (Neg)
DDC_DIN_B8_DPP	D5	I	LVDS_25_I		-	DDC_DCLK_B	DDR	Data B bit 8 Input (Pos)
DDC_DIN_B9_DPN	C7	I	LVDS_25	100 Ω across pair (not terminated in the DLPC410)	-	DDC_DCLK_B	DDR	Data B bit 9 Input (Neg)
DDC_DIN_B9_DPP	C6	I	LVDS_25_I		-	DDC_DCLK_B	DDR	Data B bit 9 Input (Pos)
DDC_DIN_B10_DPN	B6	I	LVDS_25	100 Ω across pair (not terminated in the DLPC410)	-	DDC_DCLK_B	DDR	Data B bit 10 Input (Neg)
DDC_DIN_B10_DPP	B5	I	LVDS_25_I		-	DDC_DCLK_B	DDR	Data B bit 10 Input (Pos)
DDC_DIN_B11_DPN	D4	I	LVDS_25	100 Ω across pair (not terminated in the DLPC410)	-	DDC_DCLK_B	DDR	Data B bit 11 Input (Neg)
DDC_DIN_B11_DPP	D3	I	LVDS_25_I		-	DDC_DCLK_B	DDR	Data B bit 11 Input (Pos)
DDC_DIN_B12_DPN	B4	I	LVDS_25	100 Ω across pair (not terminated in the DLPC410)	-	DDC_DCLK_B	DDR	Data B bit 12 Input (Neg)
DDC_DIN_B12_DPP	C4	I	LVDS_25_I		-	DDC_DCLK_B	DDR	Data B bit 12 Input (Pos)
DDC_DIN_B13_DPN	C3	I	LVDS_25	100 Ω across pair (not terminated in the DLPC410)	-	DDC_DCLK_B	DDR	Data B bit 13 Input (Neg)
DDC_DIN_B13_DPP	C2	I	LVDS_25_I		-	DDC_DCLK_B	DDR	Data B bit 13 Input (Pos)
DDC_DIN_B14_DPN	A3	I	LVDS_25	100 Ω across pair (not terminated in the DLPC410)	-	DDC_DCLK_B	DDR	Data B bit 14 Input (Neg)
DDC_DIN_B14_DPP	A2	I	LVDS_25_I		-	DDC_DCLK_B	DDR	Data B bit 14 Input (Pos)
DDC_DIN_B15_DPN	B2	I	LVDS_25	100 Ω across pair (not terminated in the DLPC410)	-	DDC_DCLK_B	DDR	Data B bit 15 Input (Neg)
DDC_DIN_B15_DPP	B1	I	LVDS_25_I		-	DDC_DCLK_B	DDR	Data B bit 15 Input (Pos)
DDC_DIN_C0_DPN	E20	I	LVDS_25	100 Ω across pair (not terminated in the DLPC410)	-	DDC_DCLK_C	DDR	Data C bit 0 Input (Neg)
DDC_DIN_C0_DPP	E21	I	LVDS_25_I		-	DDC_DCLK_C	DDR	Data C bit 0 Input (Pos)
DDC_DIN_C1_DPN	F20	I	LVDS_25	100 Ω across pair (not terminated in the DLPC410)	-	DDC_DCLK_C	DDR	Data C bit 1 Input (Neg)
DDC_DIN_C1_DPP	G20	I	LVDS_25_I		-	DDC_DCLK_C	DDR	Data C bit 1 Input (Pos)
DDC_DIN_C2_DPN	H19	I	LVDS_25	100 Ω across pair (not terminated in the DLPC410)	-	DDC_DCLK_C	DDR	Data C bit 2 Input (Neg)
DDC_DIN_C2_DPP	J19	I	LVDS_25_I		-	DDC_DCLK_C	DDR	Data C bit 2 Input (Pos)
DDC_DIN_C3_DPN	E23	I	LVDS_25	100 Ω across pair (not terminated in the DLPC410)	-	DDC_DCLK_C	DDR	Data C bit 3 Input (Neg)
DDC_DIN_C3_DPP	E22	I	LVDS_25_I		-	DDC_DCLK_C	DDR	Data C bit 3 Input (Pos)
DDC_DIN_C4_DPN	F23	I	LVDS_25	100 Ω across pair (not terminated in the DLPC410)	-	DDC_DCLK_C	DDR	Data C bit 4 Input (Neg)
DDC_DIN_C4_DPP	F22	I	LVDS_25_I		-	DDC_DCLK_C	DDR	Data C bit 4 Input (Pos)
DDC_DIN_C5_DPN	G22	I	LVDS_25	100 Ω across pair (not terminated in the DLPC410)	-	DDC_DCLK_C	DDR	Data C bit 5 Input (Neg)
DDC_DIN_C5_DPP	G21	I	LVDS_25_I		-	DDC_DCLK_C	DDR	Data C bit 5 Input (Pos)
DDC_DIN_C6_DPN	J20	I	LVDS_25	100 Ω across pair (not terminated in the DLPC410)	-	DDC_DCLK_C	DDR	Data C bit 6 Input (Neg)
DDC_DIN_C6_DPP	J21	I	LVDS_25_I		-	DDC_DCLK_C	DDR	Data C bit 6 Input (Pos)

Pin Functions (continued)

PIN		TYPE	SIGNAL	TERMINATION /NOTES	ACTIVE (Hi or Lo)	CLOCK	DATA RATE	DESCRIPTION
NAME	NO.							
DDC_DIN_C7_DPN	H22	I	LVDS_25	100 Ω across pair (not terminated in the DLPC410)	-	DDC_DCLK_C	DDR	Data C bit 7 Input (Neg)
DDC_DIN_C7_DPP	H21	I	LVDS_25_I		-	DDC_DCLK_C	DDR	Data C bit 7 Input (Pos)
DDC_DIN_C8_DPN	J23	I	LVDS_25	100 Ω across pair (not terminated in the DLPC410)	-	DDC_DCLK_C	DDR	Data C bit 8 Input (Neg)
DDC_DIN_C8_DPP	H23	I	LVDS_25_I		-	DDC_DCLK_C	DDR	Data C bit 8 Input (Pos)
DDC_DIN_C9_DPN	K22	I	LVDS_25	100 Ω across pair (not terminated in the DLPC410)	-	DDC_DCLK_C	DDR	Data C bit 9 Input (Neg)
DDC_DIN_C9_DPP	K23	I	LVDS_25_I		-	DDC_DCLK_C	DDR	Data C bit 9 Input (Pos)
DDC_DIN_C10_DPN	M19	I	LVDS_25	100 Ω across pair (not terminated in the DLPC410)	-	DDC_DCLK_C	DDR	Data C bit 10 Input (Neg)
DDC_DIN_C10_DPP	M20	I	LVDS_25_I		-	DDC_DCLK_C	DDR	Data C bit 10 Input (Pos)
DDC_DIN_C11_DPN	M21	I	LVDS_25	100 Ω across pair (not terminated in the DLPC410)	-	DDC_DCLK_C	DDR	Data C bit 11 Input (Neg)
DDC_DIN_C11_DPP	M22	I	LVDS_25_I		-	DDC_DCLK_C	DDR	Data C bit 11 Input (Pos)
DDC_DIN_C12_DPN	N19	I	LVDS_25	100 Ω across pair (not terminated in the DLPC410)	-	DDC_DCLK_C	DDR	Data C bit 12 Input (Neg)
DDC_DIN_C12_DPP	P19	I	LVDS_25_I		-	DDC_DCLK_C	DDR	Data C bit 12 Input (Pos)
DDC_DIN_C13_DPN	N21	I	LVDS_25	100 Ω across pair (not terminated in the DLPC410)	-	DDC_DCLK_C	DDR	Data C bit 13 Input (Neg)
DDC_DIN_C13_DPP	N22	I	LVDS_25_I		-	DDC_DCLK_C	DDR	Data C bit 13 Input (Pos)
DDC_DIN_C14_DPN	P20	I	LVDS_25	100 Ω across pair (not terminated in the DLPC410)	-	DDC_DCLK_C	DDR	Data C bit 14 Input (Neg)
DDC_DIN_C14_DPP	P21	I	LVDS_25_I		-	DDC_DCLK_C	DDR	Data C bit 14 Input (Pos)
DDC_DIN_C15_DPN	N23	I	LVDS_25	100 Ω across pair (not terminated in the DLPC410)	-	DDC_DCLK_C	DDR	Data C bit 15 Input (Neg)
DDC_DIN_C15_DPP	P23	I	LVDS_25_I		-	DDC_DCLK_C	DDR	Data C bit 15 Input (Pos)
DDC_DIN_D0_DPN	T3	I	LVDS_25	100 Ω across pair (not terminated in the DLPC410)	-	DDC_DCLK_D	DDR	Data D bit 0 Input (Neg)
DDC_DIN_D0_DPP	R3	I	LVDS_25_I		-	DDC_DCLK_D	DDR	Data D bit 0 Input (Pos)
DDC_DIN_D1_DPN	R5	I	LVDS_25	100 Ω across pair (not terminated in the DLPC410)	-	DDC_DCLK_D	DDR	Data D bit 1 Input (Neg)
DDC_DIN_D1_DPP	R6	I	LVDS_25_I		-	DDC_DCLK_D	DDR	Data D bit 1 Input (Pos)
DDC_DIN_D2_DPN	R7	I	LVDS_25	100 Ω across pair (not terminated in the DLPC410)	-	DDC_DCLK_D	DDR	Data D bit 2 Input (Neg)
DDC_DIN_D2_DPP	P6	I	LVDS_25_I		-	DDC_DCLK_D	DDR	Data D bit 2 Input (Pos)
DDC_DIN_D3_DPN	N3	I	LVDS_25	100 Ω across pair (not terminated in the DLPC410)	-	DDC_DCLK_D	DDR	Data D bit 3 Input (Neg)
DDC_DIN_D3_DPP	P3	I	LVDS_25_I		-	DDC_DCLK_D	DDR	Data D bit 3 Input (Pos)
DDC_DIN_D4_DPN	P4	I	LVDS_25	100 Ω across pair (not terminated in the DLPC410)	-	DDC_DCLK_D	DDR	Data D bit 4 Input (Neg)
DDC_DIN_D4_DPP	P5	I	LVDS_25_I		-	DDC_DCLK_D	DDR	Data D bit 4 Input (Pos)
DDC_DIN_D5_DPN	N6	I	LVDS_25	100 Ω across pair (not terminated in the DLPC410)	-	DDC_DCLK_D	DDR	Data D bit 5 Input (Neg)
DDC_DIN_D5_DPP	N7	I	LVDS_25_I		-	DDC_DCLK_D	DDR	Data D bit 5 Input (Pos)
DDC_DIN_D6_DPN	N4	I	LVDS_25	100 Ω across pair (not terminated in the DLPC410)	-	DDC_DCLK_D	DDR	Data D bit 6 Input (Neg)
DDC_DIN_D6_DPP	M4	I	LVDS_25_I		-	DDC_DCLK_D	DDR	Data D bit 6 Input (Pos)
DDC_DIN_D7_DPN	M7	I	LVDS_25	100 Ω across pair (not terminated in the DLPC410)	-	DDC_DCLK_D	DDR	Data D bit 7 Input (Neg)
DDC_DIN_D7_DPP	L7	I	LVDS_25_I		-	DDC_DCLK_D	DDR	Data D bit 7 Input (Pos)
DDC_DIN_D8_DPN	K7	I	LVDS_25	100 Ω across pair (not terminated in the DLPC410)	-	DDC_DCLK_D	DDR	Data D bit 8 Input (Neg)
DDC_DIN_D8_DPP	K6	I	LVDS_25_I		-	DDC_DCLK_D	DDR	Data D bit 8 Input (Pos)
DDC_DIN_D9_DPN	J4	I	LVDS_25	100 Ω across pair (not terminated in the DLPC410)	-	DDC_DCLK_D	DDR	Data D bit 9 Input (Neg)
DDC_DIN_D9_DPP	J5	I	LVDS_25_I		-	DDC_DCLK_D	DDR	Data D bit 9 Input (Pos)
DDC_DIN_D10_DPN	H7	I	LVDS_25	100 Ω across pair (not terminated in the DLPC410)	-	DDC_DCLK_D	DDR	Data D bit 10 Input (Neg)
DDC_DIN_D10_DPP	J6	I	LVDS_25_I		-	DDC_DCLK_D	DDR	Data D bit 10 Input (Pos)
DDC_DIN_D11_DPN	G4	I	LVDS_25	100 Ω across pair (not terminated in the DLPC410)	-	DDC_DCLK_D	DDR	Data D bit 11 Input (Neg)
DDC_DIN_D11_DPP	H4	I	LVDS_25_I		-	DDC_DCLK_D	DDR	Data D bit 11 Input (Pos)
DDC_DIN_D12_DPN	G5	I	LVDS_25	100 Ω across pair (not terminated in the DLPC410)	-	DDC_DCLK_D	DDR	Data D bit 12 Input (Neg)
DDC_DIN_D12_DPP	H6	I	LVDS_25_I		-	DDC_DCLK_D	DDR	Data D bit 12 Input (Pos)
DDC_DIN_D13_DPN	G7	I	LVDS_25	100 Ω across pair (not terminated in the DLPC410)	-	DDC_DCLK_D	DDR	Data D bit 13 Input (Neg)
DDC_DIN_D13_DPP	G6	I	LVDS_25_I		-	DDC_DCLK_D	DDR	Data D bit 13 Input (Pos)
DDC_DIN_D14_DPN	F4	I	LVDS_25	100 Ω across pair (not terminated in the DLPC410)	-	DDC_DCLK_D	DDR	Data D bit 14 Input (Neg)
DDC_DIN_D14_DPP	F5	I	LVDS_25_I		-	DDC_DCLK_D	DDR	Data D bit 14 Input (Pos)
DDC_DIN_D15_DPN	E5	I	LVDS_25	100 Ω across pair (not terminated in the DLPC410)	-	DDC_DCLK_D	DDR	Data D bit 15 Input (Neg)
DDC_DIN_D15_DPP	E6	I	LVDS_25_I		-	DDC_DCLK_D	DDR	Data D bit 15 Input (Pos)
DDC_DOUT_A0_DPN	AE2	O	LVDS_25	Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω)	-	DDC_DCLKOUT_A	DDR	Data A bit 0 Output (Neg)
DDC_DOUT_A0_DPP	AF2	O	LVDS_25_O		-	DDC_DCLKOUT_A	DDR	Data A bit 0 Output (Pos)
DDC_DOUT_A1_DPN	AD1	O	LVDS_25	Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω)	-	DDC_DCLKOUT_A	DDR	Data A bit 1 Output (Neg)
DDC_DOUT_A1_DPP	AE1	O	LVDS_25_O		-	DDC_DCLKOUT_A	DDR	Data A bit 1 Output (Pos)

Pin Functions (continued)

PIN		TYPE	SIGNAL	TERMINATION /NOTES	ACTIVE (Hi or Lo)	CLOCK	DATA RATE	DESCRIPTION
NAME	NO.							
DDC_DOUT_A2_DPN	AC1	O	LVDS_25	Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω)	-	DDC_DCLKOUT_A	DDR	Data A bit 2 Output (Neg)
DDC_DOUT_A2_DPP	AC2	O	LVDS_25_O		-	DDC_DCLKOUT_A	DDR	Data A bit 2 Output (Pos)
DDC_DOUT_A3_DPN	AB1	O	LVDS_25	Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω)	-	DDC_DCLKOUT_A	DDR	Data A bit 3 Output (Neg)
DDC_DOUT_A3_DPP	AB2	O	LVDS_25_O		-	DDC_DCLKOUT_A	DDR	Data A bit 3 Output (Pos)
DDC_DOUT_A4_DPN	Y2	O	LVDS_25	Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω)	-	DDC_DCLKOUT_A	DDR	Data A bit 4 Output (Neg)
DDC_DOUT_A4_DPP	AA2	O	LVDS_25_O		-	DDC_DCLKOUT_A	DDR	Data A bit 4 Output (Pos)
DDC_DOUT_A5_DPN	W1	O	LVDS_25	Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω)	-	DDC_DCLKOUT_A	DDR	Data A bit 5 Output (Neg)
DDC_DOUT_A5_DPP	Y1	O	LVDS_25_O		-	DDC_DCLKOUT_A	DDR	Data A bit 5 Output (Pos)
DDC_DOUT_A6_DPN	V1	O	LVDS_25	Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω)	-	DDC_DCLKOUT_A	DDR	Data A bit 6 Output (Neg)
DDC_DOUT_A6_DPP	V2	O	LVDS_25_O		-	DDC_DCLKOUT_A	DDR	Data A bit 6 Output (Pos)
DDC_DOUT_A7_DPN	U1	O	LVDS_25	Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω)	-	DDC_DCLKOUT_A	DDR	Data A bit 7 Output (Neg)
DDC_DOUT_A7_DPP	U2	O	LVDS_25_O		-	DDC_DCLKOUT_A	DDR	Data A bit 7 Output (Pos)
DDC_DOUT_A8_DPN	R2	O	LVDS_25	Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω)	-	DDC_DCLKOUT_A	DDR	Data A bit 8 Output (Neg)
DDC_DOUT_A8_DPP	T2	O	LVDS_25_O		-	DDC_DCLKOUT_A	DDR	Data A bit 8 Output (Pos)
DDC_DOUT_A9_DPN	N2	O	LVDS_25	Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω)	-	DDC_DCLKOUT_A	DDR	Data A bit 9 Output (Neg)
DDC_DOUT_A9_DPP	M2	O	LVDS_25_O		-	DDC_DCLKOUT_A	DDR	Data A bit 9 Output (Pos)
DDC_DOUT_A10_DPN	K1	O	LVDS_25	Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω)	-	DDC_DCLKOUT_A	DDR	Data A bit 10 Output (Neg)
DDC_DOUT_A10_DPP	L2	O	LVDS_25_O		-	DDC_DCLKOUT_A	DDR	Data A bit 10 Output (Pos)
DDC_DOUT_A11_DPN	K2	O	LVDS_25	Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω)	-	DDC_DCLKOUT_A	DDR	Data A bit 11 Output (Neg)
DDC_DOUT_A11_DPP	K3	O	LVDS_25_O		-	DDC_DCLKOUT_A	DDR	Data A bit 11 Output (Pos)
DDC_DOUT_A12_DPN	J3	O	LVDS_25	Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω)	-	DDC_DCLKOUT_A	DDR	Data A bit 12 Output (Neg)
DDC_DOUT_A12_DPP	H3	O	LVDS_25_O		-	DDC_DCLKOUT_A	DDR	Data A bit 12 Output (Pos)
DDC_DOUT_A13_DPN	H2	O	LVDS_25	Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω)	-	DDC_DCLKOUT_A	DDR	Data A bit 13 Output (Neg)
DDC_DOUT_A13_DPP	J1	O	LVDS_25_O		-	DDC_DCLKOUT_A	DDR	Data A bit 13 Output (Pos)
DDC_DOUT_A14_DPN	H1	O	LVDS_25	Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω)	-	DDC_DCLKOUT_A	DDR	Data A bit 14 Output (Neg)
DDC_DOUT_A14_DPP	G1	O	LVDS_25_O		-	DDC_DCLKOUT_A	DDR	Data A bit 14 Output (Pos)
DDC_DOUT_A15_DPN	G2	O	LVDS_25	Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω)	-	DDC_DCLKOUT_A	DDR	Data A bit 15 Output (Neg)
DDC_DOUT_A15_DPP	F2	O	LVDS_25_O		-	DDC_DCLKOUT_A	DDR	Data A bit 15 Output (Pos)
DDC_DOUT_B0_DPN	AE5	O	LVDS_25	Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω)	-	DDC_DCLKOUT_B	DDR	Data B bit 0 Output (Neg)
DDC_DOUT_B0_DPP	AE6	O	LVDS_25_O		-	DDC_DCLKOUT_B	DDR	Data B bit 0 Output (Pos)
DDC_DOUT_B1_DPN	AD3	O	LVDS_25	Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω)	-	DDC_DCLKOUT_B	DDR	Data B bit 1 Output (Neg)
DDC_DOUT_B1_DPP	AD4	O	LVDS_25_O		-	DDC_DCLKOUT_B	DDR	Data B bit 1 Output (Pos)
DDC_DOUT_B2_DPN	AD5	O	LVDS_25	Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω)	-	DDC_DCLKOUT_B	DDR	Data B bit 2 Output (Neg)
DDC_DOUT_B2_DPP	AD6	O	LVDS_25_O		-	DDC_DCLKOUT_B	DDR	Data B bit 2 Output (Pos)
DDC_DOUT_B3_DPN	AC3	O	LVDS_25	Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω)	-	DDC_DCLKOUT_B	DDR	Data B bit 3 Output (Neg)
DDC_DOUT_B3_DPP	AC4	O	LVDS_25_O		-	DDC_DCLKOUT_B	DDR	Data B bit 3 Output (Pos)
DDC_DOUT_B4_DPN	AB5	O	LVDS_25	Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω)	-	DDC_DCLKOUT_B	DDR	Data B bit 4 Output (Neg)
DDC_DOUT_B4_DPP	AB6	O	LVDS_25_O		-	DDC_DCLKOUT_B	DDR	Data B bit 4 Output (Pos)
DDC_DOUT_B5_DPN	AB7	O	LVDS_25	Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω)	-	DDC_DCLKOUT_B	DDR	Data B bit 5 Output (Neg)
DDC_DOUT_B5_DPP	AC6	O	LVDS_25_O		-	DDC_DCLKOUT_B	DDR	Data B bit 5 Output (Pos)
DDC_DOUT_B6_DPN	AA5	O	LVDS_25	Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω)	-	DDC_DCLKOUT_B	DDR	Data B bit 6 Output (Neg)
DDC_DOUT_B6_DPP	AA4	O	LVDS_25_O		-	DDC_DCLKOUT_B	DDR	Data B bit 6 Output (Pos)
DDC_DOUT_B7_DPN	AA7	O	LVDS_25	Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω)	-	DDC_DCLKOUT_B	DDR	Data B bit 7 Output (Neg)
DDC_DOUT_B7_DPP	Y7	O	LVDS_25_O		-	DDC_DCLKOUT_B	DDR	Data B bit 7 Output (Pos)
DDC_DOUT_B8_DPN	Y3	O	LVDS_25	Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω)	-	DDC_DCLKOUT_B	DDR	Data B bit 8 Output (Neg)
DDC_DOUT_B8_DPP	W3	O	LVDS_25_O		-	DDC_DCLKOUT_B	DDR	Data B bit 8 Output (Pos)
DDC_DOUT_B9_DPN	W4	O	LVDS_25	Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω)	-	DDC_DCLKOUT_B	DDR	Data B bit 9 Output (Neg)
DDC_DOUT_B9_DPP	V4	O	LVDS_25_O		-	DDC_DCLKOUT_B	DDR	Data B bit 9 Output (Pos)

Pin Functions (continued)

PIN		TYPE	SIGNAL	TERMINATION /NOTES	ACTIVE (Hi or Lo)	CLOCK	DATA RATE	DESCRIPTION
NAME	NO.							
DDC_DOUT_B10_DPN	W6	O	LVDS_25	Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω)	-	DDC_DCLKOUT_B	DDR	Data B bit 10 Output (Neg)
DDC_DOUT_B10_DPP	W5	O	LVDS_25_O		-	DDC_DCLKOUT_B	DDR	Data B bit 10 Output (Pos)
DDC_DOUT_B11_DPN	V7	O	LVDS_25	Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω)	-	DDC_DCLKOUT_B	DDR	Data B bit 11 Output (Neg)
DDC_DOUT_B11_DPP	V6	O	LVDS_25_O		-	DDC_DCLKOUT_B	DDR	Data B bit 11 Output (Pos)
DDC_DOUT_B12_DPN	U4	O	LVDS_25	Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω)	-	DDC_DCLKOUT_B	DDR	Data B bit 12 Output (Neg)
DDC_DOUT_B12_DPP	V3	O	LVDS_25_O		-	DDC_DCLKOUT_B	DDR	Data B bit 12 Output (Pos)
DDC_DOUT_B13_DPN	T4	O	LVDS_25	Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω)	-	DDC_DCLKOUT_B	DDR	Data B bit 13 Output (Neg)
DDC_DOUT_B13_DPP	T5	O	LVDS_25_O		-	DDC_DCLKOUT_B	DDR	Data B bit 13 Output (Pos)
DDC_DOUT_B14_DPN	U6	O	LVDS_25	Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω)	-	DDC_DCLKOUT_B	DDR	Data B bit 14 Output (Neg)
DDC_DOUT_B14_DPP	U5	O	LVDS_25_O		-	DDC_DCLKOUT_B	DDR	Data B bit 14 Output (Pos)
DDC_DOUT_B15_DPN	U7	O	LVDS_25	Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω)	-	DDC_DCLKOUT_B	DDR	Data B bit 15 Output (Neg)
DDC_DOUT_B15_DPP	T7	O	LVDS_25_O		-	DDC_DCLKOUT_B	DDR	Data B bit 15 Output (Pos)
DDC_DOUT_C0_DPN	T22	O	LVDS_25	Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω)	-	DDC_DCLKOUT_C	DDR	Data C bit 0 Output (Neg)
DDC_DOUT_C0_DPP	T23	O	LVDS_25_O		-	DDC_DCLKOUT_C	DDR	Data C bit 0 Output (Pos)
DDC_DOUT_C1_DPN	R20	O	LVDS_25	Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω)	-	DDC_DCLKOUT_C	DDR	Data C bit 1 Output (Neg)
DDC_DOUT_C1_DPP	R21	O	LVDS_25_O		-	DDC_DCLKOUT_C	DDR	Data C bit 1 Output (Pos)
DDC_DOUT_C2_DPN	T19	O	LVDS_25	Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω)	-	DDC_DCLKOUT_C	DDR	Data C bit 2 Output (Neg)
DDC_DOUT_C2_DPP	T20	O	LVDS_25_O		-	DDC_DCLKOUT_C	DDR	Data C bit 2 Output (Pos)
DDC_DOUT_C3_DPN	U21	O	LVDS_25	Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω)	-	DDC_DCLKOUT_C	DDR	Data C bit 3 Output (Neg)
DDC_DOUT_C3_DPP	U22	O	LVDS_25_O		-	DDC_DCLKOUT_C	DDR	Data C bit 3 Output (Pos)
DDC_DOUT_C4_DPN	U20	O	LVDS_25	Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω)	-	DDC_DCLKOUT_C	DDR	Data C bit 4 Output (Neg)
DDC_DOUT_C4_DPP	U19	O	LVDS_25_O		-	DDC_DCLKOUT_C	DDR	Data C bit 4 Output (Pos)
DDC_DOUT_C5_DPN	V23	O	LVDS_25	Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω)	-	DDC_DCLKOUT_C	DDR	Data C bit 5 Output (Neg)
DDC_DOUT_C5_DPP	V24	O	LVDS_25_O		-	DDC_DCLKOUT_C	DDR	Data C bit 5 Output (Pos)
DDC_DOUT_C6_DPN	V22	O	LVDS_25	Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω)	-	DDC_DCLKOUT_C	DDR	Data C bit 6 Output (Neg)
DDC_DOUT_C6_DPP	V21	O	LVDS_25_O		-	DDC_DCLKOUT_C	DDR	Data C bit 6 Output (Pos)
DDC_DOUT_C7_DPN	W19	O	LVDS_25	Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω)	-	DDC_DCLKOUT_C	DDR	Data C bit 7 Output (Neg)
DDC_DOUT_C7_DPP	V19	O	LVDS_25_O		-	DDC_DCLKOUT_C	DDR	Data C bit 7 Output (Pos)
DDC_DOUT_C8_DPN	W23	O	LVDS_25	Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω)	-	DDC_DCLKOUT_C	DDR	Data C bit 8 Output (Neg)
DDC_DOUT_C8_DPP	W24	O	LVDS_25_O		-	DDC_DCLKOUT_C	DDR	Data C bit 8 Output (Pos)
DDC_DOUT_C9_DPN	Y22	O	LVDS_25	Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω)	-	DDC_DCLKOUT_C	DDR	Data C bit 9 Output (Neg)
DDC_DOUT_C9_DPP	Y23	O	LVDS_25_O		-	DDC_DCLKOUT_C	DDR	Data C bit 9 Output (Pos)
DDC_DOUT_C10_DPN	Y20	O	LVDS_25	Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω)	-	DDC_DCLKOUT_C	DDR	Data C bit 10 Output (Neg)
DDC_DOUT_C10_DPP	Y21	O	LVDS_25_O		-	DDC_DCLKOUT_C	DDR	Data C bit 10 Output (Pos)
DDC_DOUT_C11_DPN	AA24	O	LVDS_25	Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω)	-	DDC_DCLKOUT_C	DDR	Data C bit 11 Output (Neg)
DDC_DOUT_C11_DPP	AA23	O	LVDS_25_O		-	DDC_DCLKOUT_C	DDR	Data C bit 11 Output (Pos)
DDC_DOUT_C12_DPN	AA19	O	LVDS_25	Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω)	-	DDC_DCLKOUT_C	DDR	Data C bit 12 Output (Neg)
DDC_DOUT_C12_DPP	AA20	O	LVDS_25_O		-	DDC_DCLKOUT_C	DDR	Data C bit 12 Output (Pos)
DDC_DOUT_C13_DPN	AC24	O	LVDS_25	Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω)	-	DDC_DCLKOUT_C	DDR	Data C bit 13 Output (Neg)
DDC_DOUT_C13_DPP	AB24	O	LVDS_25_O		-	DDC_DCLKOUT_C	DDR	Data C bit 13 Output (Pos)
DDC_DOUT_C14_DPN	AC19	O	LVDS_25	Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω)	-	DDC_DCLKOUT_C	DDR	Data C bit 14 Output (Neg)
DDC_DOUT_C14_DPP	AD19	O	LVDS_25_O		-	DDC_DCLKOUT_C	DDR	Data C bit 14 Output (Pos)
DDC_DOUT_C15_DPN	AC22	O	LVDS_25	Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω)	-	DDC_DCLKOUT_C	DDR	Data C bit 15 Output (Neg)
DDC_DOUT_C15_DPP	AC23	O	LVDS_25_O		-	DDC_DCLKOUT_C	DDR	Data C bit 15 Output (Pos)
DDC_DOUT_D0_DPN	AB26	O	LVDS_25	Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω)	-	DDC_DCLKOUT_D	DDR	Data D bit 0 Output (Neg)
DDC_DOUT_D0_DPP	AC26	O	LVDS_25_O		-	DDC_DCLKOUT_D	DDR	Data D bit 0 Output (Pos)
DDC_DOUT_D1_DPN	AA25	O	LVDS_25	Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω)	-	DDC_DCLKOUT_D	DDR	Data D bit 1 Output (Neg)
DDC_DOUT_D1_DPP	AB25	O	LVDS_25_O		-	DDC_DCLKOUT_D	DDR	Data D bit 1 Output (Pos)

Pin Functions (continued)

PIN		TYPE	SIGNAL	TERMINATION /NOTES	ACTIVE (Hi or Lo)	CLOCK	DATA RATE	DESCRIPTION
NAME	NO.							
DDC_DOUT_D2_DPN	Y26	O	LVDS_25	Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω)	-	DDC_DCLKOUT_D	DDR	Data D bit 2 Output (Neg)
DDC_DOUT_D2_DPP	Y25	O	LVDS_25_O		-	DDC_DCLKOUT_D	DDR	Data D bit 2 Output (Pos)
DDC_DOUT_D3_DPN	W26	O	LVDS_25	Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω)	-	DDC_DCLKOUT_D	DDR	Data D bit 3 Output (Neg)
DDC_DOUT_D3_DPP	W25	O	LVDS_25_O		-	DDC_DCLKOUT_D	DDR	Data D bit 3 Output (Pos)
DDC_DOUT_D4_DPN	U26	O	LVDS_25	Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω)	-	DDC_DCLKOUT_D	DDR	Data D bit 4 Output (Neg)
DDC_DOUT_D4_DPP	V26	O	LVDS_25_O		-	DDC_DCLKOUT_D	DDR	Data D bit 4 Output (Pos)
DDC_DOUT_D5_DPN	U25	O	LVDS_25	Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω)	-	DDC_DCLKOUT_D	DDR	Data D bit 5 Output (Neg)
DDC_DOUT_D5_DPP	U24	O	LVDS_25_O		-	DDC_DCLKOUT_D	DDR	Data D bit 5 Output (Pos)
DDC_DOUT_D6_DPN	T25	O	LVDS_25	Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω)	-	DDC_DCLKOUT_D	DDR	Data D bit 6 Output (Neg)
DDC_DOUT_D6_DPP	T24	O	LVDS_25_O		-	DDC_DCLKOUT_D	DDR	Data D bit 6 Output (Pos)
DDC_DOUT_D7_DPN	R26	O	LVDS_25	Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω)	-	DDC_DCLKOUT_D	DDR	Data D bit 7 Output (Neg)
DDC_DOUT_D7_DPP	R25	O	LVDS_25_O		-	DDC_DCLKOUT_D	DDR	Data D bit 7 Output (Pos)
DDC_DOUT_D8_DPN	P24	O	LVDS_25	Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω)	-	DDC_DCLKOUT_D	DDR	Data D bit 8 Output (Neg)
DDC_DOUT_D8_DPP	P25	O	LVDS_25_O		-	DDC_DCLKOUT_D	DDR	Data D bit 8 Output (Pos)
DDC_DOUT_D9_DPN	N24	O	LVDS_25	Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω)	-	DDC_DCLKOUT_D	DDR	Data D bit 9 Output (Neg)
DDC_DOUT_D9_DPP	M24	O	LVDS_25_O		-	DDC_DCLKOUT_D	DDR	Data D bit 9 Output (Pos)
DDC_DOUT_D10_DPN	L25	O	LVDS_25	Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω)	-	DDC_DCLKOUT_D	DDR	Data D bit 10 Output (Neg)
DDC_DOUT_D10_DPP	L24	O	LVDS_25_O		-	DDC_DCLKOUT_D	DDR	Data D bit 10 Output (Pos)
DDC_DOUT_D11_DPN	K26	O	LVDS_25	Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω)	-	DDC_DCLKOUT_D	DDR	Data D bit 11 Output (Neg)
DDC_DOUT_D11_DPP	K25	O	LVDS_25_O		-	DDC_DCLKOUT_D	DDR	Data D bit 11 Output (Pos)
DDC_DOUT_D12_DPN	J26	O	LVDS_25	Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω)	-	DDC_DCLKOUT_D	DDR	Data D bit 12 Output (Neg)
DDC_DOUT_D12_DPP	J25	O	LVDS_25_O		-	DDC_DCLKOUT_D	DDR	Data D bit 12 Output (Pos)
DDC_DOUT_D13_DPN	J24	O	LVDS_25	Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω)	-	DDC_DCLKOUT_D	DDR	Data D bit 13 Output (Neg)
DDC_DOUT_D13_DPP	H24	O	LVDS_25_O		-	DDC_DCLKOUT_D	DDR	Data D bit 13 Output (Pos)
DDC_DOUT_D14_DPN	H26	O	LVDS_25	Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω)	-	DDC_DCLKOUT_D	DDR	Data D bit 14 Output (Neg)
DDC_DOUT_D14_DPP	G26	O	LVDS_25_O		-	DDC_DCLKOUT_D	DDR	Data D bit 14 Output (Pos)
DDC_DOUT_D15_DPN	G25	O	LVDS_25	Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω)	-	DDC_DCLKOUT_D	DDR	Data D bit 15 Output (Neg)
DDC_DOUT_D15_DPP	G24	O	LVDS_25_O		-	DDC_DCLKOUT_D	DDR	Data D bit 15 Output (Pos)
DDC_M0	W18	-	NC	4.7 kΩ pullup to 2.5V	Hi	-		Xilinx Configuration
DDC_M1	Y17	-	NC	4.7 kΩ pullup to 2.5V	Hi	-		Xilinx Configuration
DDC_M2	V18	-	NC	4.7 kΩ pullup to 2.5V	Hi	-		Xilinx Configuration
DDC_SCTRL_AN	R1	O	LVDS_25	Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω)	-	DDC_DCLKOUT_A	DDR	Bank A Serial Control Data (Neg)
DDC_SCTRL_AP	P1	O	LVDS_25_O		-	DDC_DCLKOUT_A	DDR	Bank A Serial Control Data (Pos)
DDC_SCTRL_BN	AA3	O	LVDS_25	Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω)	-	DDC_DCLKOUT_B	DDR	Bank B Serial Control Data (Neg)
DDC_SCTRL_BP	AB4	O	LVDS_25_O		-	DDC_DCLKOUT_B	DDR	Bank B Serial Control Data (Pos)
DDC_SCTRL_CN	W20	O	LVDS_25	Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω)	-	DDC_DCLKOUT_C	DDR	Bank C Serial Control Data (Neg)
DDC_SCTRL_CP	W21	O	LVDS_25_O		-	DDC_DCLKOUT_C	DDR	Bank C Serial Control Data (Pos)
DDC_SCTRL_DN	N26	O	LVDS_25	Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω)	-	DDC_DCLKOUT_D	DDR	Bank D Serial Control Data (Neg)
DDC_SCTRL_DP	P26	O	LVDS_25_O		-	DDC_DCLKOUT_D	DDR	Bank D Serial Control Data (Pos)
DDC_VERSION_0	F18	O	LVCMOS25_F_12_O		Hi = 1	-		DLPC410 Firmware Rev Number bit 0
DDC_VERSION_1	G17	O	LVCMOS25_F_12_O		Hi = 1	-		DLPC410 Firmware Rev Number bit 1
DDC_VERSION_2	H18	O	LVCMOS25_F_12_O		Hi = 1	-		DLPC410 Firmware Rev Number bit 2

Pin Functions (continued)

PIN		TYPE	SIGNAL	TERMINATION /NOTES	ACTIVE (Hi or Lo)	CLOCK	DATA RATE	DESCRIPTION
NAME	NO.							
DDC_SPARE_0	AB21	-	LVCMOS25_F_12_I/O	Do not connect	-	-		Not Used
DDC_SPARE_1	AC21	-	LVCMOS25_F_12_O		-	-		Not Used
DMD_A_RESET	AD14	O	LVCMOS25_F_12_O	Connected in Reference Design to 36 Ω resistor with 27 pF cap to ground (signal name DMD_A_RESET_FILT after resisitor - connects to DMD signal $\overline{\text{DMDRST}}$)	Lo	-		DMD Circuitry Reset (not data reset)
$\overline{\text{DMD_A_SCPEN}}$	AB14	O	LVCMOS25_F_12_O	Connected in Reference Design to 36 Ω resistor with 27 pF cap to ground (called DMD_A_SCPEN# in Reference Design- signal name DMD_A_SCPEN#_FILT after resisitor - connects to DMD signal $\overline{\text{DMDSEL}}$)	Lo	-		DMD SCP Output Enable
DMD_B_RESET	AA12	O	LVCMOS25_S_12_O	Connected in Reference Design to 36 Ω resistor with 27 pF cap to ground (signal name DMD_B_RESET_FILT after resisitor - NC after that point)	-	-		Not Used
$\overline{\text{DMD_B_SCPEN}}$	AC14	O	LVCMOS25_S_12_O	Connected in Reference Design to 36 Ω resistor with 27 pF cap to ground (called DMD_B_SCPEN# in Reference Design - signal name DMD_B_SCPEN#_FILT after resisitor - NC after that point)	-	-		Not Used
DMD_TYPE_0	AA17	O	LVCMOS25_F_12_O		Hi = 1	-		DMD Attached Type bit 0
DMD_TYPE_1	AC16	O	LVCMOS25_F_12_O		Hi = 1	-		DMD Attached Type bit 1
DMD_TYPE_2	AB17	O	LVCMOS25_F_12_O		Hi = 1	-		DMD Attached Type bit 2
DMD_TYPE_3	AD15	O	LVCMOS25_F_12_O		Hi = 1	-		DMD Attached Type bit 3
DONE_DDC	K10	O	-	4.7 kΩ pullup to 2.5V - connected to DLPR410 $\overline{\text{CE}}$ pin and LED D3 pin 3 (cathode) in series with 62 Ω resistor to 3.3 V	Hi	-		DLPR410 Initialization Routine Complete
DVALID_A_DPN	D20	I	LVDS_25	100 Ω across pair (not terminated in the DLPC410)	-	DDC_DCLK_A		Bank A Valid Input Signal (Neg)
DVALID_A_DPP	D21	I	LVDS_25_I		-	DDC_DCLK_A		Bank A Valid Input Signal (Pos)
DVALID_B_DPN	C8	I	LVDS_25	100 Ω across pair (not terminated in the DLPC410)	-	DDC_DCLK_B		Bank B Valid Input Signal (Neg)
DVALID_B_DPP	D8	I	LVDS_25_I		-	DDC_DCLK_B		Bank B Valid Input Signal (Pos)
DVALID_C_DPN	L19	I	LVDS_25	100 Ω across pair (not terminated in the DLPC410)	-	DDC_DCLK_C		Bank C Valid Input Signal (Neg)
DVALID_C_DPP	L20	I	LVDS_25_I		-	DDC_DCLK_C		Bank C Valid Input Signal (Pos)
DVALID_D_DPN	L3	I	LVDS_25	100 Ω across pair (not terminated in the DLPC410)	-	DDC_DCLK_D		Bank D Valid Input Signal (Neg)
DVALID_D_DPP	L4	I	LVDS_25_I		-	DDC_DCLK_D		Bank D Valid Input Signal (Pos)
DXN_0	R13	-	NC	TP17 in Reference Design	-	-		Dedicated Xilinx Temperature Diode (anode); Not Used in Reference Design
DXP_0	R14	-	NC	TP14 in Reference Design	-	-		Dedicated Xilinx Temperature Diode (cathode); Not Used in Reference Design
ECP2_FINISHED	Y18	O	LVCMOS25_F_12_O	Connected to LED D3 pin 2 (anode) in series with 62 Ω resistor to 3.3 V	Hi	-		DLPR410 Initialization Routine Complete
ECP2_M_TP0	AD11	-	LVCMOS25_F_12_O	Mictor J8 Pin 2 in Reference Design	-	-		Not Used - do not connect

Pin Functions (continued)

PIN		TYPE	SIGNAL	TERMINATION /NOTES	ACTIVE (Hi or Lo)	CLOCK	DATA RATE	DESCRIPTION
NAME	NO.							
ECP2_M_TP1	AD10	-	LVCMOS25_F_12_O	Mictor J8 Pin 4 in Reference Design	-	-		Not Used - do not connect
ECP2_M_TP2	AD8	-	LVCMOS25_F_12_O	Mictor J8 Pin 6 in Reference Design	-	-		Not Used - do not connect
ECP2_M_TP3	AC8	O	LVCMOS25_F_12_O	Mictor J8 Pin 8 in Reference Design	-	-		Buffered data clock - test point
ECP2_M_TP4	AC7	O	LVCMOS25_F_12_O	Mictor J8 Pin 10 in Reference Design	-	-		System clock - test point
ECP2_M_TP5	AC9	O	LVCMOS25_F_12_O	Mictor J8 Pin 12 in Reference Design	Hi			DVALID A - test point
ECP2_M_TP6	AB9	O	LVCMOS25_F_12_O	Mictor J8 Pin 14 in Reference Design	Hi			DVALID B - test point
ECP2_M_TP7	AA8	O	LVCMOS25_F_12_O	Mictor J8 Pin 16 in Reference Design	Hi			DVALID C - test point
ECP2_M_TP8	AA9	O	LVCMOS25_F_12_O	Mictor J8 Pin 18 in Reference Design	Hi			DVALID D - test point
ECP2_M_TP9	Y8	O	LVCMOS25_F_12_O	Mictor J8 Pin 20 in Reference Design	-	-		Not Used - do not connect
ECP2_M_TP10	AB10	O	LVCMOS25_F_12_O	Mictor J8 Pin 22 in Reference Design	Lo			$\overline{\text{ARST}}$ (DLPC410 reset) - test point
ECP2_M_TP11	AA10	O	LVCMOS25_F_12_O	Mictor J8 Pin 24 in Reference Design	Hi			DMD A/B bus OK - test point
ECP2_M_TP12	Y10	O	LVCMOS25_F_12_O	Mictor J8 Pin 26 in Reference Design	Hi			DMD C/D bus OK - test point
ECP2_M_TP13	AC11	O	LVCMOS25_F_12_O	Mictor J8 Pin 28 in Reference Design	Hi			System PLL locked - test point
ECP2_M_TP14	Y12	O	LVCMOS25_F_12_O	Mictor J8 Pin 30 in Reference Design	Hi			Reference PLL locked - test point
ECP2_M_TP15	Y11	O	LVCMOS25_F_12_O	Mictor J8 Pin 32 in Reference Design	-			System clock - test point
ECP2_M_TP16	AB11	O	LVCMOS25_F_12_O	Mictor J8 Pin 34 in Reference Design	Hi			Clock reset - test point
ECP2_M_TP17	H8	O	LVCMOS25_F_12_O	Mictor J8 Pin 36 in Reference Design	Hi			System PLL reset - test point
ECP2_M_TP18	H9	O	LVCMOS25_F_12_O	Mictor J8 Pin 38 in Reference Design	Hi			Reference PLL reset - test point
ECP2_M_TP19	F12	O	LVCMOS25_F_12_O	Mictor J8 Pin 37 in Reference Design	-	-		Not Used - do not connect
ECP2_M_TP20	G11	O	LVCMOS25_F_12_O	Mictor J8 Pin 35 in Reference Design	Hi			System initialization in progress - test point
ECP2_M_TP21	G12	O	LVCMOS25_F_12_O	Mictor J8 Pin 33 in Reference Design	Hi			Bus A calibration done - test point
ECP2_M_TP22	E11	O	LVCMOS25_F_12_O	Mictor J8 Pin 31 in Reference Design	Hi			Bus B calibration done - test point
ECP2_M_TP23	E10	O	LVCMOS25_F_12_O	Mictor J8 Pin 29 in Reference Design	Hi			Bus C calibration done - test point
ECP2_M_TP24	E8	O	LVCMOS25_F_12_O	Mictor J8 Pin 27 in Reference Design	Hi			Bus D calibration done - test point
ECP2_M_TP25	F10	O	LVCMOS25_F_12_O	Mictor J8 Pin 25 in Reference Design	Hi			Not Used - do not connect
ECP2_M_TP26	F9	O	LVCMOS25_F_12_O	Mictor J8 Pin 23 in Reference Design	Hi			DMD initialization in progress - test point
ECP2_M_TP27	F8	O	LVCMOS25_F_12_O	Mictor J8 Pin 21 in Reference Design	Hi			DLPA200 Number 1 initialization in progress - test point
ECP2_M_TP28	G10	O	LVCMOS25_F_12_O	Mictor J8 Pin 19 in Reference Design	Hi			DLPA200 Number 2 initialization in progress - test point
ECP2_M_TP29	G9	O	LVCMOS25_F_12_O	Mictor J8 Pin 17 in Reference Design	Hi			System Calibration in progress - test point
ECP2_M_TP30	H11	O	LVCMOS25_F_12_O	Mictor J8 Pin 15 in Reference Design	-	-		Not Used - do not connect
ECP2_M_TP31	H12	O	LVCMOS25_F_12_O	Mictor J8 Pin 13 in Reference Design	-	-		Not Used - do not connect

Pin Functions (continued)

PIN		TYPE	SIGNAL	TERMINATION /NOTES	ACTIVE (Hi or Lo)	CLOCK	DATA RATE	DESCRIPTION
NAME	NO.							
GND	A1, A6, A11, A16, A21, A26, AA1, AA11, AA21, AA26, AB8, AB18, AC5, AC15, AC25, AD2, AD12, AD22, AE4, AE9, AE14, AE19, AF1, AF6, AF11, AF16, AF21, AF26, B3, B8, B13, B18, C5, C15, C25, D2, D12, D22, E9, E19, F1, F6, F16, F26, G3, G13, G18, G23, H10, H20, J7, J9, J13, J15, J17, K4, K8, K12, K14, K16, K19, K24, L1, L9, L11, L13, L15, L17, L21, L26, M3, M8, M10, M12, M16, M18, N5, N9, N11, N15, N17, N25, P2, P7, P8, P10, P12, P16, P22, R9, R11, R15, R17, R19, T1, T6, T8, T10, T12, T14, T16, T26, U3, U9, U13, U15, U17, U18, U23, V8, V10, V14, V16, V20, W7, W9, W13, W15, W17, Y4, Y14, Y16, Y19, Y24	-	GND		-	-		Connect to Ground
HSWAPEN	L18	-	-	4.7 kΩ pullup to 2.5 V	-	-		Xilinx Configuration
INIT_ACTIVE	AA18	O	LVCMOS25_F_12_O		Hi	-		DLPC410 Initilization Routine Active
INTB_DDC	J11	-	-	4.7 kΩ pullup to 2.5 V connected to DLPR410 OE/$\overline{\text{RESET}}$	Hi	-		Xilinx Configuration
NS_FLIP	F19	I	LVCMOS25_S_12_I		Hi	-		Top/Bottom image flip on DMD
PROGB_DDC	J18		-	4.7 kΩ pullup to 2.5 V connected to DLPR410 $\overline{\text{CF}}$	Hi	-		Xilinx Configuration
PROM_CCK_DDC	J10	I	LVCMOS25_S_12	Connected to center of voltage divider (100/100 Ω) and through R53 to DLPR410 CLKOUT	-	PROM_CCK_DDC		Configuration PROM Clock
PROM_D0_DDC	K11	-	-	Connected to DLPR410 Data 0 (D0)	-	PROM_CCK_DDC		Configuration PROM Data Out
PWR_FLOAT	AC17	I	LVCMOS25_S_12_I	Connected to output of U22 NOR Gate (inputs $\overline{\text{V5\_PWR\_FLOAT}}$ and PWRGD)	Hi	-		DMD Power Good indicator
RDWR_B	P18	-	-	1 kΩ pulldown to ground	-	-		Xilinx Configuration
ROWAD_0	D14	I	LVCMOS25_S_12_I		Hi = 1	-		DMD Row Address bit 0
ROWAD_1	D15	I	LVCMOS25_S_12_I		Hi = 1	-		DMD Row Address bit 1
ROWAD_2	E15	I	LVCMOS25_S_12_I		Hi = 1	-		DMD Row Address bit 2
ROWAD_3	F14	I	LVCMOS25_S_12_I		Hi = 1	-		DMD Row Address bit 3
ROWAD_4	G14	I	LVCMOS25_S_12_I		Hi = 1	-		DMD Row Address bit 4
ROWAD_5	E16	I	LVCMOS25_S_12_I		Hi = 1	-		DMD Row Address bit 5

Pin Functions (continued)

PIN		TYPE	SIGNAL	TERMINATION /NOTES	ACTIVE (Hi or Lo)	CLOCK	DATA RATE	DESCRIPTION
NAME	NO.							
ROWAD_6	F15	I	LVCMOS25_S_12_I		Hi = 1	-		DMD Row Address bit 6
ROWAD_7	G15	I	LVCMOS25_S_12_I		Hi = 1	-		DMD Row Address bit 7
ROWAD_8	E17	I	LVCMOS25_S_12_I		Hi = 1	-		DMD Row Address bit 8
ROWAD_9	F17	I	LVCMOS25_S_12_I		Hi = 1	-		DMD Row Address bit 9
ROWAD_10	G16	I	LVCMOS25_S_12_I		Hi = 1	-		DMD Row Address bit 10
ROWMD_0	H17	I	LVCMOS25_S_12_I		Hi = 1	-		DMD Row Mode bit 0
ROWMD_1	H16	I	LVCMOS25_S_12_I		Hi = 1	-		DMD Row Mode bit 1
RST_ACTIVE	AB16	I	LVCMOS25_F_12_O		Hi = 1	-		DMD Reset in Progress
$\overline{\text{RST2BLK}}$	E18	I	LVCMOS25_S_12_I		Hi = 1	-		Dual Block Reset bit
RSVD_0	R18	-	-	Connect to Ground	-	-		Not Used - must be tied to Ground
RSVD_1	T18	-	-	Connect to Ground	-	-		Not Used - must be tied to Ground
SCPCLK	AB15		LVCMOS25_F_12_O	Connected to DLPA200 Number 1 and Number 2 SCPCLK and to R105 36 Ω filter resistor with 27 pF cap after - called DMD_A_SCPCLK_FILT after - connects to DMD SCPCLK (also connects to R97 filter resistor with 27 pF cap after - called DMD_B_SCPCLK_FILT but NC after)	-	SCPCLK		SCP Clock
SCPDI	AA15	I	LVCMOS25_S_12_I	1 kΩ pullup to 2.5 V - connects to DLPA200 Number 1 and Number 2 SCPDO and to DMD SCPDO through flex A - on DMD board there is an LCR filter [2 x 100 pF caps, inductor and 34 Ω resistor] also connects to flex B but NC on other end.	-	SCPCLK		SCP data input to DLPC410
SCPDO	AA14	O	LVCMOS25_F_12_O	1 kΩ pullup to 2.5 V - connects to DLPA200 Number 1 and Number 2 SCPDI and to R96 filter cap with 27 pF cap after - called DMD_A_FILTER - connect through flex A to DMD SCPDI - also connects to R71 36 Ω filter resistor with 27 pF cap to DMD_B_SCPDO_FILT but NC on other end.	-	SCPCLK		SCP data output from DLPC410
STEPVCC	Y13	-	LVCMOS25_S_12_I	1 kΩ pulldown to ground	-	-		Not Used
TCK_JTAG	U11		-	Connects to DLPC410, DLPR410, and JTAG header TCK (if user has JTAG they must build their chain accordingly)	-	TCK_JTAG		JTAG Clock
TDO_DDC	W10		-	Connects to JTAG return TDO on JTAG header	-	TCK_JTAG		JTAG data out of DLPC410
TDO_XCF16DDC	V11		-	Connects to DLPR410 TDO (DLPC410 internal signal TDI_0)	-	TCK_JTAG		JTAG data out of DLPR410 to DLPC410
TMS_JTAG	V12		-	Connects to DLPC410, DLPR410, and JTAG header TMS	Hi	TCK_JTAG		JTAG
VBATT_0	K18		-	Connecteto 4.7 kΩ pullup to 2.5 V	-	-		Not Used

Pin Functions (continued)

PIN		TYPE	SIGNAL	TERMINATION /NOTES	ACTIVE (Hi or Lo)	CLOCK	DATA RATE	DESCRIPTION
NAME	NO.							
VCCAUX	J8, K17, L8, M17, N8, P17, R8, T17, U8, V17, W8, W16		POWER	VCC_2P5V	-	-		Aux Power
VCCINT	H15, J12, J14, J16, K9, K13, K15, L10, L12, L14, L16, M9, M11, M15, N10, N12, N16, P9, P11, P15, R10, R12, R16, T9, T11, T13, T15, U10, U12, U14, U16, V9, V13, V15, W14, Y15		POWER	VCC_1P0V	-	-		Power
VCCO_0_1	Y9		POWER	VCC_2P5V	-	-		Power
VCCO_0_2	W12		POWER		-	-		Power
VCCO_1_1	C10		POWER		-	-		Power
VCCO_1_2	F11		POWER		-	-		Power
VCCO_2_1	AA16		POWER		-	-		Power
VCCO_2_2	AD17		POWER		-	-		Power
VCCO_3_1	E14		POWER		-	-		Power
VCCO_3_2	D17		POWER		-	-		Power
VCCO_4_1	AC10		POWER		-	-		Power
VCCO_4_2	AB13		POWER		-	-		Power
VCCO_11_1	F21		POWER		-	-		Power
VCCO_11_2	J22		POWER		-	-		Power
VCCO_11_3	H25		POWER		-	-		Power
VCCO_12_1	J2		POWER		-	-		Power
VCCO_12_2	H5		POWER		-	-		Power
VCCO_12_3	L6		POWER		-	-		Power
VCCO_13_1	R24		POWER		-	-		Power
VCCO_13_2	M23		POWER		-	-		Power
VCCO_13_3	N20		POWER		-	-		Power
VCCO_14_1	V5		POWER		-	-		Power
VCCO_14_2	R4		POWER		-	-		Power
VCCO_14_3	W2		POWER		-	-		Power
VCCO_15_1	E24		POWER		-	-		Power
VCCO_15_2	B23		POWER		-	-		Power
VCCO_15_3	C20		POWER		-	-		Power
VCCO_16_1	G8		POWER		-	-		Power
VCCO_16_2	D7		POWER		-	-		Power
VCCO_16_3	E4		POWER		-	-		Power
VCCO_17_1	V25		POWER		-	-		Power
VCCO_17_2	W22		POWER		-	-		Power
VCCO_17_3	T21		POWER		-	-		Power
VCCO_18_1	AD7		POWER		-	-		Power
VCCO_18_2	AA6		POWER		-	-		Power
VCCO_18_3	AB3		POWER	VCC_2P5V	-	-		Power
VLED0	AC18	O	LVCMOS25_F_12_O	Connects to LED D9 in series with 22.1 Ω resistor to 2.5 V	Hi = On	-		Power Indicator LED Output
VLED1	AD18	O	LVCMOS25_F_12_O	Connects to LED D10 in series with 22.1 Ω resistor to 2.5 V	Hi = On	-		Heartbeat Indicator LED Output
VN_0	P13	-	-	Connect to Ground	-	-		Xilinx System Monitor (not used - must be connected to ground)
VP_0	N14	-	-	Connect to Ground	-	-		Xilinx System Monitor (not used - must be connected to ground)

Pin Functions (continued)

PIN		TYPE	SIGNAL	TERMINATION /NOTES	ACTIVE (Hi or Lo)	CLOCK	DATA RATE	DESCRIPTION
NAME	NO.							
VREFN_0	N13	-	LVCMOS25_S_12	Connect to Ground	-	-		Xilinx System Monitor reference voltage (not used - must be connected to ground)
VREFP_0	P14	-	LVCMOS25_S_12	Connect to Ground	-	-		Xilinx System Monitor reference ground (not used - must be connected to ground)
$\overline{\text{WDT\_ENBL}}$	AA13	I	LVCMOS25_S_12_I		Lo	-		DMD Mirror Clocking Pulse Watchdog Timer Enable
UNUSED	AB23, AC20, AD9, AD16, AD20, AD21, AD23, AD24, AD25, AD26, AE7, AE8, AE10, AE11, AE12, AE13, AE15, AE16, AE17, AE18, AE20, AE21, AE22, AE23, AE24, AE25, AE26, AF7, AF8, AF9, AF10, AF12, AF13, AF14, AF15, AF17, AF18, AF19, AF20, AF22, AF23, AF24, AF25		NC	No Connection (listed as Xilinx NC0 - NC42)	-	-		Unused Pins

8 Specifications

NOTE

The information contained in the following sections has been adapted from the Xilinx XC5VLX30 data sheet. For any information beyond what is listed here, consult the Xilinx XC5VLX30 data sheet. Where appropriate, DLPC410 specific values have been substituted in place of generic parameters.

8.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
ELECTRICAL					
	Supply voltage (2)	V_{CCINT}	–0.50	1.05	V
		V_{CCO}	–0.50	3.45	V
		V_{CCAUX}	2.35	2.625	V
V_I	Input voltage (3)	2.5 V	–0.75	V_{CCO} + 0.50	V
V_O	Output voltage(4)	2.5 V	–0.30	V_{CCO} + 0.30	V
ENVIRONMENTAL					
T_A	Operating free-air temperature(5)		0	85	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to GND.
(3) Applies to external input and bidirectional buffers.
(4) Applies to external output and bidirectional buffers.
(5) Maximum Ambient Temperature may be further limited by the device's power dissipation (which is data and configuration dependent), air flow and resultant junction temperature.

8.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	400	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

8.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CCINT}	1-V Supply voltage, core logic		0.95	1.00	1.05	V
V_{CCO}	2.5-V Supply voltage, I/O		1.14	2.50	3.45	V
V_{CCAUX}	2.5-V Supply voltage, I/O		2.375	2.500	2.625	V
V_I	Input voltage	2.5-V CMOS	0		V_{CCO}	V
		2.5-V LVDS	0.3		2.2	
V_O	Output voltage	2.5-V CMOS	0		V_{CCO}	V
		2.5-V LVDS	0.825		1.675	
T_J	Operating junction temperature(1)		0		125	°C
P_D	Continuous total power dissipation			2.7	2.8	W

(1) Thermal analysis and design should be carefully considered to ensure that the junction temperature is maintained within the above specifications.

8.4 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High-level Input voltage	2.5-V CMOS	1.7			V
V_{IL}	Low-level Input voltage	2.5-V CMOS			0.7	V
V_{OH}	High-level output voltage	2.5-V Interface	V_{CCO}-.4			V
		2.5-V LVDS		1.38		
V_{OL}	Low-level output voltage	2.5-V Interface			0.4	V
		2.5-V LVDS		1.03		
C_I	Input capacitance	2.5-V Interface		8		pF
		2.5-V LVDS		8		
I_{CCINT}	Supply voltage range, core supply			300		mA
I_{CCO}	Supply voltage range, I/O supply			850		mA

8.5 Timing Requirements

(see (1))

			MIN	NOM	MAX	UNIT
f_{cd}	Clock frequency, DCLKIN_n (2)		200		400	MHz
f_{cr}	Clock frequency, CLK_R			50		MHz
t_c	Cycle time, DCLKIN_n		2.5		5	ns
$t_{w(H)}$	Pulse duration, high	50% to 50% reference points (signal)	1.25		2.5	ns
$t_{w(L)}$	Pulse duration, low	50% to 50% reference points (signal)	1.25		2.5	ns
t_t	Transition time, $t_t = t_f / t_r$	20% to 80% reference points (signal)			.6	ns
t_{jp}	Period Jitter DCLKIN_n (3)			150		ps
t_{SK}	Skew, DIN_A(15-0) to DCLKIN_A		–150		150	ps
	Skew, DIN_B(15-0) to DCLKIN_B		–150		150	
	Skew, DIN_C(15-0) to DCLKIN_C		–150		150	
	Skew, DIN_D(15-0) to DCLKIN_D		–150		150	
	Skew, DVALID_n to DCLKIN_n↑		–150		150	
	Skew, BLK_MD BLK_AD to DCLKIN_n↑ (4)		–150		150	
	Skew, ROWMD or ROWAD to DCLKIN_n↑ (4)		–150		150	
	Skew, STEPVCC to DCLKIN↑ (4)		–150		150	

(1) It is recommended that the COMP_DATA, NS_FLIP and $\overline{\text{RST2BLK}}$ flags be set to one value and not adjusted during normal system operation.
(2) Preferred DCLKIN_n duty cycle = 50%
(3) This is the deviation in period from ideal period due solely to high frequency jitter.
(4) First edge of DIN*, ROW*, BLK* and STEPVCC should be synchronous to DVALID rising edge

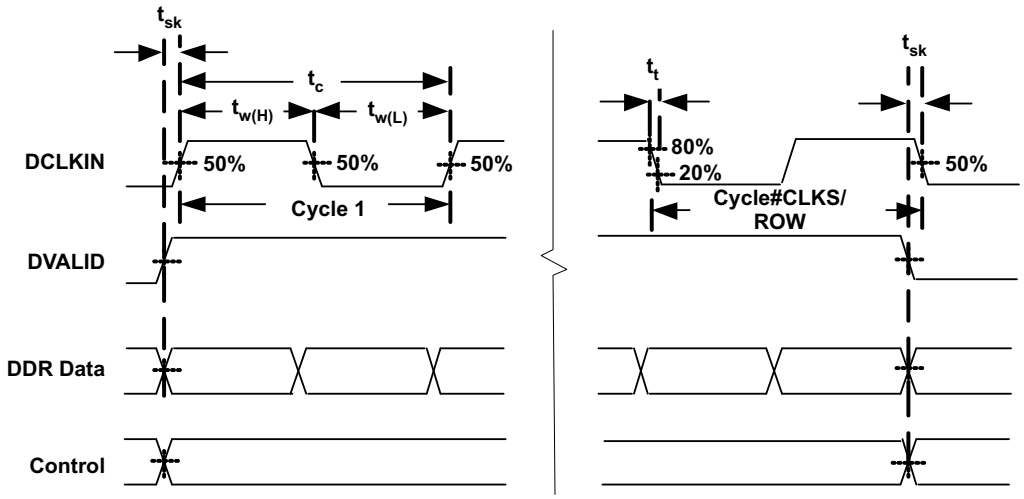


Figure 2. Input Interface Timing

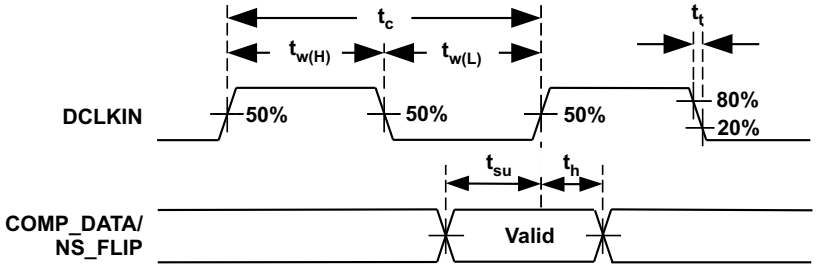


Figure 3. Control Timing

NOTE

Dynamic changes to NS_FLIP and COMP_DATA during normal operation is not recommended.

9 Detailed Description

9.1 Overview

The DLPC410 controller processes digital input binary data and converts the data into the digital format needed by the DLP7000 / DLP7000UV or the DLP9500 / DLP9500UV. For further details, refer to the DLP7000 / DLP7000UV or the DLP9500 / DLP9500UV data sheets.

The DLPC410 combined with a DLP7000 / DLP7000UV provides a native XGA resolution (1024 x 768) binary pattern resolution.

The DLPC410 combined with a DLP9500 / DLP9500UV provides a native 1080p resolution (1920 x 1080) binary pattern resolution.

9.2 Functional Block Diagrams

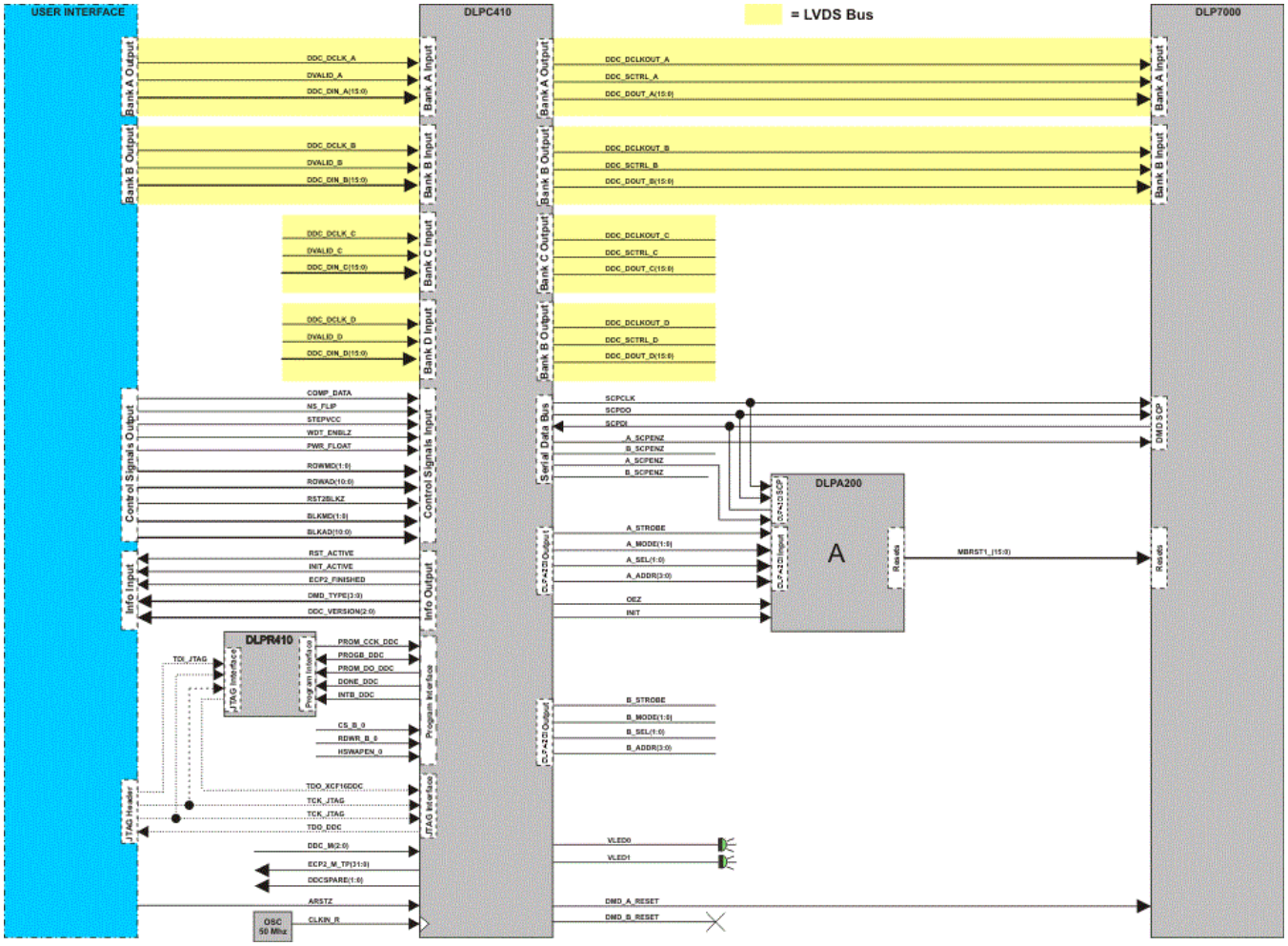


Figure 4. DLPC410 and DLP7000 / DLP7000UV Functional Block Diagram

Functional Block Diagrams (continued)

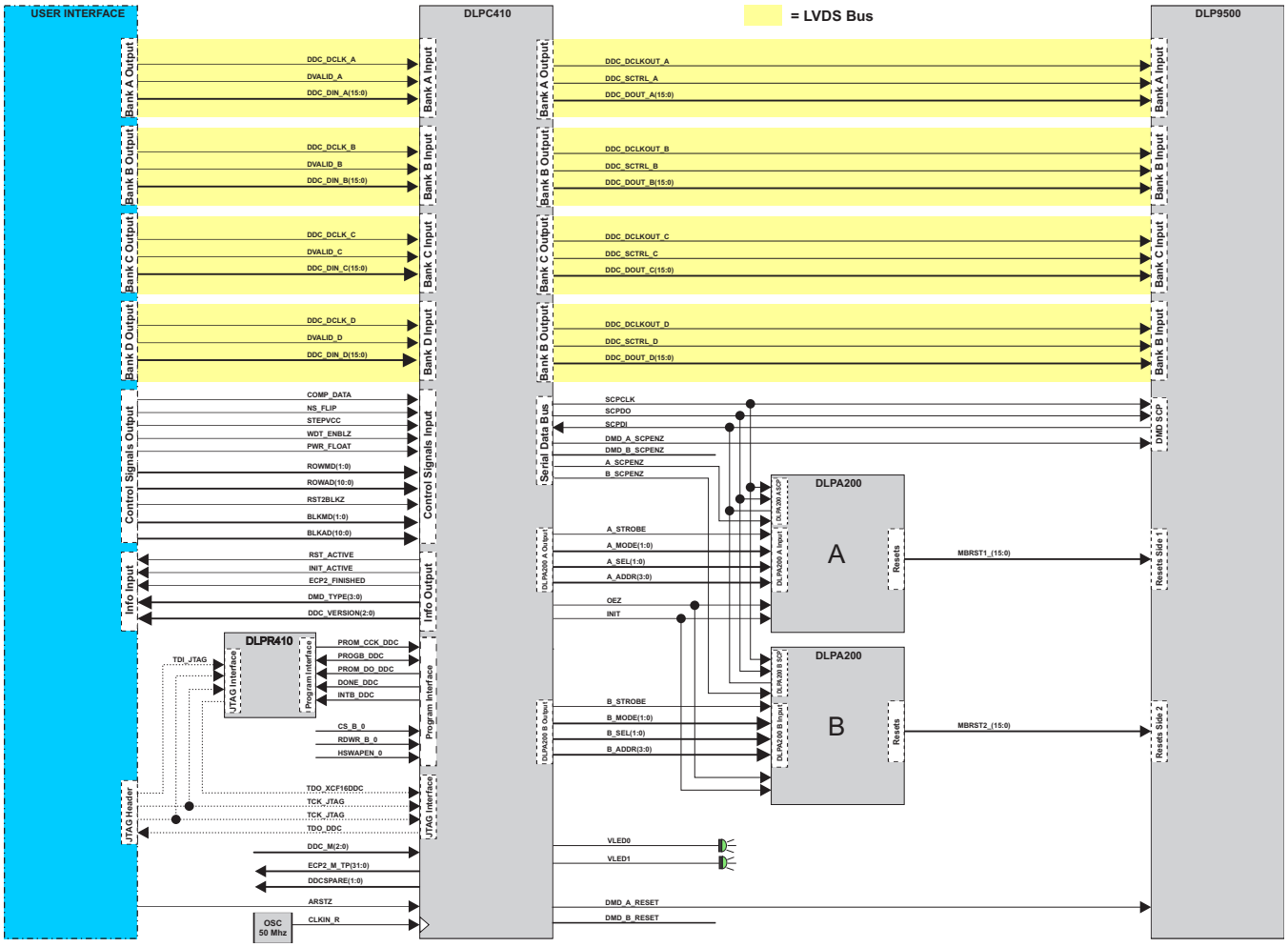


Figure 5. DLPC410 and DLP9500 / DLP9500UV Functional Block Diagram

9.3 Feature Description

9.3.1 DLPC410 Control Interface

9.3.1.1 Clocks and Reset Inputs

9.3.1.1.1 $\overline{\text{ARST}}$

$\overline{\text{ARST}}$ is an active low, asynchronous reset. This reset can be sourced from a voltage supervisor or from the customer interface. Be aware that the chipset will not operate correctly if all DLPC410 power supplies are not in range at the time this reset is released.

9.3.1.1.2 CLKIN_R

The reference clock, CLKIN_R, supplied from an oscillator must be 50 MHz. This is required for precise timing used to perform the DMD Mirror Clocking Pulse (Reset). This clock should be valid prior to releasing $\overline{\text{ARST}}$.

Feature Description (continued)

9.3.1.1.3 DDC_DCLKIN_[A, B, C, D]

The data clock, DDC_DCLKIN, must operate continuously. All signals associated with the data clock should be synchronous to these signals. For example, DDC_DIN_* and DVALID should be synchronous to the rising edge of DDC_DCLKIN. This clock should be valid prior to releasing ARST. DDC_DCLKIN is a DDR clock with data loaded on both rising and falling edges of DDC_DCLKIN. The jitter on this clock should be minimal.

9.3.1.2 Control Inputs

The DLPC410 supports two 2XLVDS DMD types as shown in Table 2.

Table 2. DMD Characteristics

TYPE	DMD_TYPE	COLUMNS	ROWS	BLOCKS	ROWS PER BLOCK	CLOCKS PER ROW	NO. OF DATA LINES
DLP7000 / DLP7000UV - 0.7 XGA Type A	0001	1024	768	16	48	16	32
DLP9500 / DLP9500UV - 0.95 1080p Type A	0000	1920	1080	15	72	16	64

NOTE

The DLP9500 / DLP9500UV DMD is loaded as 15 blocks of 72 rows each. The first 64 bits of pixel data and last 64 bits of pixel data for all rows are not visible.

9.3.1.3 System Initialization Signals

The INIT_ACTIVE signal indicates that the DMD, Digital Micromirror Driver, and the Digital Controller are in an initialization state after power is applied. During this initialization period, the DLPC410 is calibrating the data interface, initializing the DMD, and DLPA200(s). When this signal goes low, the system has completed initialization. System initialization takes approximately 220 ms to complete. Data and command write cycles must not be asserted during the initialization. This signal is driven by a CLK_R register and should be considered an asynchronous signal. Standard synchronization techniques should be applied if monitoring this signal with a synchronous circuit clocked by a clock other than CLK_R. After initialization is complete, a delay of at least 64 clocks should be observed before the first DVALID is asserted (to ensure a clean start up process).

Note: The NS_FLIP, COMP_DATA, and $\overline{\text{RST2BLK}}$ signals should be kept low during initialization to ensure proper setup of the system.

9.3.1.4 DMD Operations

The DMD data is loaded one row at a time with two (DLP7000 / DLP7000UV) or four (DLP9500 / DLP9500UV) LVDS buses into the DMD SRAM pixels. The DLP9500 / DLP9500UV requires all four data buses (A,B,C,D) while the DLP7000 / DLP7000UV requires only two data buses (A,B). Each bus consists of a clock (DDC_DCLKOUT), a control signal (SCTRL) and 16 differential pairs of LVDS signals (DDC_DOUT[15:0]) that are output from the DLPC410 as listed in *Pin Configuration and Functions*. Data, and control are clocked into the DMD on both the rising and falling edges of the DDR data clocks -- DDC_DCLKOUT_[A, B, C, D]. Data loading does not cause mirror switching until a Mirror Clocking Pulse (Reset) operation is completed.

The row load length in clocks can be determined by the equation (number of pixels per rows) / (data bus bit width × 2 edges per clock). There is a two in the denominator because the DMD data bus is dual data rate. This equation yields 15 clocks per row for 1920 x 1080 and a 64 bit bus or 16 clocks per row for 1024x768 and a 32 bit bus. However, with the DLP9500 / DLP9500UV there are 64 bits at the beginning and end of each row that are not displayed, yielding 16 clocks per row for both 1920 × 1080 and 1024 × 768 displays.

9.3.2 DLPC410 LVDS Input Data Bus Operations

Figure 6 shows an example of how the data should be formatted for a DLP9500 / DLP9500UV which takes 16 clocks to load a row. The clock should be synchronous and edge aligned with all data and control signals. Depending on the design, skewing the clock to data relationship may cause a problem.

No visible data is loaded for the first clock cycle for A and B data and for the last clock cycle for C and D data for each row load operation. This only applies to the DLP9500 / DLP9500UV.

Figure 7 shows an example of the data formatting for the DLP7000 / DLP7000UV.

The DVALID signal should be asserted synchronous to the data it is meant to frame. DVALID can be asserted as:

- Framing individual row loads with breaks between rows
- Framing block loads
- Framing the entire DMD load

If the DVALID frames blocks or the whole DMD, assure that block and row controls are adjusted at the proper locations in the data stream. See section *Block Operations* for further information.

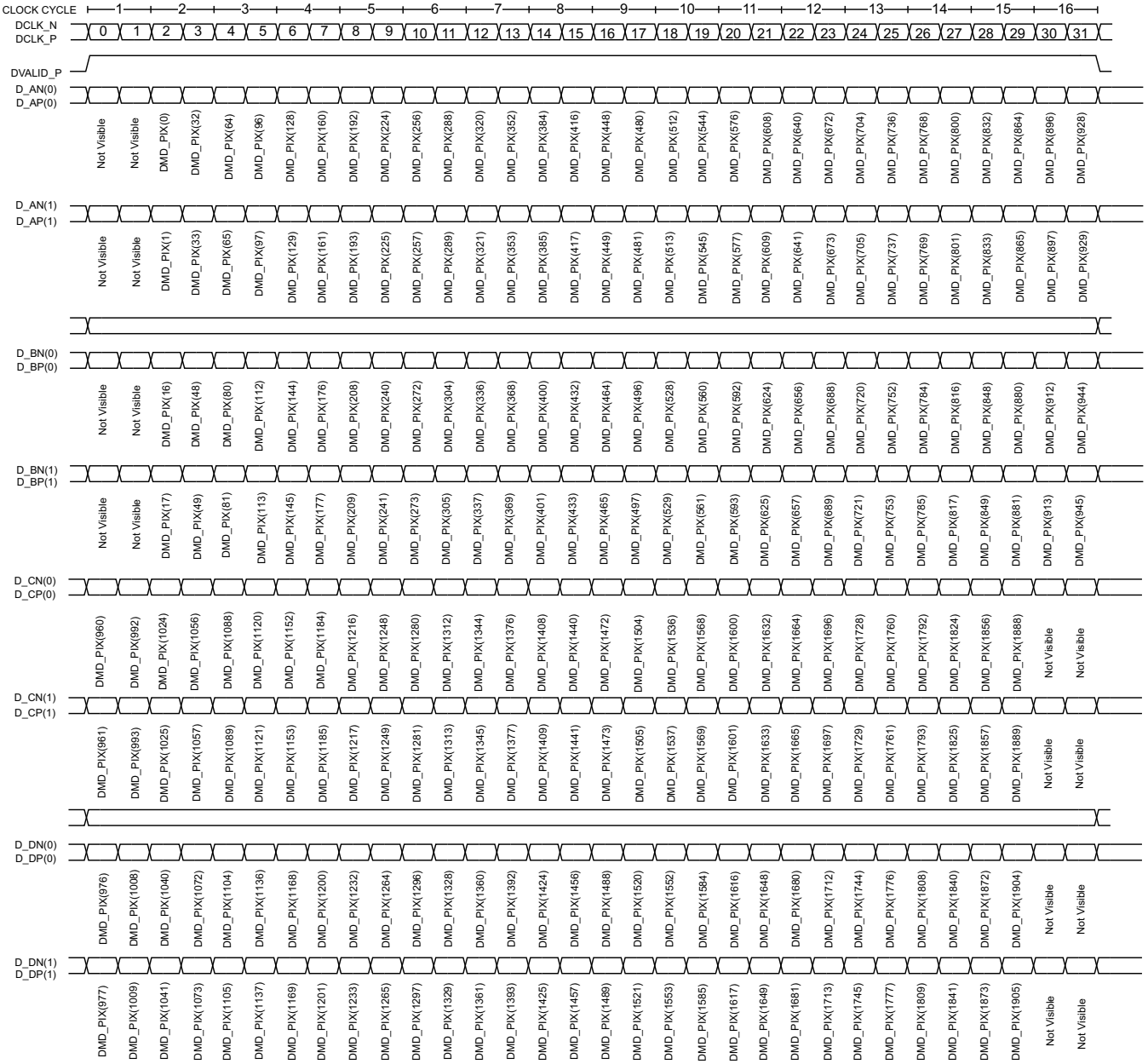


Figure 6. DLP9500 / DLP9500UV 2XLVDS DMD Input Data Bus

Table 3. DLP9500 / DLP9500UV 2XLVDS DMD Data Pixel Mapping D_A(16-0)

DCLK EDGE	D_A(0)	D_A(1)	D_A(2)	D_A(3)	D_A(4)	D_A(5)	D_A(6)	D_A(7)	D_A(8)	D_A(9)	D_A(10)	D_A(11)	D_A(12)	D_A(13)	D_A(14)	D_A(15)
0	Not Visible															
1																
2	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
3	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47
4	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79
5	96	97	98	99	100	101	102	103	104	105	106	107	108	109	110	111
6	128	129	130	131	132	133	134	135	136	137	138	139	140	141	142	143
7	160	161	162	163	164	165	166	167	168	169	170	171	172	173	174	175
8	192	193	194	195	196	197	198	199	200	201	202	203	204	205	206	207
9	224	225	226	227	228	229	230	231	232	233	234	235	236	237	238	239
10	256	257	258	259	260	261	262	263	264	265	266	267	268	269	270	271
11	288	289	290	291	292	293	294	295	296	297	298	299	300	301	302	303
12	320	321	322	323	324	325	326	327	328	329	330	331	332	333	334	335
13	352	353	354	355	356	357	358	359	360	361	362	363	364	365	366	367
14	384	385	386	387	388	389	390	391	392	393	394	395	396	397	398	399
15	416	417	418	419	420	421	422	423	424	425	426	427	428	429	430	431
16	448	449	450	451	452	453	454	455	456	457	458	459	460	461	462	463
17	480	481	482	483	484	485	486	487	488	489	490	491	492	493	494	495
18	512	513	514	515	516	517	518	519	520	521	522	523	524	525	526	527
19	544	545	546	547	548	549	550	551	552	553	554	555	556	557	558	559
20	576	577	578	579	580	581	582	583	584	585	586	587	588	589	590	591
21	608	609	610	611	612	613	614	615	616	617	618	619	620	621	622	623
22	640	641	642	643	644	645	646	647	648	649	650	651	652	653	654	655
23	672	673	674	675	676	677	678	679	680	681	682	683	684	685	686	687
24	704	705	706	707	708	709	710	711	712	713	714	715	716	717	718	719
25	736	737	738	739	740	741	742	743	744	745	746	747	748	749	750	751
26	768	769	770	771	772	773	774	775	776	777	778	779	780	781	782	783
27	800	801	802	803	804	805	806	807	808	809	810	811	812	813	814	815
28	832	833	834	835	836	837	838	839	840	841	842	843	844	845	846	847
29	864	865	866	867	868	869	870	871	872	873	874	875	876	877	878	879
30	896	897	898	899	900	901	902	903	904	905	906	907	908	909	910	911
31	928	929	930	931	932	933	934	935	936	937	938	939	940	941	942	943

Table 4. DLP9500 / DLP9500UV 2XLVDS DMD Data Pixel Mapping D_B(16-0)

DCLK EDGE	D_B(0)	D_B(1)	D_B(2)	D_B(3)	D_B(4)	D_B(5)	D_B(6)	D_B(7)	D_B(8)	D_B(9)	D_B(10)	D_B(11)	D_B(12)	D_B(13)	D_B(14)	D_B(15)
0	Not Visible															
1																
2	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
3	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63
4	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95
5	112	113	114	115	116	117	118	119	120	121	122	123	124	125	126	127
6	144	145	146	147	148	149	150	151	152	153	154	155	156	157	158	159
7	176	177	178	179	180	181	182	183	184	185	186	187	188	189	190	191
8	208	209	210	211	212	213	214	215	216	217	218	219	220	221	222	223
9	240	241	242	243	244	245	246	247	248	249	250	251	252	253	254	255
10	272	273	274	275	276	277	278	279	280	281	282	283	284	285	286	287
11	304	305	306	307	308	309	310	311	312	313	314	315	316	317	318	319
12	336	337	338	339	340	341	342	343	344	345	346	347	348	349	350	351
13	368	369	370	371	372	373	374	375	376	377	378	379	380	381	382	383
14	400	401	402	403	404	405	406	407	408	409	410	411	412	413	414	415
15	432	433	434	435	436	437	438	439	440	441	442	443	444	445	446	447
16	464	465	466	467	468	469	470	471	472	473	474	475	476	477	478	479
17	496	497	498	499	500	501	502	503	504	505	506	507	508	509	510	511
18	528	529	530	531	532	533	534	535	536	537	538	539	540	541	542	543
19	560	561	562	563	564	565	566	567	568	569	570	571	572	573	574	575
20	592	593	594	595	596	597	598	599	600	601	602	603	604	605	606	607
21	624	625	626	627	628	629	630	631	632	633	634	635	636	637	638	639
22	656	657	658	659	660	661	662	663	664	665	666	667	668	669	670	671
23	688	689	690	691	692	693	694	695	696	697	698	699	700	701	702	703
24	720	721	722	723	724	725	726	727	728	729	730	731	732	733	734	735
25	752	753	754	755	756	757	758	759	760	761	762	763	764	765	766	767
26	784	785	786	787	788	789	790	791	792	793	794	795	796	797	798	799
27	816	817	818	819	820	821	822	823	824	825	826	827	828	829	830	831
28	848	849	850	851	852	853	854	855	856	857	858	859	860	861	862	863
29	880	881	882	883	884	885	886	887	888	889	890	891	892	893	894	895
30	912	913	914	915	916	917	918	919	920	921	922	923	924	925	926	927
31	944	945	946	947	948	949	950	951	952	953	954	955	956	957	958	959

Table 5. DLP9500 / DLP9500UV 2XLVDS DMD Data Pixel Mapping D_C(16-0)

DCLK EDGE	D_C(0)	D_C(1)	D_C(2)	D_C(3)	D_C(4)	D_C(5)	D_C(6)	D_C(7)	D_C(8)	D_C(9)	D_C(10)	D_C(11)	D_C(12)	D_C(13)	D_C(14)	D_C(15)
0	960	961	962	963	964	965	966	967	968	969	970	971	972	973	974	975
1	992	993	994	995	996	997	998	999	1000	1001	1002	1003	1004	1005	1006	1007
2	1024	1025	1026	1027	1028	1029	1030	1031	1032	1033	1034	1035	1036	1037	1038	1039
3	1056	1057	1058	1059	1060	1061	1062	1063	1064	1065	1066	1067	1068	1069	1070	1071
4	1088	1089	1090	1091	1092	1093	1094	1095	1096	1097	1098	1099	1100	1101	1102	1103
5	1120	1121	1122	1123	1124	1125	1126	1127	1128	1129	1130	1131	1132	1133	1134	1135
6	1152	1153	1154	1155	1156	1157	1158	1159	1160	1161	1162	1163	1164	1165	1166	1167
7	1184	1185	1186	1187	1188	1189	1190	1191	1192	1193	1194	1195	1196	1197	1198	1199
8	1216	1217	1218	1219	1220	1221	1222	1223	1224	1225	1226	1227	1228	1229	1230	1231
9	1248	1249	1250	1251	1252	1253	1254	1255	1256	1257	1258	1259	1260	1261	1262	1263
10	1280	1281	1282	1283	1284	1285	1286	1287	1288	1289	1290	1291	1292	1293	1294	1295
11	1312	1313	1314	1315	1316	1317	1318	1319	1320	1321	1322	1323	1324	1325	1326	1327
12	1344	1345	1346	1347	1348	1349	1350	1351	1352	1353	1354	1355	1356	1357	1358	1359
13	1376	1377	1378	1379	1380	1381	1382	1383	1384	1385	1386	1387	1388	1389	1390	1391
14	1408	1409	1410	1411	1412	1413	1414	1415	1416	1417	1418	1419	1420	1421	1422	1423
15	1440	1441	1442	1443	1444	1445	1446	1447	1448	1449	1450	1451	1452	1453	1454	1455
16	1472	1473	1474	1475	1476	1477	1478	1479	1480	1481	1482	1483	1484	1485	1486	1487
17	1504	1505	1506	1507	1508	1509	1510	1511	1512	1513	1514	1515	1516	1517	1518	1519
18	1536	1537	1538	1539	1540	1541	1542	1543	1544	1545	1546	1547	1548	1549	1550	1551
19	1568	1569	1570	1571	1572	1573	1574	1575	1576	1577	1578	1579	1580	1581	1582	1583
20	1600	1601	1602	1603	1604	1605	1606	1607	1608	1609	1610	1611	1612	1613	1614	1615
21	1632	1633	1634	1635	1636	1637	1638	1639	1640	1641	1642	1643	1644	1645	1646	1647
22	1664	1665	1666	1667	1668	1669	1670	1671	1672	1673	1674	1675	1676	1677	1678	1679
23	1696	1697	1698	1699	1700	1701	1702	1703	1704	1705	1706	1707	1708	1709	1710	1711
24	1728	1729	1730	1731	1732	1733	1734	1735	1736	1737	1738	1739	1740	1741	1742	1743
25	1760	1761	1762	1763	1764	1765	1766	1767	1768	1769	1770	1771	1772	1773	1774	1775
26	1792	1793	1794	1795	1796	1797	1798	1799	1800	1801	1802	1803	1804	1805	1806	1807
27	1824	1825	1826	1827	1828	1829	1830	1831	1832	1833	1834	1835	1836	1837	1838	1839
28	1856	1857	1858	1859	1860	1861	1862	1863	1864	1865	1866	1867	1868	1869	1870	1871
29	1888	1889	1890	1891	1892	1893	1894	1895	1896	1897	1898	1899	1900	1901	1902	1903
30	Not Visible															
31																

Table 6. DLP9500 / DLP9500UV 2XLVDS DMD Data Pixel Mapping D_D(16-0)

DCLK EDGE	D_D(0)	D_D(1)	D_D(2)	D_D(3)	D_D(4)	D_D(5)	D_D(6)	D_D(7)	D_D(8)	D_D(9)	D_D(10)	D_D(11)	D_D(12)	D_D(13)	D_D(14)	D_D(15)
0	976	977	978	979	980	981	982	983	984	985	986	987	988	989	990	991
1	1008	1009	1010	1011	1012	1013	1014	1015	1016	1017	1018	1019	1020	1021	1022	1023
2	1040	1041	1042	1043	1044	1045	1046	1047	1048	1049	1050	1051	1052	1053	1054	1055
3	1072	1073	1074	1075	1076	1077	1078	1079	1080	1081	1082	1083	1084	1085	1086	1087
4	1104	1105	1106	1107	1108	1109	1110	1111	1112	1113	1114	1115	1116	1117	1118	1119
5	1136	1137	1138	1139	1140	1141	1142	1143	1144	1145	1146	1147	1148	1149	1150	1151
6	1168	1169	1170	1171	1172	1173	1174	1175	1176	1177	1178	1179	1180	1181	1182	1183
7	1200	1201	1202	1203	1204	1205	1206	1207	1208	1209	1210	1211	1212	1213	1214	1215
8	1232	1233	1234	1235	1236	1237	1238	1239	1240	1241	1242	1243	1244	1245	1246	1247
9	1264	1265	1266	1267	1268	1269	1270	1271	1272	1273	1274	1275	1276	1277	1278	1279
10	1296	1297	1298	1299	1300	1301	1302	1303	1304	1305	1306	1307	1308	1309	1310	1311
11	1328	1329	1330	1331	1332	1333	1334	1335	1336	1337	1338	1339	1340	1341	1342	1343
12	1360	1361	1362	1363	1364	1365	1366	1367	1368	1369	1370	1371	1372	1373	1374	1375
13	1392	1393	1394	1395	1396	1397	1398	1399	1400	1401	1402	1403	1404	1405	1406	1407
14	1424	1425	1426	1427	1428	1429	1430	1431	1432	1433	1434	1435	1436	1437	1438	1439
15	1456	1457	1458	1459	1460	1461	1462	1463	1464	1465	1466	1467	1468	1469	1470	1471
16	1488	1489	1490	1491	1492	1493	1494	1495	1496	1497	1498	1499	1500	1501	1502	1503
17	1520	1521	1522	1523	1524	1525	1526	1527	1528	1529	1530	1531	1532	1533	1534	1535
18	1552	1553	1554	1555	1556	1557	1558	1559	1560	1561	1562	1563	1564	1565	1566	1567
19	1584	1585	1586	1587	1588	1589	1590	1591	1592	1593	1594	1595	1596	1597	1598	1599
20	1616	1617	1618	1619	1620	1621	1622	1623	1624	1625	1626	1627	1628	1629	1630	1631
21	1648	1649	1650	1651	1652	1653	1654	1655	1656	1657	1658	1659	1660	1661	1662	1663
22	1680	1681	1682	1683	1684	1685	1686	1687	1688	1689	1690	1691	1692	1693	1694	1695
23	1712	1713	1714	1715	1716	1717	1718	1719	1720	1721	1722	1723	1724	1725	1726	1727
24	1744	1745	1746	1747	1748	1749	1750	1751	1752	1753	1754	1755	1756	1757	1758	1759
25	1776	1777	1778	1779	1780	1781	1782	1783	1784	1785	1786	1787	1788	1789	1790	1791
26	1808	1809	1810	1811	1812	1813	1814	1815	1816	1817	1818	1819	1820	1821	1822	1823
27	1840	1841	1842	1843	1844	1845	1846	1847	1848	1849	1850	1851	1852	1853	1854	1855
28	1872	1873	1874	1875	1876	1877	1878	1879	1880	1881	1882	1883	1884	1885	1886	1887
29	1904	1905	1906	1907	1908	1909	1910	1911	1912	1913	1914	1915	1916	1917	1918	1919
30	Not Visible															
31																

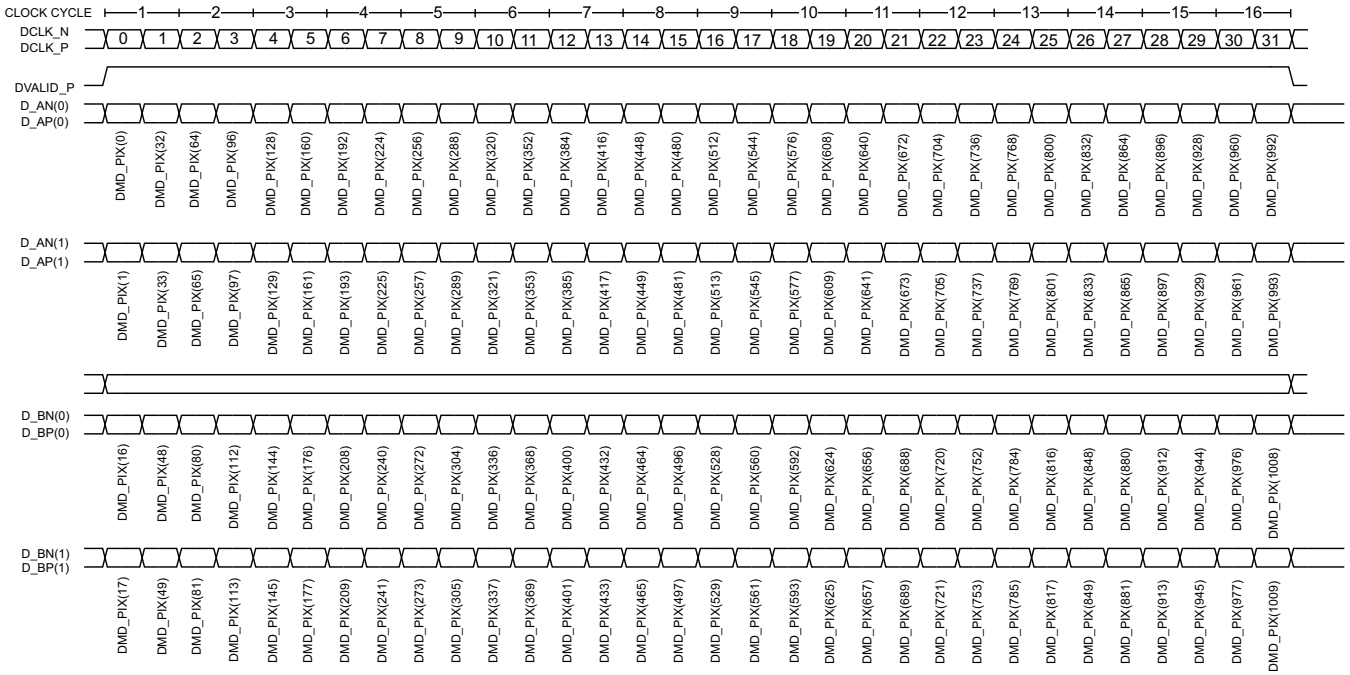


Figure 7. DLP7000 / DLP7000UV 2XLVDS DMD Input Data Bus

Table 7. DLP7000 / DLP7000UV 2XLVDS DMD Data Pixel Mapping D_A(16-0)

DCLK EDGE	D_A(0)	D_A(1)	D_A(2)	D_A(3)	D_A(4)	D_A(5)	D_A(6)	D_A(7)	D_A(8)	D_A(9)	D_A(10)	D_A(11)	D_A(12)	D_A(13)	D_A(14)	D_A(15)
0	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
1	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47
2	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79
3	96	97	98	99	100	101	102	103	104	105	106	107	108	109	110	111
4	128	129	130	131	132	133	134	135	136	137	138	139	140	141	142	143
5	160	161	162	163	164	165	166	167	168	169	170	171	172	173	174	175
6	192	193	194	195	196	197	198	199	200	201	202	203	204	205	206	207
7	224	225	226	227	228	229	230	231	232	233	234	235	236	237	238	239
8	256	257	258	259	260	261	262	263	264	265	266	267	268	269	270	271
9	288	289	290	291	292	293	294	295	296	297	298	299	300	301	302	303
10	320	321	322	323	324	325	326	327	328	329	330	331	332	333	334	335
11	352	353	354	355	356	357	358	359	360	361	362	363	364	365	366	367
12	384	385	386	387	388	389	390	391	392	393	394	395	396	397	398	399
13	416	417	418	419	420	421	422	423	424	425	426	427	428	429	430	431
14	448	449	450	451	452	453	454	455	456	457	458	459	460	461	462	463
15	480	481	482	483	484	485	486	487	488	489	490	491	492	493	494	495
16	512	513	514	515	516	517	518	519	520	521	522	523	524	525	526	527
17	544	545	546	547	548	549	550	551	552	553	554	555	556	557	558	559
18	576	577	578	579	580	581	582	583	584	585	586	587	588	589	590	591
19	608	609	610	611	612	613	614	615	616	617	618	619	620	621	622	623
20	640	641	642	643	644	645	646	647	648	649	650	651	652	653	654	655
21	672	673	674	675	676	677	678	679	680	681	682	683	684	685	686	687
22	704	705	706	707	708	709	710	711	712	713	714	715	716	717	718	719
23	736	737	738	739	740	741	742	743	744	745	746	747	748	749	750	751
24	768	769	770	771	772	773	774	775	776	777	778	779	780	781	782	783
25	800	801	802	803	804	805	806	807	808	809	810	811	812	813	814	815
26	832	833	834	835	836	837	838	839	840	841	842	843	844	845	846	847
27	864	865	866	867	868	869	870	871	872	873	874	875	876	877	878	879
28	896	897	898	899	900	901	902	903	904	905	906	907	908	909	910	911
29	928	929	930	931	932	933	934	935	936	937	938	939	940	941	942	943
30	960	961	962	963	964	965	966	967	968	969	970	971	972	973	974	975
31	992	993	994	995	996	997	998	999	1000	1001	1002	1003	1004	1005	1006	1007

Table 8. DLP7000 / DLP7000UV 2XLVDS DMD Data Pixel Mapping D_B(16-0)

DCLK EDGE	D_B(0)	D_B(1)	D_B(2)	D_B(3)	D_B(4)	D_B(5)	D_B(6)	D_B(7)	D_B(8)	D_B(9)	D_B(10)	D_B(11)	D_B(12)	D_B(13)	D_B(14)	D_B(15)
0	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
1	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63
2	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95
3	112	113	114	115	116	117	118	119	120	121	122	123	124	125	126	127
4	144	145	146	147	148	149	150	151	152	153	154	155	156	157	158	159
5	176	177	178	179	180	181	182	183	184	185	186	187	188	189	190	191
6	208	209	210	211	212	213	214	215	216	217	218	219	220	221	222	223
7	240	241	242	243	244	245	246	247	248	249	250	251	252	253	254	255
8	272	273	274	275	276	277	278	279	280	281	282	283	284	285	286	287
9	304	305	306	307	308	309	310	311	312	313	314	315	316	317	318	319
10	336	337	338	339	340	341	342	343	344	345	346	347	348	349	350	351
11	368	369	370	371	372	373	374	375	376	377	378	379	380	381	382	383
12	400	401	402	403	404	405	406	407	408	409	410	411	412	413	414	415
13	432	433	434	435	436	437	438	439	440	441	442	443	444	445	446	447
14	464	465	466	467	468	469	470	471	472	473	474	475	476	477	478	479
15	496	497	498	499	500	501	502	503	504	505	506	507	508	509	510	511
16	528	529	530	531	532	533	534	535	536	537	538	539	540	541	542	543
17	560	561	562	563	564	565	566	567	568	569	570	571	572	573	574	575
18	592	593	594	595	596	597	598	599	600	601	602	603	604	605	606	607
19	624	625	626	627	628	629	630	631	632	633	634	635	636	637	638	639
20	656	657	658	659	660	661	662	663	664	665	666	667	668	669	670	671
21	688	689	690	691	692	693	694	695	696	697	698	699	700	701	702	703
22	720	721	722	723	724	725	726	727	728	729	730	731	732	733	734	735
23	752	753	754	755	756	757	758	759	760	761	762	763	764	765	766	767
24	784	785	786	787	788	789	790	791	792	793	794	795	796	797	798	799
25	816	817	818	819	820	821	822	823	824	825	826	827	828	829	830	831
26	848	849	850	851	852	853	854	855	856	857	858	859	860	861	862	863
27	880	881	882	883	884	885	886	887	888	889	890	891	892	893	894	895
28	912	913	914	915	916	917	918	919	920	921	922	923	924	925	926	927
29	944	945	946	947	948	949	950	951	952	953	954	955	956	957	958	959
30	976	977	978	979	980	981	982	983	984	985	986	987	988	989	990	991
31	1008	1009	1010	1011	1012	1013	1014	1015	1016	1017	1018	1019	1020	1021	1022	1023

9.3.3 Block Operations

The DMD mirrors and corresponding SRAM pixels are organized into BLKS and each block is broken into groups of ROWS per BLK as described in Table 2. Mirror blocks are addressed for either the Mirror Clocking Pulse (Reset) or Memory Clear functions by asserting block control signals at the start of each row data load. RST2BLK, BLK_MD and BLK_AD are used as shown in Table 9 to designate which mirror block or blocks are to be issued a Mirror Clocking Pulse or Cleared. Refer to the individual DMD data sheets for block location information.

- The clear operation sets all of the SRAM pixels in the designated block to logic zero during the current row cycle.
- It is possible to issue a Mirror Clocking Pulse to a block while loading a different block.
- It is not possible to Clear a block while writing to a different block.
- It is not necessary to Clear a block if it is going to be reloaded with new data (just like a normal memory cell).
- For the DLP9500 / DLP9500UV a Block Clear operation must be followed by two no-op row load cycles.
- Note that the DLP9500 / DLP9500UV has 15 blocks (block 00 – block 14) so block operations on block 15 have no function for this DMD.
- It is recommended that $\overline{\text{RST2BLK}}$ be set to one value and not adjusted during normal system operation. A change in $\overline{\text{RST2BLK}}$ is not immediately effective and will require more than one row load cycle to complete.

NOTE

(1080p DMD Only) To clear one Mirror Clocking Pulse (Reset) Group in the DMD Block, one Clear command followed by two consecutive No Operation commands are required. Therefore, 15 total Block Clear commands and 30 total No Operation commands are required to clear the entire DMD array.

NOTE

$\overline{\text{RST2BLK}}$ needs to be kept low during initialization for proper setup of the system.

Table 9. Block Operations

$\overline{\text{RST2BLK}}$	BLK_MD 1	BLK_MD 0	BLK_AD 3	BLK_AD2	BLK_AD 1	BLK_AD 0	OPERATION
X	0	0	X	X	X	X	None
X	0	1	0	0	0	0	Clear block 00
X	0	1	0	0	0	1	Clear block 01
X	0	1	0	0	1	0	Clear block 02
X	0	1	0	0	1	1	Clear block 03
X	0	1	0	1	0	0	Clear block 04
X	0	1	0	1	0	1	Clear block 05
X	0	1	0	1	1	0	Clear block 06
X	0	1	0	1	1	1	Clear block 07
X	0	1	1	0	0	0	Clear block 08
X	0	1	1	0	0	1	Clear block 09
X	0	1	1	0	1	0	Clear block 10
X	0	1	1	0	1	1	Clear block 11
X	0	1	1	1	0	0	Clear block 12
X	0	1	1	1	0	1	Clear block 13
X	0	1	1	1	1	0	Clear block 14
X	0	1	1	1	1	1	Clear block 15
X	1	0	0	0	0	0	Reset block 00
X	1	0	0	0	0	1	Reset block 01
X	1	0	0	0	1	0	Reset block 02
X	1	0	0	0	1	1	Reset block 03
X	1	0	0	1	0	0	Reset block 04
X	1	0	0	1	0	1	Reset block 05
X	1	0	0	1	1	0	Reset block 06
X	1	0	0	1	1	1	Reset block 07
X	1	0	1	0	0	0	Reset block 08
X	1	0	1	0	0	1	Reset block 09
X	1	0	1	0	1	0	Reset block 10
X	1	0	1	0	1	1	Reset block 11
X	1	0	1	1	0	0	Reset block 12
X	1	0	1	1	0	1	Reset block 13
X	1	0	1	1	1	0	Reset block 14
X	1	0	1	1	1	1	Reset block 15
0	1	1	0	0	0	0	Reset blocks 00-01
0	1	1	0	0	0	1	Reset blocks 02-03
0	1	1	0	0	1	0	Reset blocks 04-05
0	1	1	0	0	1	1	Reset blocks 06-07
0	1	1	0	1	0	0	Reset blocks 08-09
0	1	1	0	1	0	1	Reset blocks 10-11
0	1	1	0	1	1	0	Reset blocks 12-13
0	1	1	0	1	1	1	Reset blocks 14-15
1	1	1	0	0	0	X	Reset blocks 00-03
1	1	1	0	0	1	X	Reset blocks 04-07
1	1	1	0	1	0	X	Reset blocks 08-11
1	1	1	0	1	1	X	Reset blocks 12-15
X	1	1	1	0	X	X	Reset blocks 00-15
X	1	1	1	1	X	X	Float blocks 00-15

9.3.3.1 Mirror Clocking Pulse (Reset) and Float Operations

A Mirror Clocking Pulse (Reset) sequence begins by asserting BLK_MD and BLK_AD as described in Table 9. Shortly after, RST_ACTIVE goes high for approximately 4.5 µs, indicating a Mirror Clocking Pulse operation is in progress. During this time, no additional Mirror Clocking Pulses may be initiated until RST_ACTIVE returns low. RST_ACTIVE does not return to low unless continuous no-op or data loading row cycles are issued. See the Figure 8 and Figure 9 for typical Mirror Clocking Pulse sequences in which consecutive DMD blocks are loaded then sent Mirror Clocking Pulses. Mirror Clocking Pulse time is identical for single, dual, quad or global operations.

Note that it may take longer to complete a Mirror Clocking Pulse on a block than it does to load, depending on the clock rate and the DMD type, so the scenario in Figure 8 does not show the situation when the Mirror Clocking Pulse time exceeds the block load time. The block load time may be calculated as:

Block Load Time = Clock Period × number CLKS per ROW × number ROWS per BLK

Table 10. DMD Block Load Time at 400 MHz DMD Clock

DMD	MINIMUM BLOCK LOAD TIME
DLP7000 / DLP7000UV	1.92 µsec
DLP9500 / DLP9500UV	2.88 µsec

For any case which involves sending a Mirror Clocking Pulse or Clearing blocks without data loading, the customer interface must send no-op row cycles. This can be accomplished by asserting DVALID, while holding ROWMD at “00” and BLKMD at “00” for number of CLKS per ROW (Table 10) clock cycles, as in Figure 10. For example, the sequence shown in Figure 9 does not show the required no-op row during the Delay cycle where a Mirror Clocking Pulse of Block 0 occurs. At least one row cycle must be completed to initiate the Mirror Clocking Pulse. The same procedure applies to the Global Mirror Clocking Pulse case as shown in Figure 11. Following the loading of all rows in the device, a no-op row cycle must be completed to initiate the Mirror Clocking Pulse. If the global Mirror Clocking Pulse is asserted prior to loading all rows of the device, rows which were not updated will show old data. Additional Mirror Clocking Pulse operations may not be initiated until RST_ACTIVE is low. Block clear operations for DLP9500 / DLP9500UV must be followed by two consecutive no-op row cycle commands.

To obtain full utilization of the DLP9500 / DLP9500UV bandwidth (at 400MHz data rate), load two blocks and then issue a Mirror Clocking Pulse to the two blocks at a time by setting $\overline{\text{RST2BLK}}$ to “0” and BLK_MD to “11” and the appropriate address in BLK_AD. This method is indicated in Figure 12. To obtain full utilization of the DLP7000 / DLP7000UV bandwidth (at 400 MHz data rate), load and issue a Mirror Clocking Pulse to four blocks at a time by setting $\overline{\text{RST2BLK}}$ to “1” and BLK_MD to “11” and the appropriate address in BLK_AD.

IMPORTANT:

While RST_ACTIVE is high, and for 8 µs after, the data for the block(s) being issued a Mirror Clocking Pulse should not be changed to allow for the settling required for the mirrors to become stable.

It is possible to load other blocks while the block previously issued a Mirror Clocking Pulse is settling. Figure 13 shows a single block load, Mirror Clocking Pulse and reload sequence with the light gray areas indicating mirror settling time.

It is best to issue a float command to avoid leaving a static image on the DMD for extended periods of time. A mirror float sequence begins by asserting the proper BLK_MD and BLK_AD as described in Table 9. During the following row cycle, the DMD releases the tension under each mirror so that all mirrors are in a relatively flat position. The float operation takes approximately 3 µs to complete, during which time RST_ACTIVE is asserted.

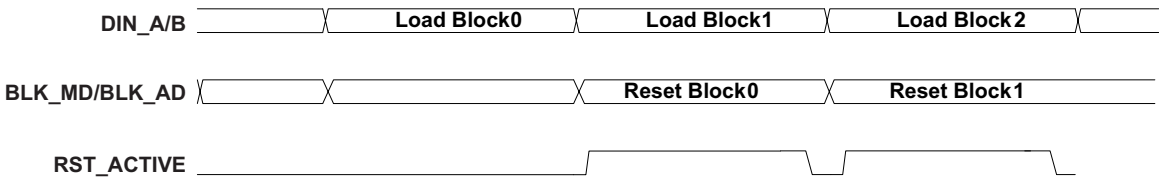


Figure 8. Typical Phased Mirror Clocking Pulse Sequence

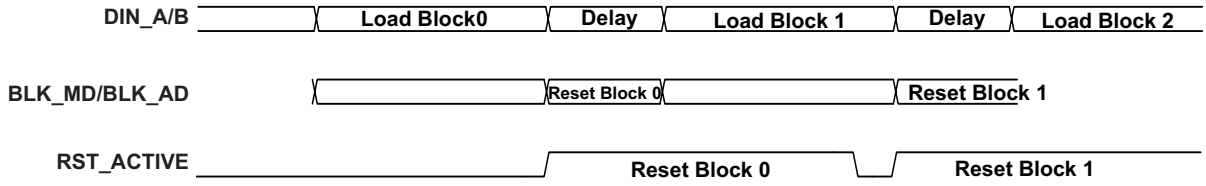


Figure 9. Alternate Phased Mirror Clocking Pulse Sequence

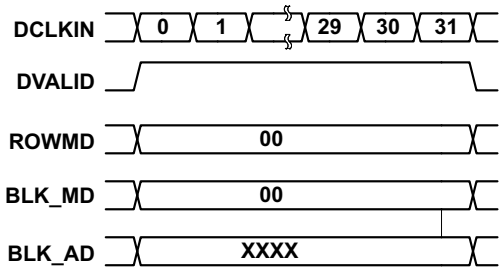


Figure 10. DMD No-op Row Cycle

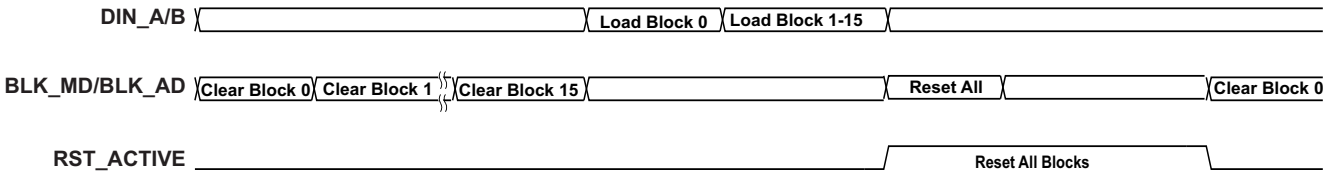


Figure 11. Full Device Load and Global Mirror Clocking Pulse

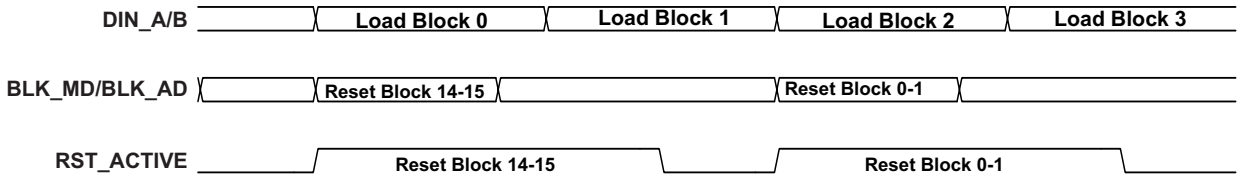


Figure 12. Phased Mirror Clocking Pulse Sequence with Dual Block Mirror Clocking Pulses without Memory Clear

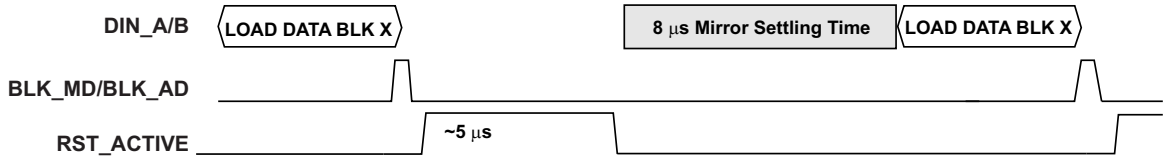


Figure 13. Block Load and Reload

NOTE

After a Mirror Clocking Pulse or Clear command is given, RST_ACTIVE may not be asserted until up to 60ns (depending on the clock frequency) after the command. During this time, no other command should be given.

9.3.3.2 Global Mirror Clocking Pulse (Reset) Consideration

A Global Mirror Clocking Pulse (BLK_MD = 11 and BLK_AD = 10XX), takes the same amount of time as the single, dual, and quad block Mirror Clocking Pulses. In addition to requiring a no-op row cycle to initiate a global Mirror Clocking Pulse, a row cycle (either no-op or data loading) is also required to complete the operation. If the customer interface is monitoring RST_ACTIVE to determine when to send a subsequent row cycle, it never sees RST_ACTIVE transition low. One method of operation would be to continue sending no-op row cycles until RST_ACTIVE goes low then continue loading data with real row cycles. Another method of operation is to delay greater than 4.5 µs, then start loading new data to DMD.

9.3.3.3 RST_ACTIVE

After a Mirror Clocking Pulse (Reset) or Float operation is requested, RST_ACTIVE is asserted to indicate that the operation is in progress. The *Mirror Clocking Pulse (Reset) and Float Operations* section has more details about the use of this signal. RST_ACTIVE is synchronized to a version of DCLKIN. As such, circuits in the application FPGA should consider this signal asynchronous and use standard synchronization techniques to assure reliable registering of this signal.

9.3.3.4 Interface Training Pattern

The DLPC410 detects the phase differences between the ½ speed clock (used in the device driving the LVDS data) and the internally generated ½ speed data clocks and automatically corrects their alignment. This is done by supplying a simple repeating pattern on all of the data inputs while the INIT_ACTIVE output of the DLPC410 is high/active. The details of the training pattern are described below.

This is a simple block diagram of the training pattern insertion logic.

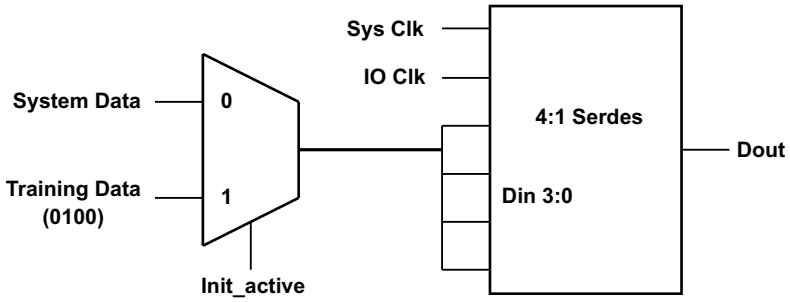


Figure 14. Block Diagram of Training Pattern Logic

The expected training pattern is 0100. In Figure 15 the data input to the 4:1 SERDES cells is captured on the rising edge of the ½ speed system clock. The output latency shown is based on the documentation for the Xilinx SERDES cells. Individual implementation may vary depending on the type of cells, technology, and design technique used.

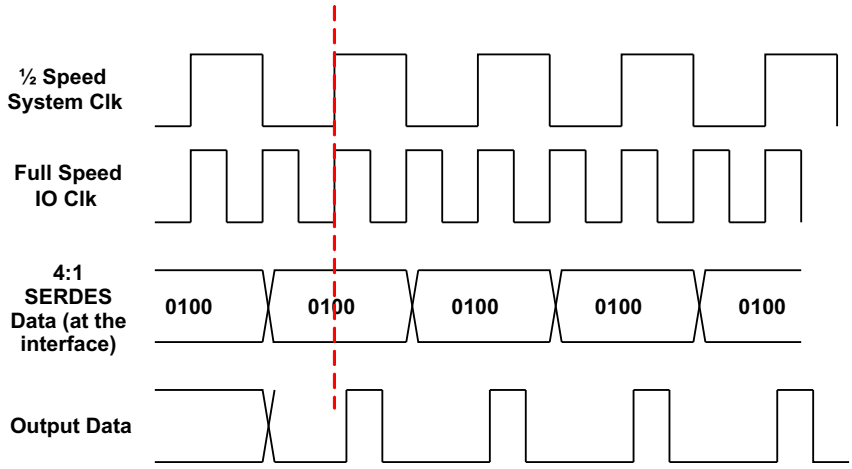


Figure 15. Training Pattern Alignment

NOTE

In Xilinx FPGAs (due to the construction of the ISERDES and OSERDES cells) a pattern of 0010 needs to be applied to the output/transmitting SERDES cells data pins (D1 = 0, D2 = 0, D3 = 1, D4 = 0) in order to receive a result of 0100 (Q1 = 0, Q2 = 1, Q3 = 0, Q4 = 0) at the input/receiving SERDES cell.

The patterns should be applied on all of the data and DVALID pins. In this respect, the interface is treated as a 17 bit interface with DVALID being the 17th data bit. The receiving logic in the DLPC410 will shift the data until the correct pattern is seen at the inputs. The SERDES cells align the incoming data with the ½ speed system clock (derived from the full speed data clock). This allows DLPC410 to correctly align the DVALID signal and the incoming data and will contribute to a more robust interface. It is important that the training pattern is applied to the DVALID and data inputs of the DLPC410 before reset to the device is deasserted, as training commences immediately on the deassertion of reset. The INIT_ACTIVE signal is asserted while the device is held in reset in order to help facilitate this behavior.

9.3.4 LED0

The LED0 signal is typically connected to an LED to show that the DLPC410 is operating normally. The signal is 1 Hz with 50% duty cycle, otherwise known as the heartbeat.

9.3.5 LED1

The LED1 signal is typically connected to an LED indicator to show the status of system initialization and the status of the clock circuits. The LED1 signal is asserted only when system initialization is complete and clock circuits are initialized. Logically, these signals are ANDed together to show an indication of the health of the system. If the Phase Locked Loop (PLL) connected to the data clock and the DMD clock are functioning correctly after system initialization, the LED will be illuminated.

9.3.6 Watchdog Timer

The DLPC410 contains a watchdog timer that initiates a global DMD Mirror Clocking Pulse in the event that any DMD reset block has not received a Mirror Clocking Pulse by the user within 10 seconds. This auto-Mirror Clocking Pulse function can be disabled by taking $\overline{\text{WDT\_ENABLE}}$ high.

9.3.7 Miscellaneous DMD Controls

It is recommended that the Complement and Flip flags be set to one value and not adjusted during normal system operation. These controls are asserted through a different mechanism than the data and row controls, hence their effect is asynchronous and cannot be expected to take effect immediately upon assertion.

9.3.7.1 Complement Data

By setting the COMP_DATA flag high, the user is able to command the DMD to internally complement its data inputs prior to loading the data into the mirror array. At least 0.6 ms is needed for the signal to be loaded. This signal should not be used to invert data on a row basis. When used with the “Clear” command, the mirrors are still set to zero regardless of the COMP_DATA bit. The COMP_DATA signal should be kept low during initialization to ensure proper setup of the system.

9.3.7.2 North/South Flip

NS_FLIP allows the user to specify the loading direction of rows in the DMD when used with ROWMD = “01”. This control has no effect if ROWMD = “10”.

Table 11 and Table 12 describe the effect of N/S flip. If NS_FLIP is set, this does not reverse the direction of Mirror Clocking Pulse groups (blocks). For example, the normal case is to Mirror Clocking Pulse blocks 0 – 15 in order. When NS_FLIP is set, the order of block Mirror Clocking Pulses must be reversed to 15 – 0.

The NS_FLIP signal should be kept low during initialization to ensure proper setup of the system.

9.3.7.3 DMD_A_RESET

DMD_A_RESET is an active low reset to the DMD. This signal is deasserted as appropriate at the end of system initialization.

9.3.8 DLPA200 Control Signals

Coordinating the operation of the DLPA200 with the DMD is one of the primary functions of the DLPC410. During system initialization, the DLPC410 releases the reset pin (DAD_INIT) and communicates with the DLPA200 via a serial bus to configure the device. Once this is complete, the high voltage output pins are enabled to prepare for command execution. As the DLPC410 is commanded to load data and perform Mirror Clocking Pulses, the DAD_ADDR address, DAD_MODE mode, DAD_SEL select and DAD_STROBE strobe signals are asserted as appropriate to cause the Mirror Clocking Pulse.

9.3.9 DDC_VERSION(3:0)

These four pins identify the version of the DLPC410 determined by the contents of DLPR410. If a problem is encountered, provide the version number with detailed information of the problem. See the DLPR410 datasheet (DLPS027) for the version number reported on these pins.

9.3.10 DMD_TYPE(3:0)

Four Output pins from the DLPC410 identify the DMD type detected by the DLPC410 (shown in Table 2). DMD_TYPE will return 1111 if the DMD is not attached or not recognized.

9.3.11 ECM2M_TP_ (31:0)

Reserved signals for test signal output. Do not drive these signals.

9.4 Device Functional Modes

The DLPC410 has one basic functional mode: displaying binary patterns at very high speeds. The input clock can be from 200 to 400 MHz. The *Feature Description* section describes various functions of the controller that can control how the binary data is loaded and displayed.

9.5 Programming

9.5.1 Data and Command Write Cycle

Once initialization is complete (INIT_ACTIVE = 0) the user is free to send data and control information to the DLPC410. When the user asserts the DVALID signal for the LVDS input buses, the DLPC410 begins sampling the LVDS data inputs and synchronously sending this information to the DMD along with row address control information. The row cycle period is exactly 16 clock cycles long and begins with DVALID as shown in Figure 6. If DVALID is removed, the DLPC410 stops loading data and commands until DVALID goes active again.

Programming (continued)

Figure 16 shows an example of data written to the DLPC410 for a single row using the DLP7000 / DLP7000UV. Data is written to the DMD 32 bits (16 A bits + 16 B bits) on each clock edge. An entire line must be written for data to be latched into memory and it requires 16 DDR clock cycles to write a single row of 1024 bits. For the DLP9500 / DLP9500UV 64 data bits (16 A bits + 16 B bits + 16 C bits + 16 D bits) are written on each clock edge. C data and D data bits are not used for the DLP7000 / DLP7000UV.

The DMD incorporates single row write operations using a row address counter that is randomly addressable. As shown in Table 11 and Table 12, ROWMD(1:0) determines the single row write count mode and ROWAD(10:0) determines the single row write address. ROWMD and ROWAD must be asserted and deasserted synchronously with DVALID and must be valid synchronous to the beginning of the data as shown in Figure 16.

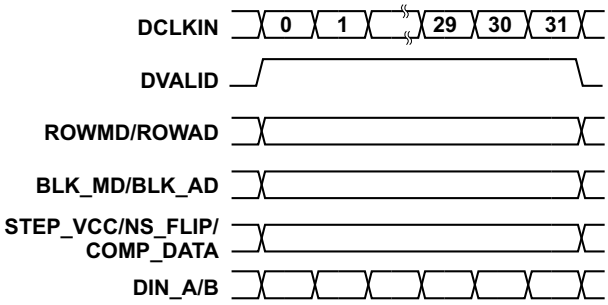


Figure 16. Single Row Write Operation

Row address orientation depends on the North or South Flip Flag (NS_FLIP) input to the DLPC410. See the individual DMD data sheets for orientation of rows, columns, and Mirror Clocking Pulse blocks. The row address counter does not automatically wrap-around when using the increment row address pointer instruction. After the final row is addressed, the row address pointer must be cleared to 0.

Table 11. Row Write Modes - N/S Flip Flag = 0

ROWMD		ROWAD											ACTION
1	0	10	9	8	7	6	5	4	3	2	1	0	
0	0	0	0	0	0	0	0	0	0	0	0	0	None
0	1	0	0	0	0	0	0	0	0	0	0	0	Increment row address pointer and write the concurrent data into that row
1	0	R	R	R	R	R	R	R	R	R	R	R	Set row address pointer to R and write the concurrent data into that row.
1	1	0	0	0	0	0	0	0	0	0	0	0	Clear row address pointer to 0 and write concurrent data into first row (that is, row ‘0’)

Table 12. Row Write Modes - N/S Flip Flag = 1

ROWMD		ROWAD											ACTION
1	0	10	9	8	7	6	5	4	3	2	1	0	
0	0	0	0	0	0	0	0	0	0	0	0	0	None
0	1	0	0	0	0	0	0	0	0	0	0	0	Decrement the row address pointer and write the concurrent data into that row
1	0	R	R	R	R	R	R	R	R	R	R	R	Set the row address pointer to R and write the concurrent data into that row.
1	1	0	0	0	0	0	0	0	0	0	0	0	Set row address pointer to row = last row and write concurrent data into last row (that is, the last row = 767 for the 0.7 XGA)

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The DLP7000 / DLP7000UV and DLP9500 / DLP9500UV devices require they be coupled with the DLPC410 controller to provide a reliable solution for many different applications. The DMDs are spatial light modulators which reflect incoming light from an illumination source to one of two directions, with the primary direction being into a projection collection optic. Each application is derived primarily from the optical architecture of the system and the format of the data coming into the DLPC410. Applications of interest include industrial, medical and intelligent display.

10.1.1 Device Description

The DLP7000 / DLP7000UV and DLP9500 / DLP9500UV chipsets offer developers a convenient way to design a wide variety of industrial, medical, and advanced display applications by delivering maximum flexibility in formatting data, sequencing data, and light patterns.

These chipsets include the following components:

DLPC410 DMD Digital Controller

- Provides high speed LVDS data and control interface to the user.
- Drives mirror clocking pulse and timing information to the DLPA200.
- Supports random row addressing.

DLPR410 EEPROM

- Contains startup configuration information.

DLPA200 DMD Micromirror Driver (1 required for DLP7000 / DLP7000UV DMD and 2 required for DLP9500 and DLP9500UV DMD)

- Generates Micromirror Clocking Pulse control (sometimes referred to as a *Reset*) of 16 banks of DMD mirrors.

DMD: Digital Micromirror Device containing the array of aluminum mirrors that steer light in two digital positions (+12 degrees and -12 degrees).

- DLP7000 / DLP7000UV DMD: 0.7-inch array diagonal, 1024 x 768 micromirror array, XGA display resolution.
- DLP9500 / DLP9500UV DMD: 0.95-inch array diagonal, 1920 x 1080 micromirror array, 1080p display resolution.

  Reliable function and operation of the DLP7000 / DLP7000UV and DLP9500 / DLP9500 / DLP9500UV require the DMDs to be used in conjunction with the components listed in Table 1. This document describes the proper integration and use of the chipset components.

  The DLPC410 chipset can be combined with a user programmable Application FPGA (not included) to create high performance systems.

10.2 Typical Application

A typical embedded system application using the DLPC410 controller is shown in Figure 17 and in Figure 18. In this configuration, the DLPC410 controller supports a 24-bit parallel RGB input, typical of LCD interfaces, from an exteral source or processor. This system supports both still and motion video sources. However, the controller only supports sources with periodic synchronization pulses. This is ideal for motion video sources, but can also be used for still images by maintaining periodic syncs and only sending a new frame of data when needed. The still image must be fully contained within a single video frame and meet the frame timing constraints. The DLPC410 controller refreshes the displayed image at the source frame rate and repeats the last active frame for intervals in which no new frame has been received.

Typical Application (continued)

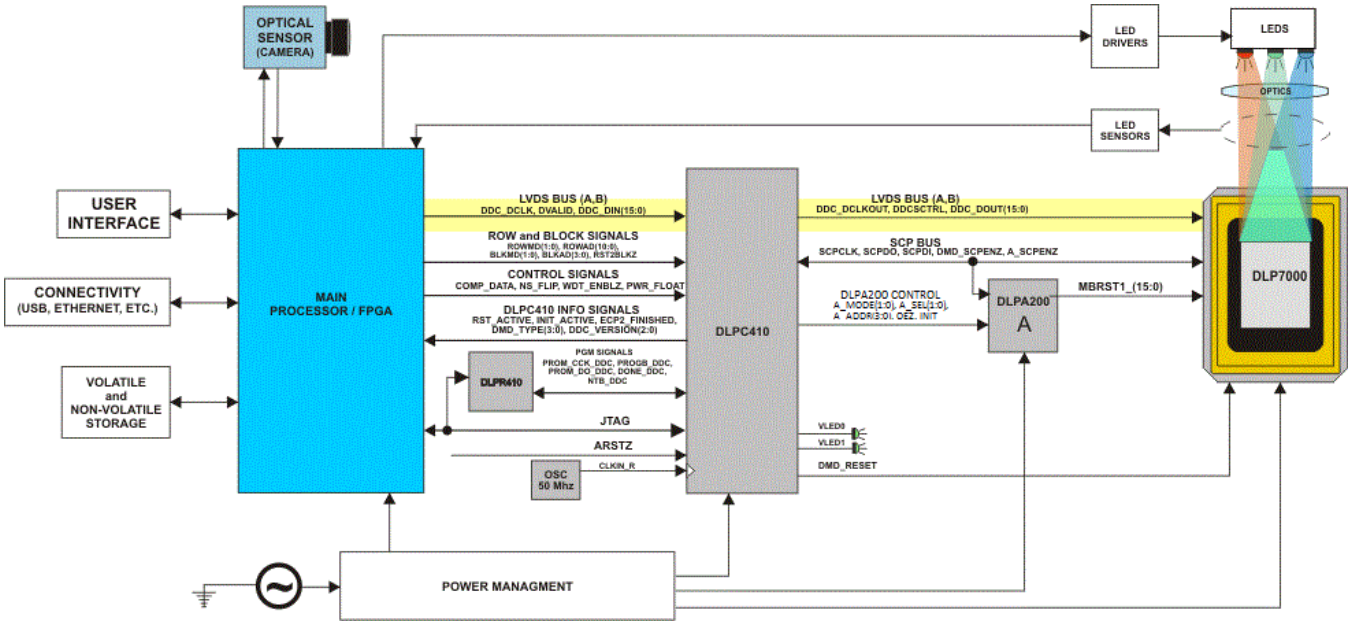


Figure 17. DLPC410 and DLP7000 / DLP7000UV Embedded Example Block Diagram

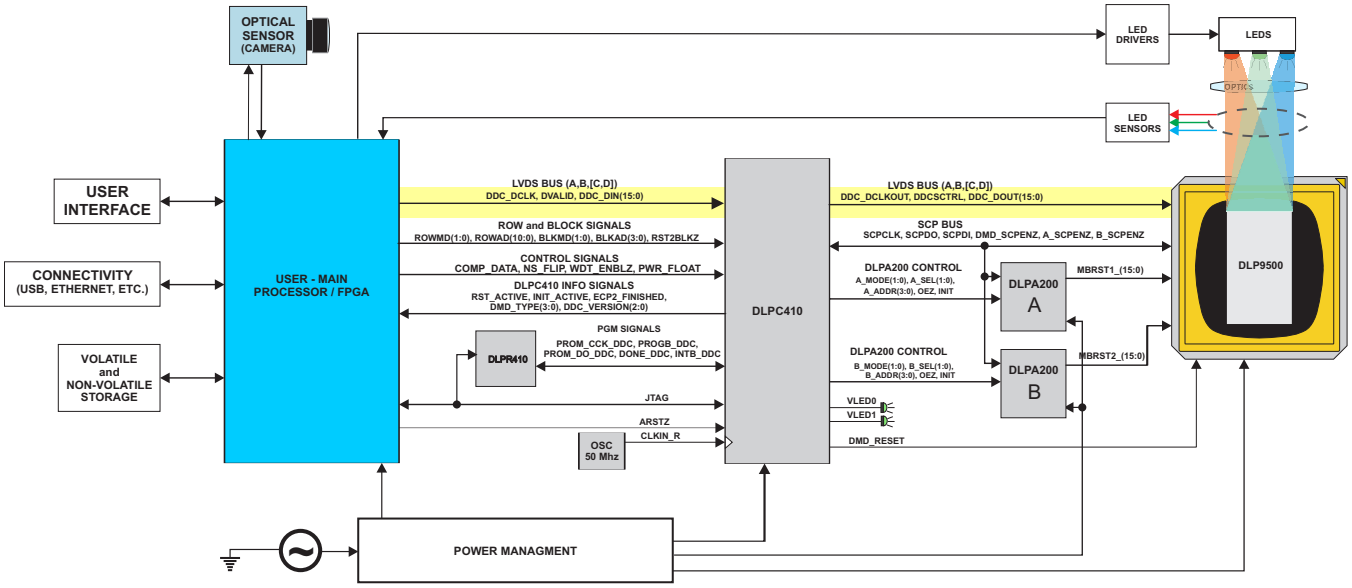


Figure 18. DLPC410 and DLP9500 / DLP9500UV Embedded Example Block Diagram

10.2.1 Design Requirements

All applications using the DLP 0.7-inch XGA or DLP 0.95-inch 1080p chipsets require both the DLPC410 controller and the DMD components for operation. The system also requires an external parallel flash memory device loaded with the DLPC410 Configuration and Support Firmware. The chipset has several system interfaces and requires some support circuitry. The following interfaces and support circuitry are required:

- DLPC410 System Interfaces:
  - Control Interface
  - Trigger Interface

Typical Application (continued)

  - Input Data Interface
  - Illumination Interface
  - Reference CLock
- DMD Interfaces:
  - DLPC410 to DLP7000 / DLP7000UV or DLP9500 / DLP9500UV Digital Data
  - DLPC410 to DLP7000 / DLP7000UV or DLP9500 / DLP9500UV Control Interface
  - DLPC410 to DLP7000 / DLP7000UV or DLP9500 / DLP9500UV Micromirror Clocking Pulse (Reset) Control Interface

10.2.2 Detailed Design Procedure

The DLP7000 and DLP9500 DMD are designed to be operated by the DLPC410 controller and are well suited for visible light applications requiring fast, spatially programmable light patterns using the micromirror array. In addition the DLP7000UV and DLP9500UV are well suited for direct imaging lithography, 3D printing applications, and other applications requiring ultraviolet light (UVA). See the block diagrams in *Functional Block Diagrams* to see the connections between the DLP7000 / DLP7000UV or DLP9500 / DLP9500UV DMD, the DLPC410 digital controller, the DLPR410 EEPROM, and the DLPA200 DMD micromirror drivers. Layout guidelines should be followed for reliability.

10.2.3 Application Curves

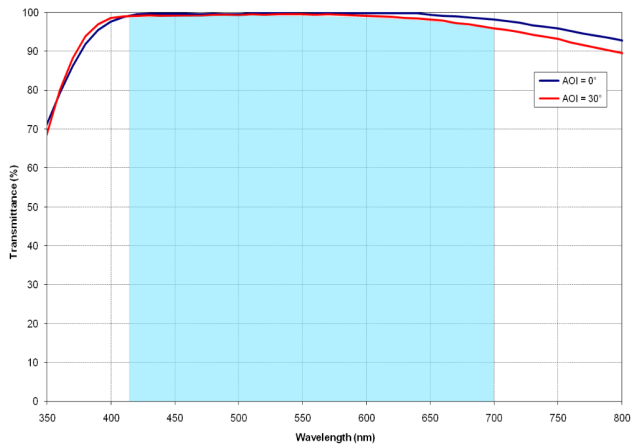


Figure 19. DLP7000 and DLP9500 Transmittance (Visible Window)

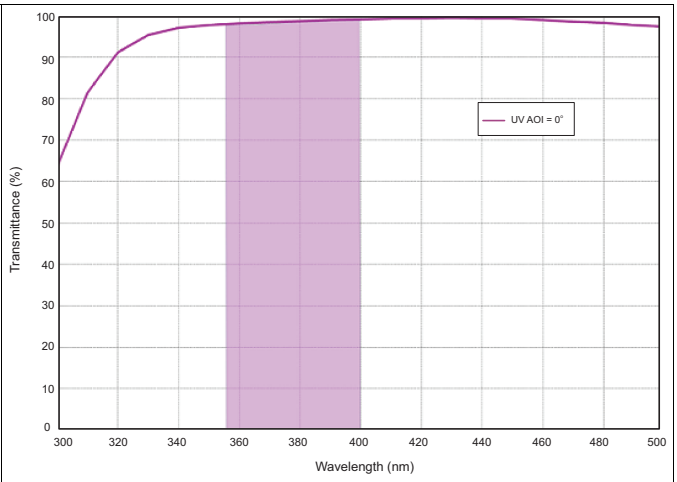


Figure 20. DLP7000UV and DLP9500UV Transmittance (UV Window)

10.3 Initialization Setup

10.3.1 Debugging Guidelines

Prior to checking the DLPC410 signals, make sure the reference clock to the DLPC410 is running at 50 MHz. Check that DONE_DDC (pin K10) signal is asserted indicating the DLPR410 PROM has correctly programmed the DLPC410 FPGA.

10.3.2 Initialization

Initialization will automatically start after $\overline{\text{ARST}}$ (pin AC13) is deasserted. The initialization process includes the following components in the order presented here:

1. Calibration
2. DLPA200 number 1 Initialization (all DMDs)
3. DMD Initialization
4. DLPA200 number 2 Initialization (DLP9500 & DLP9500UV only)

Initialization Setup (continued)

5. Command Sequence

10.3.2.1 Calibration

Calibration is done on each of the data (DDC_DIN) and DVALID signal pairs using the training pattern (see *Interface Training Pattern*). When calibration is successful, the following signals will go high:

- ECP2_M_TP21 (pin G12) - input bank A calibration complete (all DMDs)
- ECP2_M_TP22 (pin E11) - input bank B calibration complete (all DMDs)
- ECP2_M_TP23 (pin E10) - input bank C calibration complete (DLP9500 & DLP9500UV only)
- ECP2_M_TP24 (pin E8) - input bank D calibration complete (DLP9500 & DLP9500UV only)

NOTE

The training pattern going into the SERDES on the transmit side is different than the pattern on the receive SERDES. On the receive side the value should be “0100”. However, this could translate to “0010” on the transmit side. Please see *Interface Training Pattern* for more information. An improper training pattern could cause the part to not perform the commands correctly.

10.3.2.2 DLPA200 Number 1 Initialization

DLPA200 number 1 is initialized for all DMDs. The DLPC410 output $\overline{\text{DAD\_A\_SCPEN}}$ (pin AE3) signal should be asserted indicating that the DLPC410 is ready to communicate with DLPA200 number 1. Toggling should be seen on SCPCLK (pin AB15), SCPDO (pin AA15 - SCP output from the DLPC410) and SCPDI (pin AA15 - SCP input to the DLPC410) lines. Be sure that the direction of the SCP input and output signals are connected correctly.

Table 13. DLPA200 Number 1 Initialization Status

ECP2_M_TP27 (PIN F8)	NOTE
1	DLPA200 number 1 initialization in progress
0	DLPA200 number 1 initialization complete

Check V_{BIAS}, V_{RESET}, and V_{OFFSET} voltage values on the DLPA200 number 1 and compare against the DLPA200 data sheet specifications for the particular DMD being used with the DLPC410.

10.3.2.3 DMD Initialization

The DLPC410 output $\overline{\text{DMD\_A\_SCPEN}}$ (pin AB14) signal should be asserted indicating that the DLPC410 is ready to communicate to the DMD. Toggling should be seen on SCPCLK (pin AB15), SCPDO (pin AA15 - SCP output from the DLPC410) and SCPDI (pin AA15 - SCP input to the DLPC410) lines. Be sure that the direction of the SCP input and output signals are connected correctly.

Table 14. DMD Initialization Status

ECP2_M_TP26 (PIN F9)	NOTE
1	DMD initialization in progress
0	DMD initialization complete

10.3.2.3.1 DMD Device ID Check

Check the four DMD_TYPE(3:0) pins (AA17, AC16, AB17, and AD15)) to see if the attached DMD type was correctly identified as listed in Table 2. DMD_TYPE will return 1111 if the DMD is not attached or not recognized.

10.3.2.3.2 DMD Device OK

NOTE

Only DMDs listed in Table 2 are supported by the DLPC410.

The signals ECP2_M_TP11 (pin AA10) and ECP2_M_TP12 (pin Y10) indicate the status of the DMD buses:

Table 15. DMD Device OK Status

ECP2_M_TP11 (PIN AA10 - A/B SIDE)	ECP2_M_TP12 (PIN Y10 - C/D SIDE)	NOTE
0	0	DMD not initialized or not supported
1	0	A/B side is attached and initialized. Expected for DLP7000 or DLP7000 UV (DLP9500 or DLP9500UV indicates a problem with C/D side)
0	1	Invalid output
1	1	All buses (A/B/C/D) are attached and initialized

10.3.2.4 DLPA200 Number 2 Initialization

DLPA200 number 2 is initialized only for DLP9500 and DLP9500UV DMDs. The DLPC410 output DAD_B_SCPEN (pin AB19) signal should be asserted indicating that the DLPC410 is ready to communicate with DLPA200 number 2. Toggling should be seen on SCPCLK (pin AB15), SCPDO (pin AA15 - SCP output from the DLPC410) and SCPDI (pin AA15 - SCP input to the DLPC410) lines. Be sure that the direction of the SCP input and output signals are connected correctly.

Table 16. DLPA200 Number 2 Initialization Status

ECP2_M_TP28 (pin G10)	NOTE
1	DLPA200 number 2 initialization in progress
0	DLPA200 number 2 initialization complete

Check V_{BIAS}, V_{RESET}, and V_{OFFSET} voltage values on the DLPA200 number 2 and compare against the DLPA200 data sheet specifications for the DLP9500 or DLP9500UV.

10.3.2.5 Command Sequence Initialization

The last portion of the initialization process involves a series of commands sent from the DLPC410 to the DMD. This will complete the initialization process.

During this step, check the output of the DLPA200(s). One should expect to see several Mirror Clocking Pulse waveforms indicating the DLPA200(s) is (are) initialized correctly.

At the end of the initialization sequence, if the initialization is successful, ECP2_M_TP20 (pin G11) will deassert (go low) indicating that the initialization process is complete.

Table 17. DLPC410 Initialization Status

ECP2_M_TP20 (pin G11)	NOTE
1	DLPC410 initialization in progress
0	DLPC410 initialization complete

NOTE

Initialization complete indicates that the initialization sequence of the DLPC410 has completed, but does not ensure that each step was completed correctly, only that it finished. For example the initialization of a DLPA200 may complete, but if the voltages set are incorrect further investigation is needed to uncover the reason.

10.3.3 Image Display Issues

There are three steps to displaying an image on the DMD, each of which can cause an image to fail to display correctly or in some case not at all. These steps are:

1. Generate Data – Pattern data generated by the users device.
2. Load Data to the DMD – Data is loaded from the DLPC410 into the attached CMOS memory array of the DMDs.
3. Issue Mirror Clocking Pulse – A mirror clocking pulse is issued to block(s) to change the state of the micromirrors based on the data loaded in step two. See *Mirror Clocking Pulse (Reset) and Float Operations*.

10.3.3.1 Generate Data

If there is a problem with the image displayed, one of the first places to check is the data generation. This portion is done outside of the DLPC410. Please see *Data and Command Write Cycle* for a description of how to send data to the DLPC410.

10.3.3.2 Load Data to DMD

After data and commands are sent to the DLPC410, the DLPC410 processes the information and passes the it to the DMD. If there is no image displayed, first check the data output and SCTRL lines of the DLPC410 to see if there is data coming out. Data output (DDC_DOUT...) and DDC_SCTRL pins can be found in the *Pin Configuration and Functions*.

PWR_FLOAT (pin AC17) will prevent the data from coming out of the DLPC410 if asserted. Check to make sure that it is at logic level 0.

A *Float blocks 00-15* command will also prevent data from the DLPC410. Please see the last entry of Table 9.

10.3.3.3 Mirror Clocking Pulse

For an image to display Mirror Clocking Pulses must be received by the block or blocks that have data loaded to the DMD memory array. Check DAD_A_STROBE (pin AF3) and DAD_B_STROBE (pin AB20) [if applicable] for pulses to verify that requests for mirror clocking pulses are being sent to the DLPA200(s). Also check the DLPA200(s) output is enabled by checking that DAD_OE (pin AF5) is low.

11 Power Supply Recommendations

11.1 Power Down Operation

For correct operation of the DMD, the following power down procedure must be executed. Prior to power removal, assert PWR_FLOAT and allow approximately 300 µs for the procedure to complete. This procedure will assure the mirrors are in a flat state, similar to the float operation. Following this procedure, the power can be safely removed.

To restart after assertion of PWR_FLOAT the DLPC410 must be reset ($\overline{\text{ARST}}$ low then high) or power must be cycled.

12 Layout

12.1 Layout Guidelines

The DLPC410 is part of a chipset that is controls a DLP7000 / DLP7000UV or DLP9500 / DLP9500UV DMD in conjunction with the DLPA200 driver(s). These guidelines are targeted at designing a PCB board with these components.

12.1.1 Impedance Requirements

Signals should be routed to have a matched impedance of 50 Ω ±10% except for LVDS differential pairs (DMD_DAT_Xnn, DMD_DCKL_Xn, and DMD_SCTRL_Xn), which should be matched to 100 Ω ±10% across each pair.

12.1.2 PCB Signal Routing

When designing a PCB board for the DLPC7000 / DLP7000UV or DLP9500 / DLP9500UV controlled by the DLPC410 in conjunction with the DLPA200(s), the following are recommended:

Signal trace corners should be no sharper than 45°. Adjacent signal layers should have the predominate traces routed orthogonal to each other. TI recommends that critical signals be hand routed in the following order: DDR2 Memory, DMD (LVDS signals), then DLPA200 signals.

TI does not recommend signal routing on power or ground planes.

TI does not recommend ground plane slots.

High speed signal traces should not cross over slots in adjacent power and/or ground planes.

Table 18. Important Signal Trace Constraints

SIGNAL	CONSTRAINTS
LVDS (DMD_DAT_xnn, DMD_DCKL_xn, and DMD_SCTRL_xn)	P-to-N data, clock, and SCTRL: <10 mils (0.25 mm); Pair-to-pair <10 mils (0.25 mm); Bundle-to-bundle <2000 mils (50 mm, for example DMD_DAT_Ann to DMD_DAT_Bnn) Trace width: 4 mil (0.1 mm) Trace spacing: In ball field – 4 mil (0.11 mm); PCB etch – 14 mil (0.36 mm) Maximum recommended trace length <6 inches (150 mm)

Table 19. Power Trace Widths and Spacing

SIGNAL NAME	MINIMUM TRACE WIDTH	MINIMUM TRACE SPACING	LAYOUT REQUIREMENTS
GND	Maximize	5 mil (0.13 mm)	Maximize trace width to connecting pin as a minimum
P2P5V, P1P0V	50 mil (1.3 mm)	10 mil (0.25 mm)	Create mini planes and connect to devices as necessary with multiple vias
P2P5V, P1P0V	30 mil (0.76 mm) - stub width	10 mil (0.25 mm)	Stub width to connecting IC pins; maximize width when possible

12.1.3 Fiducials

Fiducials for automatic component insertion should be 0.05-inch copper with a 0.1-inch cutout (antipad). Fiducials for optical auto insertion are placed on three corners of both sides of the PCB.

12.1.4 PCB Layout Guidelines

A target impedance of 50 Ω for single ended signals and 100 Ω between LVDS signals is specified for all signal layers.

12.1.4.1 DMD Interface

The digital interface from the DLPC410 to the DMD are LVDS signals that run at clock rates up to 400 MHz. Data is clocked into the DMD on both the rising and falling edge of the clock, so the data rate is 800 MHz. The LVDS signals should have 100-Ω differential impedance. The differential signals should be matched but kept as short as possible. Parallel termination at the LVDS receiver is in the DMD; therefore, on board termination is not necessary.

12.1.4.1.1 Trace Length Matching

The DLPC410 DMD data signals require precise length matching. Differential signals should have impedance of 100 Ω (with 5% tolerance). It is important that the propagation delays are matched. The maximum differential pair uncoupled length is 150 mils with a relative propagation delay of ±25 mil between the p and n. Matching all signals exactly will maximize the channel margin. The signal path through all boards, flex cables and internal DMD routing must be considered in this calculation.

12.1.4.2 DLPC410 DMD Decoupling

General decoupling capacitors for the DLPC410 DMD should be distributed around the PCB and placed to minimize the distance from IC voltage and ground pads. Each decoupling capacitor (0.1 µF recommended) should have vias directly to the ground and power planes. Via sharing between components (discreet or integrated) is discouraged. The power and ground pads of the DLPC410 DMD should be tied to the voltage and ground planes with their own vias.

12.1.4.2.1 Decoupling Capacitors

Decoupling capacitors should be placed to minimize the distance from the decoupling capacitor to the supply and ground pin of the component. It is recommended that the placement of and routing for the decoupling capacitors meet the following guidelines:

- The supply voltage pin of the capacitor should be located close to the device supply voltage pin(s). The decoupling capacitor should have vias to ground and voltage planes. The device can be connected directly to the decoupling capacitor (no via) if the trace length is less than 0.1 inch. Otherwise, the component should be tied to the voltage or ground plane through separate vias.
- The trace lengths of the voltage and ground connections for decoupling capacitors and components should be less than 0.1 inch to minimize inductance.
- The trace width of the power and ground connection to decoupling capacitors and components should be as wide as possible to minimize inductance.
- Connecting decoupling capacitors to ground and power planes through multiple vias can reduce inductance and improve noise performance.
- Decoupling performance can be improved by utilizing low ESR and low ESL capacitors.

12.1.4.3 VCC and VCC2

The VCC pins of the DMD should be connected directly to the DMD VCC plane. Decoupling for the VCC should be distributed around the DMD and placed to minimize the distance from the voltage and ground pads. Each decoupling capacitor should have vias directly connected to the ground and power planes. The VCC and GND pads of the DMD should be tied to the VCC and ground planes with their own vias.

The VCC2 voltage can be routed to the DMD as a trace. Decoupling capacitors should be placed to minimize the distance from the VCC2 and ground pads of the DMD. Using wide etch from the decoupling capacitors to the DMD connection will reduce inductance and improve decoupling performance.

12.1.4.4 DMD Layout

See the respective sections in this data sheet for package dimensions, timing and pin out information.

12.1.4.5 DLPA200

The DLPA200 generates the micromirror clocking pulses for the DMD. The DMD-drive outputs from the DLPA200 should be routed with minimum trace width of 11 mil and a minimum spacing of 15 mil. The VCC and VCC2 traces from the output capacitors to the DLPA200 should also be routed with a minimum trace width and spacing of 11 mil and 15 mil, respectively. See the DLPA200 customer data sheet for mechanical package and layout information.

12.2 Layout Example

For LVDS (and other differential signal) pairs and groups, it is important to match trace lengths. In the area of the dashed lines, Figure 21 shows correct matching of signal pair lengths with serpentine sections to maintain the correct impedance.

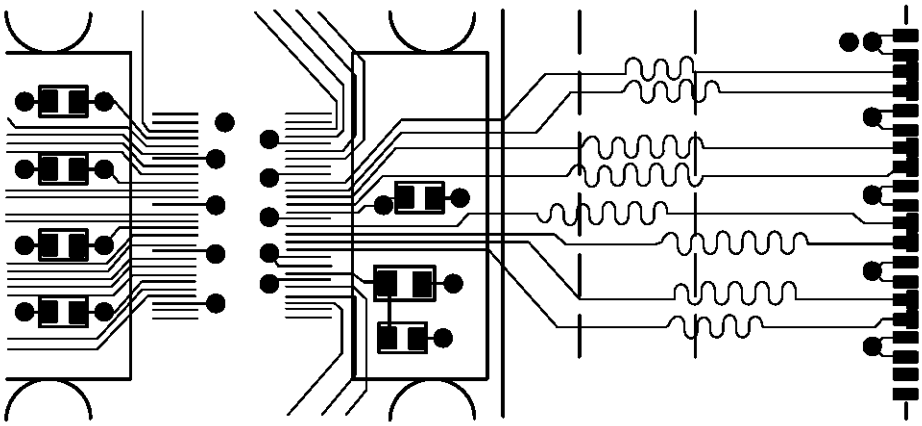


Figure 21. Mitering LVDS Traces to Match Lengths

12.3 DLPC410 Chipset Connections

The following tables list the signal connections between components of the Chipset when used with the DLP7000 / DLP700UV DMD and with the DLP9500 / DLP9500UV DMD. These tables do not include power, ground, pull-up, pull-down, termination, or any other connection requirements. Please see the Pin Functions table in the respective data sheet of each chipset component for connection requirements.

Table 20. DLPC410 Chipset Connections with the DLP7000

DLPC410 (CONTROLLER)		DLPR410 (PROM)		DLPA200 (MICROMIRROR DRIVER)		DLP7000 / UV (DMD)	
PIN		PIN		PIN		PIN	
NAME	NO.	NAME	NO.	NAME	NO.	NAME	NO.
DONE_DDC	K10	$\overline{CE}$	B4				
INTB_DDC	J11	OE/$\overline{RESET}$	A3				
PROGB_DDC	J18	$\overline{CF}$	D1				
PROM_CCK_DDC	J10	CLKOUT	C2				
PROM_D0_DDC	K11	D0	H6				
TCK_JTAG	U11	TCK	H3				
TDO_XCF16DDC	V11	TDO	E6				
TMS_JTAG	V12	TMS	E2				
DAD_A_ADDR0	E1			ADDR0	19		
DAD_A_ADDR1	E2			ADDR1	18		
DAD_A_ADDR2	E3			ADDR2	17		
DAD_A_ADDR3	F3			ADDR3	16		
DAD_A_MODE0	C1			MODE0	3		
DAD_A_MODE1	D1			MODE1	2		
DAD_A_SEL0	AB12			SEL0	5		
DAD_A_SEL1	AC12			SEL1	4		
DAD_A_STROBE	AF3			STROBE	15		
DAD_INIT	AF4			$\overline{RESET}$	59		
$\overline{DAD\_OE}$	AF5			$\overline{OE}$	6		
$\overline{DAD\_A\_SCPEN}$	AE3			$\overline{SCPEN}$	58		
SCPCLK	AB15			SCPCLK	56	SCPCLK	E3
SCPDI	AA15			SCPDO	57	SCPDO	B2
SCPDO	AA14			SCPDI	42	SCPDI	F4
$\overline{DMD\_A\_SCPEN}$	AB14					$\overline{SCPEN}$	D4
DMD_A_RESET	AD14					$\overline{PWRDN}$	C3
DDC_DCLKOUT_A_DPN	N1					DCLK_AN	B22
DDC_DCLKOUT_A_DPP	M1					DCLK_AP	B24
DDC_DCLKOUT_B_DPN	Y5					DCLK_BN	AB22
DDC_DCLKOUT_B_DPP	Y6					DCLK_BP	AB24
DDC_DOUT_A0_DPN	AE2					D_AN(0)	B10
DDC_DOUT_A0_DPP	AF2					D_AP(0)	B12
DDC_DOUT_A1_DPN	AD1					D_AN(1)	A13
DDC_DOUT_A1_DPP	AE1					D_AP(1)	A11
DDC_DOUT_A2_DPN	AC1					D_AN(2)	D16
DDC_DOUT_A2_DPP	AC2					D_AP(2)	D14
DDC_DOUT_A3_DPN	AB1					D_AN(3)	C17
DDC_DOUT_A3_DPP	AB2					D_AP(3)	C15
DDC_DOUT_A4_DPN	Y2					D_AN(4)	B18
DDC_DOUT_A4_DPP	AA2					D_AP(4)	B16

DLPC410 Chipset Connections (continued)

Table 20. DLPC410 Chipset Connections with the DLP7000 (continued)

DLPC410 (CONTROLLER)		DLPR410 (PROM)		DLPA200 (MICROMIRROR DRIVER)		DLP7000 / UV (DMD)	
PIN		PIN		PIN		PIN	
NAME	NO.	NAME	NO.	NAME	NO.	NAME	NO.
DDC_DOUT_A5_DPN	W1					D_AN(5)	A17
DDC_DOUT_A5_DPP	Y1					D_AP(5)	A19
DDC_DOUT_A6_DPN	V1					D_AN(6)	A25
DDC_DOUT_A6_DPP	V2					D_AP(6)	A23
DDC_DOUT_A7_DPN	U1					D_AN(7)	D22
DDC_DOUT_A7_DPP	U2					D_AP(7)	D20
DDC_DOUT_A8_DPN	R2					D_AN(8)	C29
DDC_DOUT_A8_DPP	T2					D_AP(8)	A29
DDC_DOUT_A9_DPN	N2					D_AN(9)	D28
DDC_DOUT_A9_DPP	M2					D_AP(9)	B28
DDC_DOUT_A10_DPN	K1					D_AN(10)	E27
DDC_DOUT_A10_DPP	L2					D_AP(10)	C27
DDC_DOUT_A11_DPN	K2					D_AN(11)	F26
DDC_DOUT_A11_DPP	K3					D_AP(11)	D26
DDC_DOUT_A12_DPN	J3					D_AN(12)	G29
DDC_DOUT_A12_DPP	H3					D_AP(12)	F30
DDC_DOUT_A13_DPN	H2					D_AN(13)	H28
DDC_DOUT_A13_DPP	J1					D_AP(13)	H30
DDC_DOUT_A14_DPN	H1					D_AN(14)	J27
DDC_DOUT_A14_DPP	G1					D_AP(14)	J29
DDC_DOUT_A15_DPN	G2					D_AN(15)	K26
DDC_DOUT_A15_DPP	F2					D_AP(15)	K28
DDC_DOUT_B0_DPN	AE5					D_BN(0)	AB10
DDC_DOUT_B0_DPP	AE6					D_BP(0)	AB12
DDC_DOUT_B1_DPN	AD3					D_BN(1)	AC13
DDC_DOUT_B1_DPP	AD4					D_BP(1)	AC11
DDC_DOUT_B2_DPN	AD5					D_BN(2)	Y16
DDC_DOUT_B2_DPP	AD6					D_BP(2)	Y14
DDC_DOUT_B3_DPN	AC3					D_BN(3)	AA17
DDC_DOUT_B3_DPP	AC4					D_BP(3)	AA15
DDC_DOUT_B4_DPN	AB5					D_BN(4)	AB18
DDC_DOUT_B4_DPP	AB6					D_BP(4)	AB16
DDC_DOUT_B5_DPN	AB7					D_BN(5)	AC17
DDC_DOUT_B5_DPP	AC6					D_BP(5)	AC19
DDC_DOUT_B6_DPN	AA5					D_BN(6)	AC25
DDC_DOUT_B6_DPP	AA4					D_BP(6)	AC23
DDC_DOUT_B7_DPN	AA7					D_BN(7)	Y22
DDC_DOUT_B7_DPP	Y7					D_BP(7)	Y20
DDC_DOUT_B8_DPN	Y3					D_BN(8)	AA29
DDC_DOUT_B8_DPP	W3					D_BP(8)	AC29
DDC_DOUT_B9_DPN	W4					D_BN(9)	Y28
DDC_DOUT_B9_DPP	V4					D_BP(9)	AB28
DDC_DOUT_B10_DPN	W6					D_BN(10)	W27

DLPC410 Chipset Connections (continued)

Table 20. DLPC410 Chipset Connections with the DLP7000 (continued)

DLPC410 (CONTROLLER)		DLPR410 (PROM)		DLPA200 (MICROMIRROR DRIVER)		DLP7000 / UV (DMD)	
PIN		PIN		PIN		PIN	
NAME	NO.	NAME	NO.	NAME	NO.	NAME	NO.
DDC_DOUT_B10_DPP	W5					D_BP(10)	AA27
DDC_DOUT_B11_DPN	V7					D_BN(11)	V26
DDC_DOUT_B11_DPP	V6					D_BP(11)	Y26
DDC_DOUT_B12_DPN	U4					D_BN(12)	T30
DDC_DOUT_B12_DPP	V3					D_BP(12)	U29
DDC_DOUT_B13_DPN	T4					D_BN(13)	R29
DDC_DOUT_B13_DPP	T5					D_BP(13)	T28
DDC_DOUT_B14_DPN	U6					D_BN(14)	R27
DDC_DOUT_B14_DPP	U5					D_BP(14)	P28
DDC_DOUT_B15_DPN	U7					D_BN(15)	N27
DDC_DOUT_B15_DPP	T7					D_BP(15)	P26
DDC_SCTRL_AN	R1					SCTRL_AN	C21
DDC_SCTRL_AP	P1					SCTRL_AP	C23
DDC_SCTRL_BN	AA3					SCTRL_BN	AA21
DDC_SCTRL_BP	AB4					SCTRL_BP	AA23

Table 21. DLPC410 Chipset Connections with the DLP9500

DLPC410 (CONTROLLER)		DLPR410 (PROM)		DLPA200 Number 1 (MICROMIRROR DRIVER)		DLPA200 Number 2 (MICROMIRROR DRIVER)		DLP9500 or UV (DMD)	
PIN		PIN		PIN		PIN		PIN	
NAME	NO.	NAME	NO.	NAME	NO.	NAME	NO.	NAME	NO.
DONE_DDC	K10	$\overline{CE}$	B4						
INTB_DDC	J11	OE/$\overline{RESET}$	A3						
PROGB_DDC	J18	$\overline{CF}$	D1						
PROM_CCK_DDC	J10	CLKOUT	C2						
PROM_D0_DDC	K11	D0	H6						
TCK_JTAG	U11	TCK	H3						
TDO_XCF16DDC	V11	TDO	E6						
TMS_JTAG	V12	TMS	E2						
DAD_A_ADDR0	E1			ADDR0	19				
DAD_A_ADDR1	E2			ADDR1	18				
DAD_A_ADDR2	E3			ADDR2	17				
DAD_A_ADDR3	F3			ADDR3	16				
DAD_A_MODE0	C1			MODE0	3				
DAD_A_MODE1	D1			MODE1	2				
DAD_A_SEL0	AB12			SEL0	5				
DAD_A_SEL1	AC12			SEL1	4				
DAD_A_STROBE	AF3			STROBE	15				
DAD_B_ADDR0	E26					ADDR0	19		
DAD_B_ADDR1	E25					ADDR1	18		
DAD_B_ADDR2	F25					ADDR2	17		
DAD_B_ADDR3	F24					ADDR3	16		
DAD_B_MODE0	D26					MODE0	3		
DAD_B_MODE1	D25					MODE1	2		
DAD_B_SEL0	R22					SEL0	5		
DAD_B_SEL1	R23					SEL1	4		
DAD_B_STROBE	AB20					STROBE	15		
DAD_INIT	AF4			$\overline{RESET}$	59	$\overline{RESET}$	59		
$\overline{DAD\_OE}$	AF5			$\overline{OE}$	6	$\overline{OE}$	6		
$\overline{DAD\_A\_SCPEN}$	AE3			$\overline{SCPEN}$	58				
$\overline{DAD\_B\_SCPEN}$	AB19					$\overline{SCPEN}$	58		
SCPCLK	AB15			SCPCLK	56	SCPCLK	56	SCPCLK	AE1
SCPDI	AA15			SCPDO	57	SCPDO	57	SCPDO	AC3
SCPDO	AA14			SCPDI	42	SCPDI	42	SCPDI	AD2
$\overline{DMD\_A\_SCPEN}$	AB14							$\overline{SCPEN}$	AD4
DMD_A_RESET	AD14							$\overline{PWRDN}$	B4
DDC_DCLKOUT_A_DPN	N1							DCLK_AN	D10
DDC_DCLKOUT_A_DPP	M1							DCLK_AP	D8
DDC_DCLKOUT_B_DPN	Y5							DCLK_BN	AJ11
DDC_DCLKOUT_B_DPP	Y6							DCLK_BP	AJ9
DDC_DCLKOUT_C_DPN	AA22							DCLK_CN	C23
DDC_DCLKOUT_C_DPP	AB22							DCLK_CP	C21
DDC_DCLKOUT_D_DPN	M26							DCLK_DN	AJ23
DDC_DCLKOUT_D_DPP	M25							DCLK_DP	AJ21
DDC_DOUT_A0_DPN	AE2							D_AN(0)	F2

Table 21. DLPC410 Chipset Connections with the DLP9500 (continued)

DLPC410 (CONTROLLER)		DLPR410 (PROM)		DLPA200 Number 1 (MICROMIRROR DRIVER)		DLPA200 Number 2 (MICROMIRROR DRIVER)		DLP9500 or UV (DMD)	
PIN		PIN		PIN		PIN		PIN	
NAME	NO.	NAME	NO.	NAME	NO.	NAME	NO.	NAME	NO.
DDC_DOUT_A0_DPP	AF2							D_AP(0)	F4
DDC_DOUT_A1_DPN	AD1							D_AN(1)	H8
DDC_DOUT_A1_DPP	AE1							D_AP(1)	H10
DDC_DOUT_A2_DPN	AC1							D_AN(2)	E5
DDC_DOUT_A2_DPP	AC2							D_AP(2)	E3
DDC_DOUT_A3_DPN	AB1							D_AN(3)	G9
DDC_DOUT_A3_DPP	AB2							D_AP(3)	G11
DDC_DOUT_A4_DPN	Y2							D_AN(4)	D2
DDC_DOUT_A4_DPP	AA2							D_AP(4)	D4
DDC_DOUT_A5_DPN	W1							D_AN(5)	G3
DDC_DOUT_A5_DPP	Y1							D_AP(5)	G5
DDC_DOUT_A6_DPN	V1							D_AN(6)	E11
DDC_DOUT_A6_DPP	V2							D_AP(6)	E9
DDC_DOUT_A7_DPN	U1							D_AN(7)	F8
DDC_DOUT_A7_DPP	U2							D_AP(7)	F10
DDC_DOUT_A8_DPN	R2							D_AN(8)	C9
DDC_DOUT_A8_DPP	T2							D_AP(8)	C11
DDC_DOUT_A9_DPN	N2							D_AN(9)	H2
DDC_DOUT_A9_DPP	M2							D_AP(9)	H4
DDC_DOUT_A10_DPN	K1							D_AN(10)	B10
DDC_DOUT_A10_DPP	L2							D_AP(10)	B8
DDC_DOUT_A11_DPN	K2							D_AN(11)	G15
DDC_DOUT_A11_DPP	K3							D_AP(11)	H14
DDC_DOUT_A12_DPN	J3							D_AN(12)	D14
DDC_DOUT_A12_DPP	H3							D_AP(12)	D16
DDC_DOUT_A13_DPN	H2							D_AN(13)	F14
DDC_DOUT_A13_DPP	J1							D_AP(13)	F16
DDC_DOUT_A14_DPN	H1							D_AN(14)	C17
DDC_DOUT_A14_DPP	G1							D_AP(14)	C15
DDC_DOUT_A15_DPN	G2							D_AN(15)	H16
DDC_DOUT_A15_DPP	F2							D_AP(15)	G17
DDC_DOUT_B0_DPN	AE5							D_BN(0)	AH2
DDC_DOUT_B0_DPP	AE6							D_BP(0)	AH4
DDC_DOUT_B1_DPN	AD3							D_BN(1)	AD8
DDC_DOUT_B1_DPP	AD4							D_BP(1)	AD10
DDC_DOUT_B2_DPN	AD5							D_BN(2)	AJ5
DDC_DOUT_B2_DPP	AD6							D_BP(2)	AJ3
DDC_DOUT_B3_DPN	AC3							D_BN(3)	AE3
DDC_DOUT_B3_DPP	AC4							D_BP(3)	AE5
DDC_DOUT_B4_DPN	AB5							D_BN(4)	AG9
DDC_DOUT_B4_DPP	AB6							D_BP(4)	AG11
DDC_DOUT_B5_DPN	AB7							D_BN(5)	AE11
DDC_DOUT_B5_DPP	AC6							D_BP(5)	AE9
DDC_DOUT_B6_DPN	AA5							D_BN(6)	AH10

Table 21. DLPC410 Chipset Connections with the DLP9500 (continued)

DLPC410 (CONTROLLER)		DLPR410 (PROM)		DLPA200 Number 1 (MICROMIRROR DRIVER)		DLPA200 Number 2 (MICROMIRROR DRIVER)		DLP9500 or UV (DMD)	
PIN		PIN		PIN		PIN		PIN	
NAME	NO.	NAME	NO.	NAME	NO.	NAME	NO.	NAME	NO.
DDC_DOUT_B6_DPP	AA4							D_BP(6)	AH8
DDC_DOUT_B7_DPN	AA7							D_BN(7)	AF10
DDC_DOUT_B7_DPP	Y7							D_BP(7)	AF8
DDC_DOUT_B8_DPN	Y3							D_BN(8)	AK8
DDC_DOUT_B8_DPP	W3							D_BP(8)	AK10
DDC_DOUT_B9_DPN	W4							D_BN(9)	AG5
DDC_DOUT_B9_DPP	V4							D_BP(9)	AG3
DDC_DOUT_B10_DPN	W6							D_BN(10)	AL11
DDC_DOUT_B10_DPP	W5							D_BP(10)	AL9
DDC_DOUT_B11_DPN	V7							D_BN(11)	AE15
DDC_DOUT_B11_DPP	V6							D_BP(11)	AD14
DDC_DOUT_B12_DPN	U4							D_BN(12)	AH14
DDC_DOUT_B12_DPP	V3							D_BP(12)	AH16
DDC_DOUT_B13_DPN	T4							D_BN(13)	AF14
DDC_DOUT_B13_DPP	T5							D_BP(13)	AF16
DDC_DOUT_B14_DPN	U6							D_BN(14)	AJ17
DDC_DOUT_B14_DPP	U5							D_BP(14)	AJ15
DDC_DOUT_B15_DPN	U7							D_BN(15)	AD16
DDC_DOUT_B15_DPP	T7							D_BP(15)	AE17
DDC_DOUT_C0_DPN	T22							D_CN(0)	B14
DDC_DOUT_C0_DPP	T23							D_CP(0)	B16
DDC_DOUT_C1_DPN	R20							D_CN(1)	E15
DDC_DOUT_C1_DPP	R21							D_CP(1)	E17
DDC_DOUT_C2_DPN	T19							D_CN(2)	A17
DDC_DOUT_C2_DPP	T20							D_CP(2)	A15
DDC_DOUT_C3_DPN	U21							D_CN(3)	G21
DDC_DOUT_C3_DPP	U22							D_CP(3)	H20
DDC_DOUT_C4_DPN	U20							D_CN(4)	B20
DDC_DOUT_C4_DPP	U19							D_CP(4)	B22
DDC_DOUT_C5_DPN	V23							D_CN(5)	F20
DDC_DOUT_C5_DPP	V24							D_CP(5)	F22
DDC_DOUT_C6_DPN	V22							D_CN(6)	D22
DDC_DOUT_C6_DPP	V21							D_CP(6)	D20
DDC_DOUT_C7_DPN	W19							D_CN(7)	G23
DDC_DOUT_C7_DPP	V19							D_CP(7)	H22
DDC_DOUT_C8_DPN	W23							D_CN(8)	B26
DDC_DOUT_C8_DPP	W24							D_CP(8)	B28
DDC_DOUT_C9_DPN	Y22							D_CN(9)	F28
DDC_DOUT_C9_DPP	Y23							D_CP(9)	F26
DDC_DOUT_C10_DPN	Y20							D_CN(10)	C29
DDC_DOUT_C10_DPP	Y21							D_CP(10)	C27
DDC_DOUT_C11_DPN	AA24							D_CN(11)	G27
DDC_DOUT_C11_DPP	AA23							D_CP(11)	G29
DDC_DOUT_C12_DPN	AA19							D_CN(12)	D26

Table 21. DLPC410 Chipset Connections with the DLP9500 (continued)

DLPC410 (CONTROLLER)		DLPR410 (PROM)		DLPA200 Number 1 (MICROMIRROR DRIVER)		DLPA200 Number 2 (MICROMIRROR DRIVER)		DLP9500 or UV (DMD)	
PIN		PIN		PIN		PIN		PIN	
NAME	NO.	NAME	NO.	NAME	NO.	NAME	NO.	NAME	NO.
DDC_DOUT_C12_DPP	AA20							D_CP(12)	D28
DDC_DOUT_C13_DPN	AC24							D_CN(13)	H28
DDC_DOUT_C13_DPP	AB24							D_CP(13)	H26
DDC_DOUT_C14_DPN	AC19							D_CN(14)	E29
DDC_DOUT_C14_DPP	AD19							D_CP(14)	E27
DDC_DOUT_C15_DPN	AC22							D_CN(15)	J29
DDC_DOUT_C15_DPP	AC23							D_CP(15)	J27
DDC_DOUT_D0_DPN	AB26							D_DN(0)	AK14
DDC_DOUT_D0_DPP	AC26							D_DP(0)	AK16
DDC_DOUT_D1_DPN	AA25							D_DN(1)	AG15
DDC_DOUT_D1_DPP	AB25							D_DP(1)	AG17
DDC_DOUT_D2_DPN	Y26							D_DN(2)	AL17
DDC_DOUT_D2_DPP	Y25							D_DP(2)	AL15
DDC_DOUT_D3_DPN	W26							D_DN(3)	AE21
DDC_DOUT_D3_DPP	W25							D_DP(3)	AD20
DDC_DOUT_D4_DPN	U26							D_DN(4)	AK20
DDC_DOUT_D4_DPP	V26							D_DP(4)	AK22
DDC_DOUT_D5_DPN	U25							D_DN(5)	AF20
DDC_DOUT_D5_DPP	U24							D_DP(5)	AF22
DDC_DOUT_D6_DPN	T25							D_DN(6)	AH22
DDC_DOUT_D6_DPP	T24							D_DP(6)	AH20
DDC_DOUT_D7_DPN	R26							D_DN(7)	AE23
DDC_DOUT_D7_DPP	R25							D_DP(7)	AD22
DDC_DOUT_D8_DPN	P24							D_DN(8)	AK26
DDC_DOUT_D8_DPP	P25							D_DP(8)	AK28
DDC_DOUT_D9_DPN	N24							D_DN(9)	AF28
DDC_DOUT_D9_DPP	M24							D_DP(9)	AF26
DDC_DOUT_D10_DPN	L25							D_DN(10)	AJ29
DDC_DOUT_D10_DPP	L24							D_DP(10)	AJ27
DDC_DOUT_D11_DPN	K26							D_DN(11)	AE27
DDC_DOUT_D11_DPP	K25							D_DP(11)	AE29
DDC_DOUT_D12_DPN	J26							D_DN(12)	AH26
DDC_DOUT_D12_DPP	J25							D_DP(12)	AH28
DDC_DOUT_D13_DPN	J24							D_DN(13)	AD28
DDC_DOUT_D13_DPP	H24							D_DP(13)	AD26
DDC_DOUT_D14_DPN	H26							D_DN(14)	AG29
DDC_DOUT_D14_DPP	G26							D_DP(14)	AG27
DDC_DOUT_D15_DPN	G25							D_DN(15)	AC29
DDC_DOUT_D15_DPP	G24							D_DP(15)	AC27
DDC_SCTRL_AN	R1							SCTRL_AN	J3
DDC_SCTRL_AP	P1							SCTRL_AP	J5
DDC_SCTRL_BN	AA3							SCTRL_BN	AF4
DDC_SCTRL_BP	AB4							SCTRL_BP	AF2
DDC_SCTRL_CN	W20							SCTRL_CN	E23

Table 21. DLPC410 Chipset Connections with the DLP9500 (continued)

DLPC410 (CONTROLLER)		DLPR410 (PROM)		DLPA200 Number 1 (MICROMIRROR DRIVER)		DLPA200 Number 2 (MICROMIRROR DRIVER)		DLP9500 or UV (DMD)	
PIN		PIN		PIN		PIN		PIN	
NAME	NO.	NAME	NO.	NAME	NO.	NAME	NO.	NAME	NO.
DDC_SCTRL_CP	W21							SCTRL_CP	E21
DDC_SCTRL_DN	N26							SCTRL_DN	AG23
DDC_SCTRL_DP	P26							SCTRL_DP	AG21

13 Device and Documentation Support

13.1 Device Support

13.1.1 Device Marking

Figure 22 is representative of the Xilinx XC5VLX30 FPGA configured for the DLPC410 device.

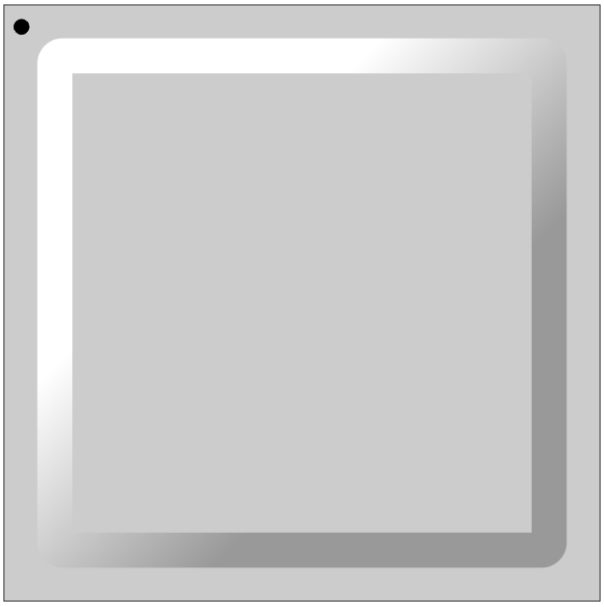


Figure 22. Diagram of the Xilinx XC5VLX30 FGPA

Figure 23 provides a legend for reading the Xilinx device marking for this DLP device.

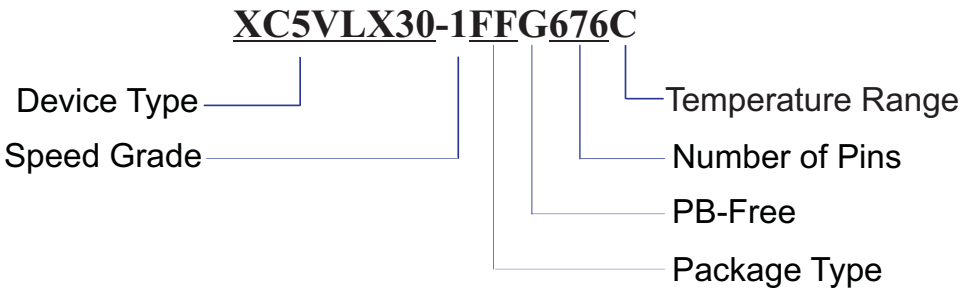


Figure 23. Legend

13.1.2 Device Nomenclature

Figure 24 provides a legend of reading the complete device name for any DLP device. The DLPC410ZYR is functionally equivalent to TI part number 2510440-001.

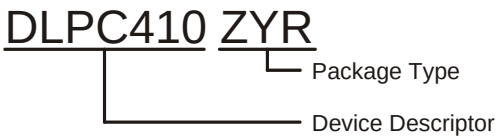


Figure 24. Device Nomenclature

13.2 Documentation Support

13.2.1 Related Documentation

Table 22. Related Documentation

DOCUMENT	TI LITERATURE NUMBER
DLP7000 0.7 XGA Type-A DMD data sheet	DLPS026
DLP7000UV 0.7 XGA UV Type-A DMD data sheet	DLPS061
DLP9500 0.95 1080p Type-A DMD data sheet	DLPS025
DLP9500UV 0.95 1080p UV Type-A DMD data sheet	DLPS033
DLPA200 DMD Micromirror Driver data sheet	DLPS015
DLPR410 EEPROM data sheet	DLPS027

13.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.4 Trademarks

E2E is a trademark of Texas Instruments.
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All other trademarks are the property of their respective owners.

13.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DLPC410ZYR	ACTIVE	FCBGA	ZYR	676	1	Pb-Free (RoHS)	Call TI	Level-4-250C-72 HRS			Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

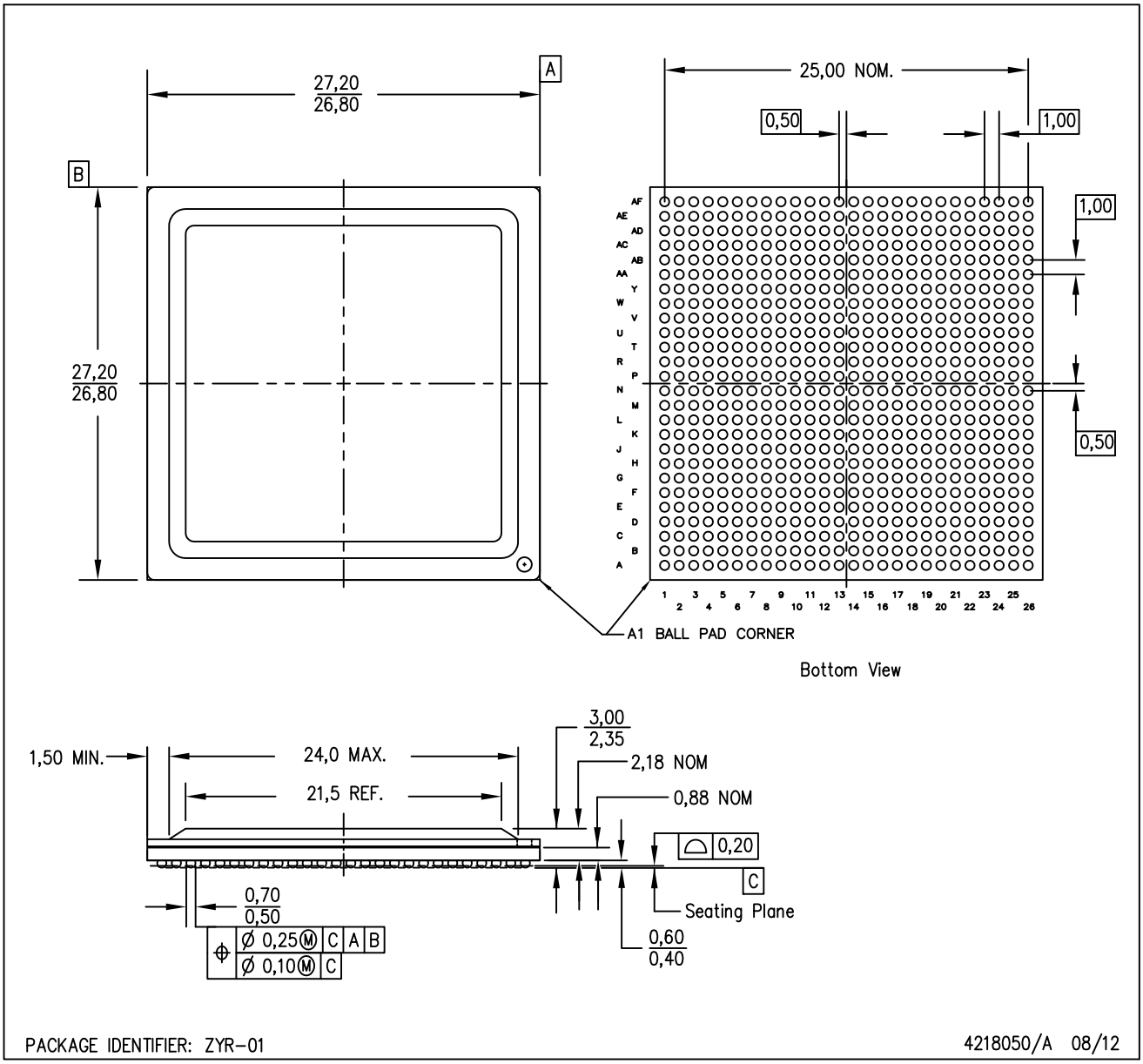
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

ZYR (S–PBGA–N676) PLASTIC BALL GRID ARRAY



PACKAGE IDENTIFIER: ZYR–01 4218050/A 08/12

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Flip chip application only.
D. Pb–free solder ball.

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