

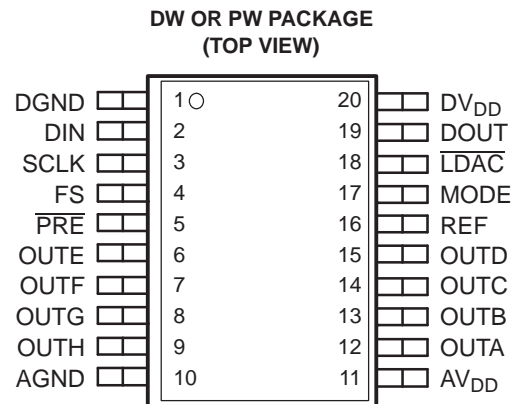
8-CHANNEL, 12-/10-/8-BIT, 2.7-V TO 5.5-V LOW POWER DIGITAL-TO-ANALOG CONVERTERS WITH POWER DOWN AND INTERNAL REFERENCE

FEATURES

- Eight Voltage Output DACs in One Package
 - TLV5630 . . . 12-Bit
 - TLV5631 . . . 10-Bit
 - TLV5632 . . . 8-Bit
 - 1 μ s in Fast Mode
 - 3 μ s in Slow Mode
- Programmable Settling Time vs Power Consumption
 - 1 μ s in Fast Mode
 - 3 μ s in Slow Mode
 - 18 mW in Slow Mode at 3 V
 - 48 mW in Fast Mode at 3 V
- Compatible With TMS320 and SPI Serial Ports
- Monotonic Over Temperature
- Low Power Consumption:
 - 18 mW in Slow Mode at 3 V
 - 48 mW in Fast Mode at 3 V
- Power-Down Mode
- Internal Reference
- Data Output for Daisy-Chaining

APPLICATIONS

- Digital Servo Control Loops
- Digital Offset and Gain Adjustment
- Industrial Process Control
- Machine and Motion Control Devices
- Mass Storage Devices



DESCRIPTION

The TLV5630, TLV5631, and TLV5632 are pin-compatible, eight-channel, 12-/10-/8-bit voltage output DACs each with a flexible serial interface. The serial interface allows glueless interface to TMS320 and SPI, QSPI, and Microwire serial ports. It is programmed with a 16-bit serial string containing 4 control and 12 data bits.

Additional features are a power-down mode, an $\overline{\text{LDAC}}$ input for simultaneous update of all eight DAC outputs, and a data output which can be used to cascade multiple devices, and an internal programmable band-gap reference.

The resistor string output voltage is buffered by a rail-to-rail output amplifier with a programmable settling time to allow the designer to optimize speed vs power dissipation. The buffered, high-impedance reference input can be connected to the supply voltage.

Implemented with a CMOS process, the DACs are designed for single-supply operation from 2.7 V to 5.5 V, and can operate on two separate analog and digital power supplies. The devices are available in 20-pin SOIC and TSSOP packages.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

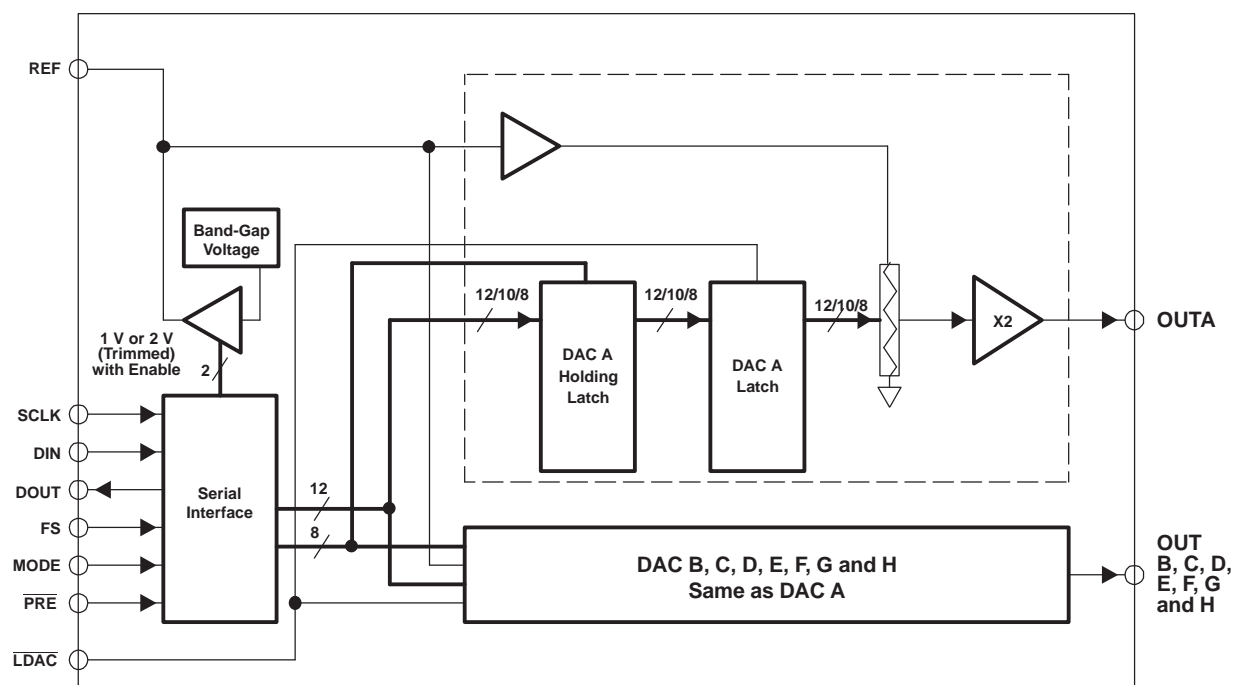


These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

AVAILABLE OPTIONS

T _A	PACKAGE		
	SOIC (DW)	TSSOP (PW)	RESOLUTION
40°C to 85°C	TLV5630IDW	TLV5630IPW	12
	TLV5631IDW	TLV5631IPW	10
	TLV5632IDW	TLV5632IPW	8

FUNCTIONAL BLOCK DIAGRAM



Terminal Functions

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
AGND	10	P	Analog ground
AV _{DD}	11	P	Analog power supply
DGND	1	P	Digital ground
DIN	2	I	Digital serial data input
DOUT	19	O	Digital serial data output
DV _{DD}	20	P	Digital power supply
FS	4	I	Frame sync input
$\overline{\text{LDAC}}$	18	I	Load DAC. The DAC outputs are only updated, if this signal is low. It is an asynchronous input.
MODE	17	I	DSP/ μ C mode pin. High = μ C mode, NC = DSP mode.
$\overline{\text{PRE}}$	5	I	Preset input
REF	16	I/O	Voltage reference input/output
SCLK	3	I	Serial clock input
OUTA-OUTH	12-15, 6-9	O	DAC outputs A, B, C, D, E, F, G and H

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature (unless otherwise noted) ⁽¹⁾

	UNIT
Supply voltage, (AV _{DD} , DV _{DD} to GND)	7 V
Reference input voltage range	- 0.3 V to AV _{DD} + 0.3
Digital input voltage range	- 0.3 V to DV _{DD} + 0.3
Operating free-air temperature range, T _A	-40°C to 85°C
Storage temperature range, T _{stg}	-65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

- (1) Stresses beyond those listed under „absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under „recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

		MIN	TYP	MAX	UNIT
Supply voltage, AV _{DD} , DV _{DD}	5-V operation	4.5	5	5.5	V
	3-V operation	2.7	3	3.3	V
High-level digital input, V _{IH}	DV _{DD} = 2.7 V	2			V
	DV _{DD} = 5.5 V	2.4			
Low-level digital input, V _{IL}	DV _{DD} = 2.7 V			0.6	V
	DV _{DD} = 5.5 V			1.0	
Reference voltage, V _{ref}	AV _{DD} = 5 V, See ⁽¹⁾	GND	2.048	AV _{DD}	V
	AV _{DD} = 3 V, See ⁽¹⁾	GND	1.024	AV _{DD}	
Analog output load resistance, R _L		2			kΩ
Analog output load capacitance, C _L				100	pF
Clock frequency, f _{CLK}				30	MHz
Operating free-air temperature, T _A		-40		85	°C

- (1) Reference input voltages greater than AV_{DD}/2 causes saturation for large DAC codes.

ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY					
I _{DD} Power supply current	No load, All inputs = DV _{DD} or GND, V _{ref} = 2.048 V, See ⁽¹⁾	Fast	16	21	mA
		Slow	6	8	
Power-down supply current			0.1		μA
POR Power on threshold			2		V
PSRR Power supply rejection ratio	Full scale, See ⁽²⁾		-50		dB

- (1) I_{DD} is measured while continuously writing code 2048 to the DAC. For V_{IH} < DV_{DD} - 0.7 V and V_{IL} > 0.7 V, supply current increases.

- (2) Power supply rejection ratio at full scale is measured by varying AV_{DD} and is given by: PSRR = 20 log [(E_G(AV_{DD}max) - E_G(AV_{DD}min))/V_{DD}max]

ELECTRICAL CHARACTERISTICS (continued)

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
STATIC DAC SPECIFICATIONS							
Resolution	TLV5630			12		Bits	
	TLV5631			10		Bits	
	TLV5632			8		Bits	
INL	Integral nonlinearity	V _{ref} = 1 V, 2 V	Code 40 to 4095	±2	±6	LSB	
	Code 20 to 1023		±0.5	±2	LSB		
	Code 6 to 255		±0.3	±1	LSB		
DNL	Differential nonlinearity	V _{ref} = 1 V, 2 V	Code 40 to 4095	±0.5	±1	LSB	
	Code 20 to 1023		±0.1	±1	LSB		
	Code 6 to 255		±0.1	±1	LSB		
E _{ZS}	Zero scale error (offset error at zero scale)					±30	mV
E _{ZS} TC	Zero scale error temperature coefficient			30		μV/°C	
E _G	Gain error					±0.6	%Full Scale V
EGTC	Gain error temperature coefficient			10		ppm/°C	
OUTPUT SPECIFICATIONS							
V _O	Voltage output range	R _L = 10 kΩ		0	AV _{DD} -0.4		V
	Output load regulation accuracy	R _L = 2 kΩ vs 10 kΩ				±0.3	%Full Scale V
REFERENCE OUTPUT							
V _{REFOUTL}	Low reference voltage	V _{DD} > 4.75 V		1.010	1.024	1.040	V
V _{REFOUTH}	High reference voltage			2.020	2.048	2.096	V
I _{ref} (Source)	Output source current					1	mA
I _{ref} (Sink)	Output sink current			-1		mA	
	Load capacitance	See ⁽³⁾		1	10	μF	
PSRR	Power supply rejection ratio			60		dB	
REFERENCE INPUT							
V _I	Input voltage range			0	AV _{DD}		V
R _I	Input resistance			50		kΩ	
C _I	Input capacitance			10		pF	
	Reference input bandwidth	V _{ref} = 0.4 V _{pp} + 2.048 Vdc, Input code = 0x800	Fast	2.2		MHz	
			Slow	1.9		MHz	
	Reference feedthrough	V _{ref} = 2 V _{pp} at 1 kHz + 2.048 Vdc, See ⁽⁴⁾		84		dB	
DIGITAL INPUTS							
I _{IH}	High-level digital input current	V _I = DV _{DD}				1	μA
I _{IL}	Low-level digital input current	V _I = 0 V		1		μA	
C _I	Input capacitance			8		pF	

(3) In parallel with a 100-nF capacitor

(4) Reference feedthrough is measured at the DAC output with an input code = 0x000.

ELECTRICAL CHARACTERISTICS (continued)

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIGITAL OUTPUT						
V_{OH}	High-level digital output voltage	$R_L = 10\text{ k}\Omega$	2.6			V
V_{OL}	Low-level digital output voltage	$R_L = 10\text{ k}\Omega$			0.4	V
	Output voltage rise time	$R_L = 10\text{ k}\Omega$, $C_L = 20\text{ pF}$, Includes propagation delay		5	10	ns
ANALOG OUTPUT DYNAMIC PERFORMANCE						
$t_{s(FS)}$	Output settling time, full scale	$R_L = 10\text{ k}\Omega$, $C_L = 100\text{ pF}$, See ⁽⁵⁾	Fast	1	3	μs
			Slow	3	7	
$t_{s(CC)}$	Output settling time, code to code	$R_L = 10\text{ k}\Omega$, $C_L = 100\text{ pF}$, See ⁽⁶⁾	Fast	0.5	1	μs
			Slow	1	2	
SR	Slew rate	$R_L = 10\text{ k}\Omega$, $C_L = 100\text{ pF}$, See ⁽⁷⁾	Fast	4	10	V/ μs
			Slow	1	3	
	Glitch energy	See ⁽⁸⁾		4		nV-s
	Channel crosstalk	10 kHz sine, 4 V_{PP}		90		dB

- (5) Settling time is the time for the output signal to remain within ± 0.5 LSB of the final measured value for a digital input code change of 0x080 to 0xFFFF and 0xFFFF to 0x080, respectively. Assured by design; not tested.
- (6) Settling time is the time for the output signal to remain within ± 0.5 LSB of the final measured value for a digital input code change of one count. The max time applies to code changes near zero scale or full scale. Assured by design; not tested.
- (7) Slew rate determines the time it takes for a change of the DAC output from 10% to 90% full-scale voltage.
- (8) Code transition: TLV5630 - 0x7FF to 0x800, TLV5631 - 0x7FC to 0x800, TLV5632 - 0x7F0 to 0x800.

DIGITAL INPUT TIMING REQUIREMENTS

PARAMETER		MIN	TYP	MAX	UNIT
$t_{su(FS-CK)}$	Setup time, FS low before next negative SCLK edge	8			ns
$t_{su(C16-FS)}$	Setup time, 16 th negative edge after FS low on which bit D0 is sampled before rising edge of FS. μC mode only	10			ns
$t_{su(FS-C17)}$	μC mode, setup time, FS high before 17 th negative edge of SCLK.	10			ns
$t_{su(CK-FS)}$	DSP mode, setup time, SCLK low before FS low.	5			ns
$t_{wL(LDAC)}$	\overline{LDAC} duration low	10			ns
t_{wH}	SCLK pulse duration high	16			ns
t_{wL}	SCLK pulse duration low	16			ns
$t_{su(FS-CK)}$	Setup time, FS low before first negative SCLK edge	8			ns
$t_{su(D)}$	Setup time, data ready before SCLK falling edge	8			ns
$t_{h(D)}$	Hold time, data held valid after SCLK falling edge	5			ns
$t_{wH(FS)}$	FS duration high	10			ns
$t_{wL(FS)}$	FS duration low	10			ns
t_s	Settling time	See AC specs			

TYPICAL CHARACTERISTICS

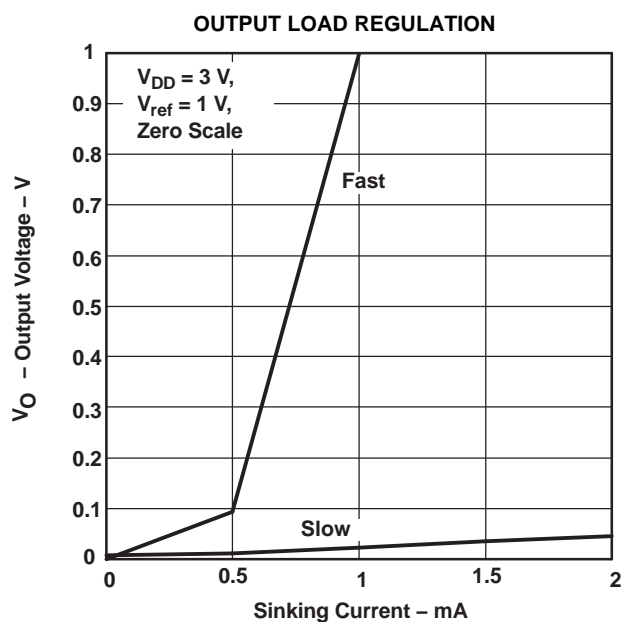


Figure 1.

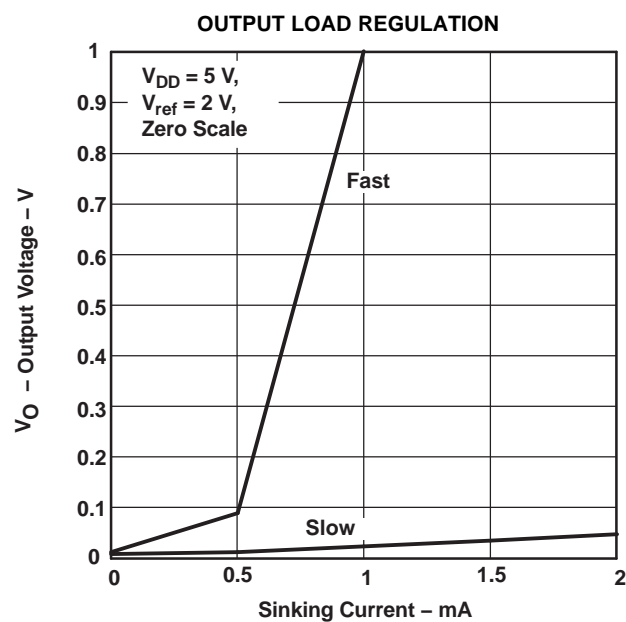


Figure 2.

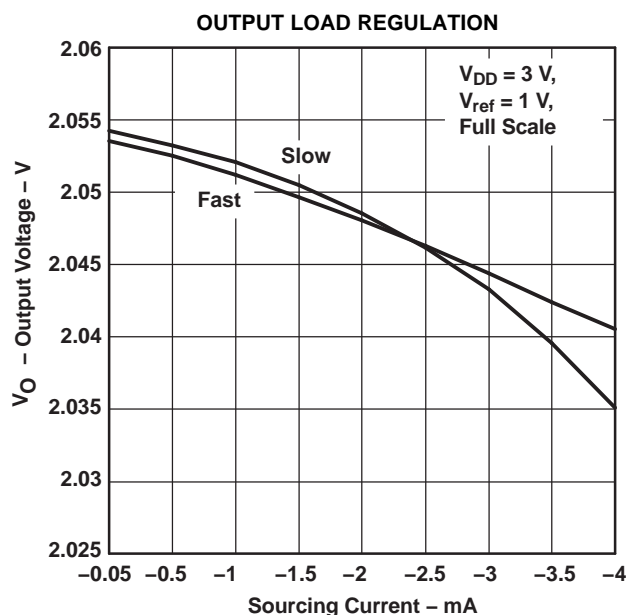


Figure 3.

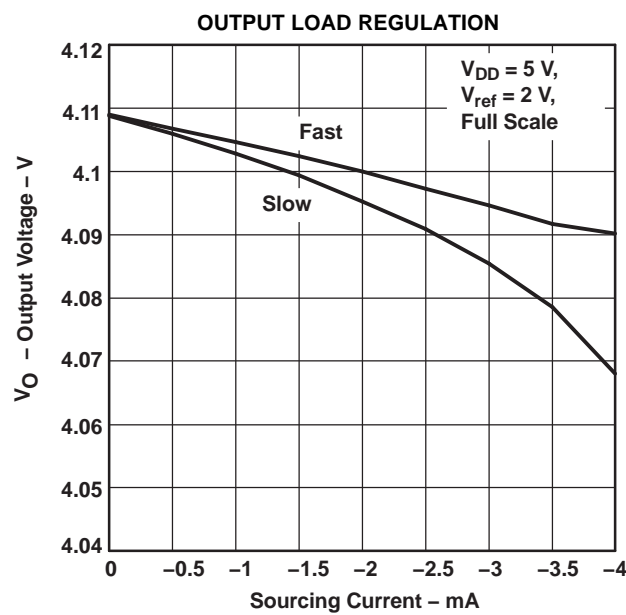


Figure 4.

TYPICAL CHARACTERISTICS (continued)

**TLV5630 INTEGRAL NONLINEARITY
vs
CODE**

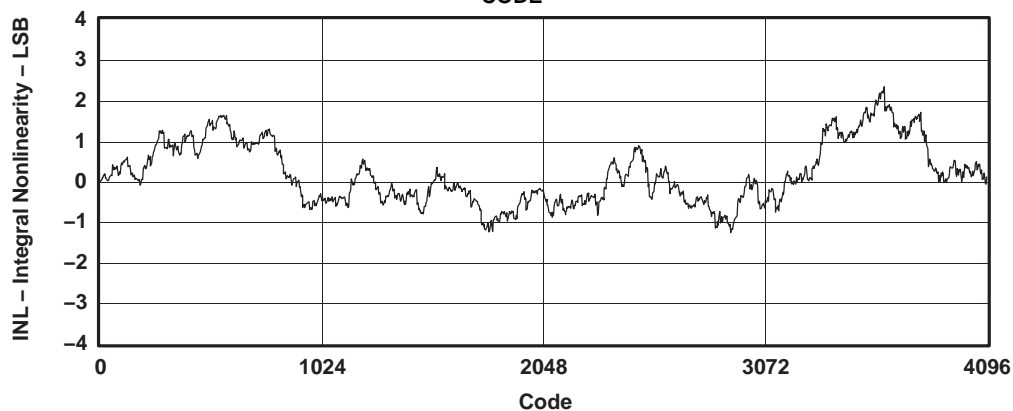


Figure 5.

**TLV5630 DIFFERENTIAL NONLINEARITY
vs
CODE**

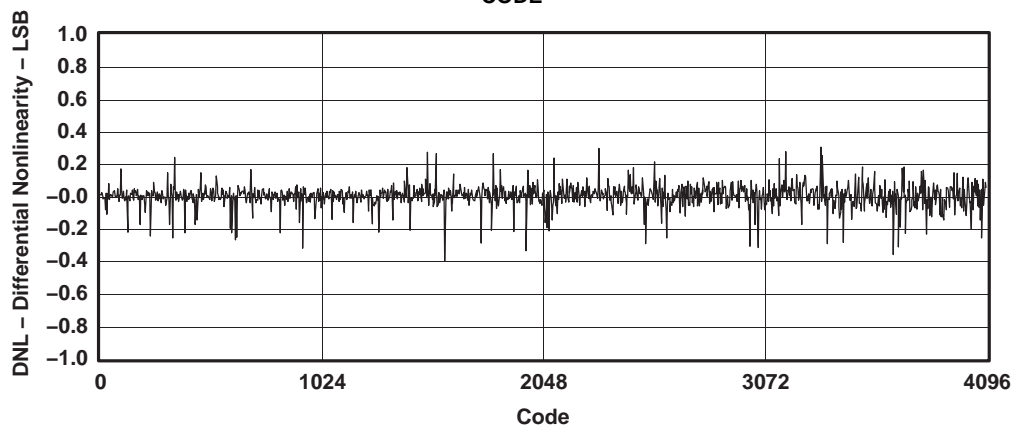


Figure 6.

**TLV5631 INTEGRAL NONLINEARITY
vs
CODE**

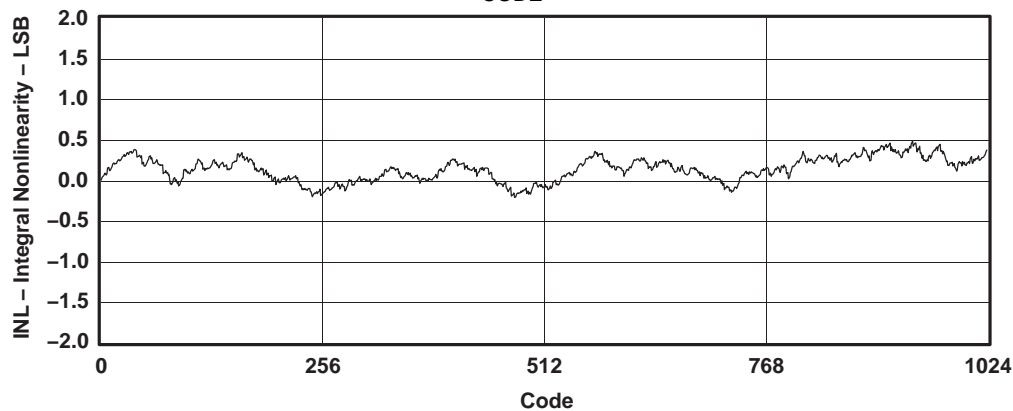


Figure 7.

TYPICAL CHARACTERISTICS (continued)

TLV5631 DIFFERENTIAL NONLINEARITY
vs
CODE

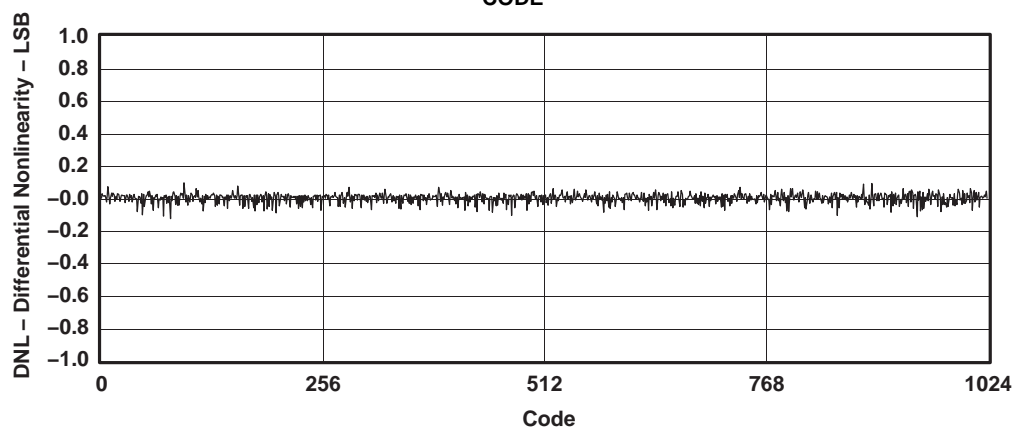


Figure 8.

TLV5632 INTEGRAL NONLINEARITY
vs
CODE

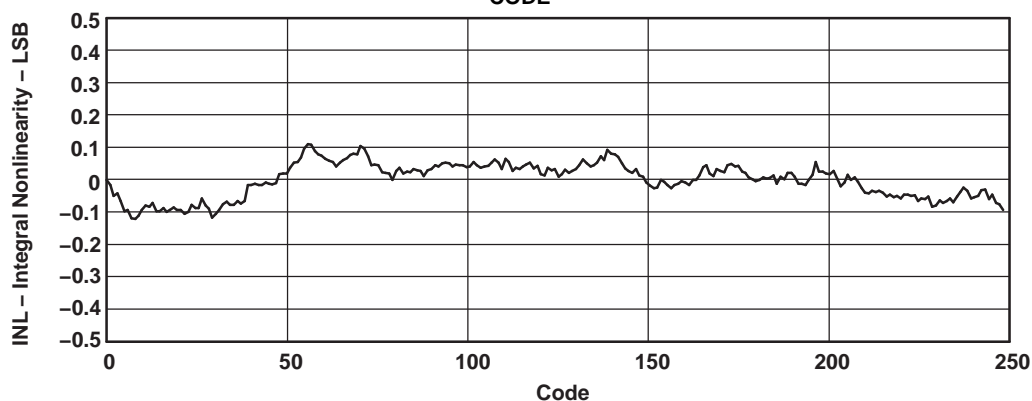


Figure 9.

TLV5632 DIFFERENTIAL NONLINEARITY
vs
CODE

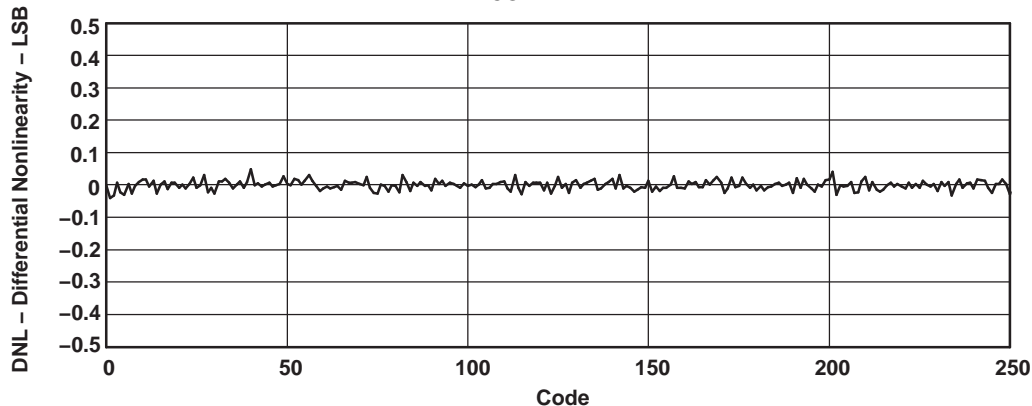


Figure 10.

PARAMETER MEASUREMENT INFORMATION

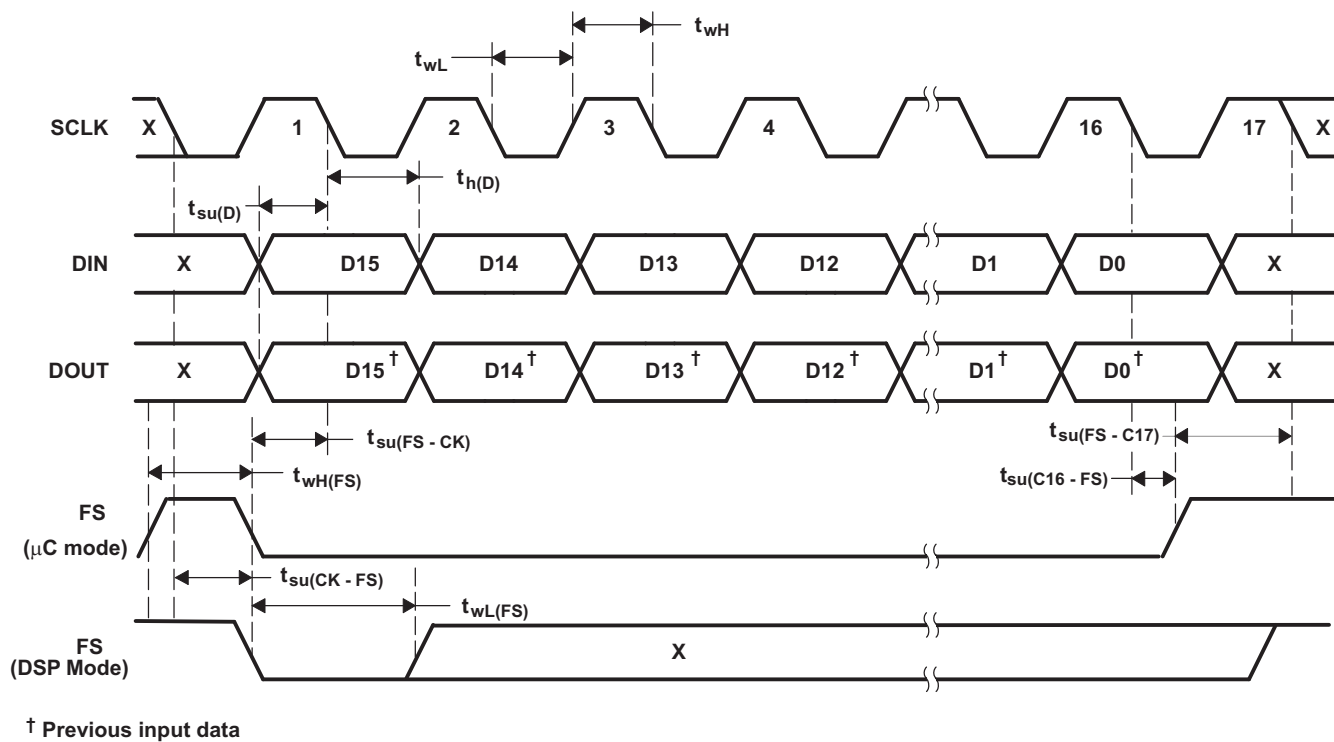


Figure 11. Serial Interface Timing

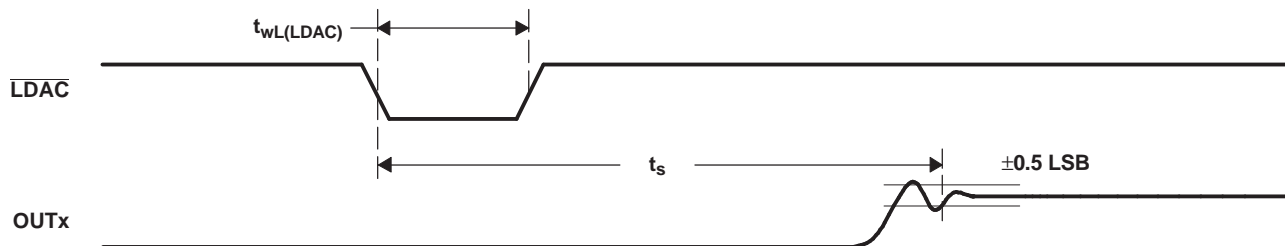


Figure 12. Output Timing

APPLICATION INFORMATION

GENERAL FUNCTION

The TLV5630/31/32 are 8-channel, single-supply DACs, based on a resistor string architecture. They consist of a serial interface, a speed and power-down control logic, an internal reference, a resistor string, and a rail-to-rail output buffer.

The output voltage (full scale determined by reference) for each channel is given by:

$$2\text{REF} \frac{\text{CODE}}{0\text{x}1000} [\text{V}]$$

where REF is the reference voltage and CODE is the digital input value. The input range is 0x000 to 0xFFF for the TLV5630, 0x000 to 0xFFC for the TLV5631, and 0x000 to 0xFF0 for the TLV5632.

POWER ON RESET (POR)

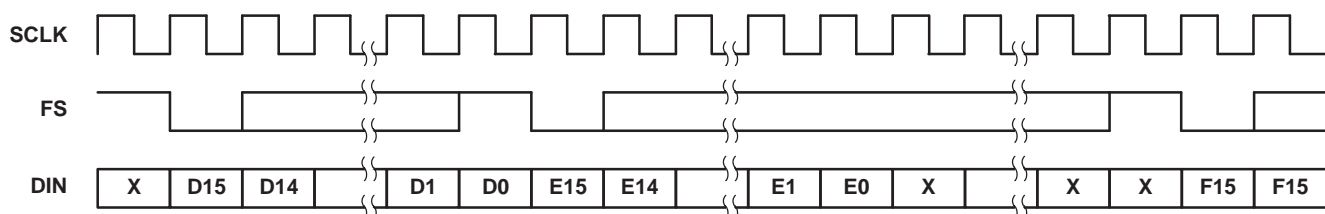
The built-in power-on-reset circuit controls the output voltage after power up. On power up, all latches including the preset register are set to zero, but the DAC outputs are only set to zero if the LDAC is low. The DAC outputs may have a small offset error produced by the output buffer. The registers remains at zero until a valid write sequence is made to the DAC, changing the DAC register data. This is useful in applications where it is important to know the state of the outputs of the DAC after power up. All digital inputs must be logic low until the digital and analog supplies are applied. Any logic high voltages applied to the logic input pins when power is not applied to AV_{DD} and DV_{DD}, may power the device logic circuit through the overvoltage protection diode causing an undesired operation. When separate analog (AV_{DD}) and digital (DV_{DD}) supplies are used, AV_{DD} must come up first before DV_{DD}, to ensure that the power-on-reset circuit operates correctly.

SERIAL INTERFACE

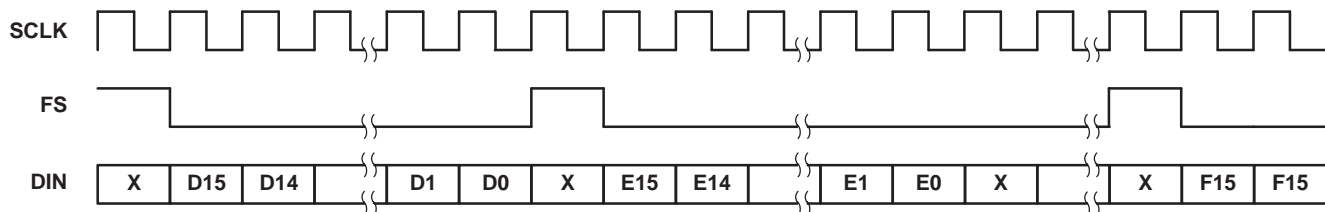
A falling edge of FS starts shifting the data on DIN starting with the MSB to the internal register on the falling edges of SCLK. After 16 bits have been transferred, the content of the shift register is moved to one of the DAC holding registers, depending on the address bits within the data word. A logic 0 on the LDAC pin is required to transfer the content of the DAC holding register to the DAC latch and to update the DAC outputs. LDAC is an asynchronous input. It can be held low if a simultaneous update of all eight channels is not needed.

For daisy-chaining, DOUT provides the data sampled on DIN with a delay of 16 clock cycles.

DSP Mode:



μC Mode:



Difference between DSP mode (MODE = N.C. or 0) and μ C (MODE = 1) mode:

- In μ C mode, FS needs to be held low until all 16 data bits have been transferred. If FS is driven high before the 16th falling clock edge, the data transfer is cancelled. The DAC is updated after a rising edge on FS.
- In DSP mode, FS needs to stay low for 20 ns and can go high before the 16th falling clock edge.
- In DSP mode there needs to be one falling SCLK edge before FS goes low to start the write (DIN) cycle. This extra falling SCLK edge has to happen at least 5 ns before FS goes low, $t_{su(CK-FS)} \geq 5$ ns.
- In μ C mode, the extra falling SCLK edge is not necessary. However, if it does happen, the extra negative SCLK edge is not allowed to occur within 10 ns after FS goes HIGH to finish the WRITE cycle ($t_{su(FS-C17)}$).

SERIAL CLOCK FREQUENCY AND UPDATE RATE

The maximum serial clock frequency is given by:

$$f_{sclkmax} = \frac{1}{t_{whmin} + t_{wlmin}} = 30 \text{ MHz}$$

The maximum update rate is:

$$f_{updatemax} = \frac{1}{16(t_{whmin} + t_{wlmin})} = 1.95 \text{ MHz}$$

Note, that the maximum update rate is just a theoretical value for the serial interface, as the settling time of the DAC has to be considered also.

DATA FORMAT

The 16-bit data word consists of two parts:

- Address bits (D15...D12)
- Data bits (D11...D0)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
A3	A2	A1	A0	Data											

Ax: Address bits. See table.

REGISTER MAP

A3	A2	A1	A0	FUNCTION
0	0	0	0	DAC A
0	0	0	1	DAC B
0	0	1	0	DAC C
0	0	1	1	DAC D
0	1	0	0	DAC E
0	1	0	1	DAC F
0	1	1	0	DAC G
0	1	1	1	DAC H
1	0	0	0	CTRL0
1	0	0	1	CTRL1
1	0	1	0	Preset
1	0	1	1	Reserved
1	1	0	0	DAC A and \overline{B}
1	1	0	1	DAC C and \overline{D}
1	1	1	0	DAC E and \overline{F}
1	1	1	1	DAC G and \overline{H}

DAC A-H AND TWO-CHANNEL REGISTERS

Writing to DAC A-H sets the output voltage of channel A-H. It is possible to automatically generate the complement of one channel by writing to one of the four two-channel registers (DAC A and \bar{B} etc.).

The TLV5630 decodes all 12 data bits. The TLV5631 decodes D11 to D2 (D1 and D0 are ignored). The TLV5632 decodes D11 to D4 (D3 to D0 are ignored).

PRESET

The outputs of the DAC channels can be driven simultaneously to a predefined value stored in the preset register by driving the $\overline{\text{PRE}}$ input pin low and asserting the $\overline{\text{LDAC}}$ input pin. The preset register is cleared (set to zero) by the POR circuit after power up. Therefore, it must be written with a predefined value before asserting the $\overline{\text{PRE}}$ pin low, unless zero is the desired preset value. The $\overline{\text{PRE}}$ input is asynchronous to the clock.

CTRL0

BIT	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Function	X	X	X	X	X	X	X	PD	DO	R1	R0	IM
Default	X	X	X	X	X	X	X	0	0	0	0	0

PD : Full device power down 0 = normal 1 = power down
DO : DOUT enable 0 = disabled 1 = enabled
R1:0 : Reference select bits 0 = external 1 = external, 2 = internal 1 V, 3 = internal 2 V
IM : Input mode 0 = straight binary 1 = twos complement
X : Reserved

If DOUT is enabled, the data input on DIN is output on DOUT with a 16-cycle delay. That makes it possible to daisy-chain multiple DACs on one serial bus.

CTRL1

BIT	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Function	X	X	X	X	P _{GH}	P _{EF}	P _{CD}	P _{AB}	S _{GH}	S _{EF}	S _{CD}	S _{AB}
Default	X	X	X	X	0	0	0	0	0	0	0	0

P_{XY} : Power Down DAC_{XY} 0 = normal 1 = power down
S_{XY} : Speed DAC_{XY} 0 = slow 1 = fast
XY : DAC pair AB, CD, EF or GH

In power-down mode, the amplifiers of the selected DAC pair are disabled and the total power consumption of the device is significantly reduced. Power-down mode of a specific DAC pair can be selected by setting the P_{XY} bit within the data word to 1.

There are two settling time modes: fast and slow. Fast mode of a DAC pair is selected by setting S_{XY} to 1 and slow mode is selected by setting S_{XY} to 0.

REFERENCE

The DAC reference can be sourced internally or externally by programming bits D2 (R1) and D1 (R0) of the CTRL0 register (address = 08h). If an external source of reference is applied to the REF pin, the device must be configured to accept the external reference source by setting R1 and R0 to 00 or 01. If R1 and R0 is set to select for internal reference, a voltage of 1.024 V (if R1 and R0 = 10) or 2.048 V (if R1 and R0 = 11) is available. The internal reference can source up to 1 mA, therefore, it can be used as an external system reference. A decoupling capacitor must be connected to the REF pin if internal reference is selected to ensure output stability. A 1 μ F to 10 μ F capacitor in parallel to a 100 pF capacitor should be sufficient, see Figure 13.

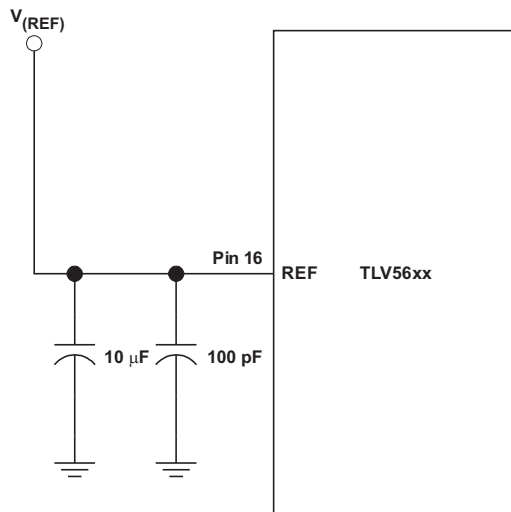


Figure 13. Reference Pin Decoupling Connection

BUFFERED AMPLIFIER

The DAC outputs are buffered by an amplifier with a gain of two, which are configurable as Class A (fast mode) or Class AB (slow or low-power mode). The output buffers have near rail-to-rail output with short-circuit protection, and can reliably drive a 2-k Ω load with a 100-pF load capacitance.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV5630IDW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TLV5630I	Samples
TLV5630IDWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TLV5630I	Samples
TLV5630IPW	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TY5630	Samples
TLV5630IPWG4	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TY5630	Samples
TLV5630IPWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TY5630	Samples
TLV5631IDW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TLV5631I	Samples
TLV5631IDWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TLV5631I	Samples
TLV5631IDWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TLV5631I	Samples
TLV5631IPW	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TY5631	Samples
TLV5631IPWG4	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TY5631	Samples
TLV5631IPWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TY5631	Samples
TLV5631IPWRG4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TY5631	Samples
TLV5632IDW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TLV5632I	Samples
TLV5632IDWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TLV5632I	Samples
TLV5632IPW	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TY5632	Samples
TLV5632IPWG4	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TY5632	Samples
TLV5632IPWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TY5632	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of ≤ 1000 ppm threshold. Antimony trioxide based flame retardants must also meet the ≤ 1000 ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

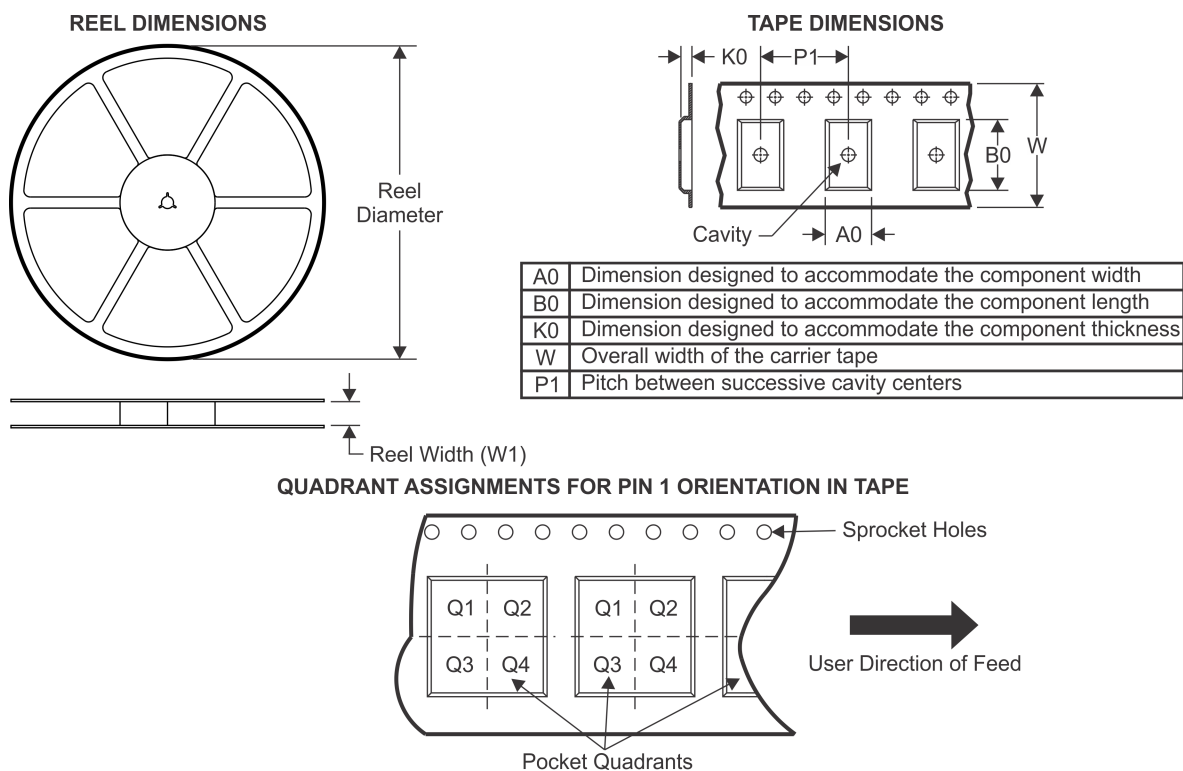
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

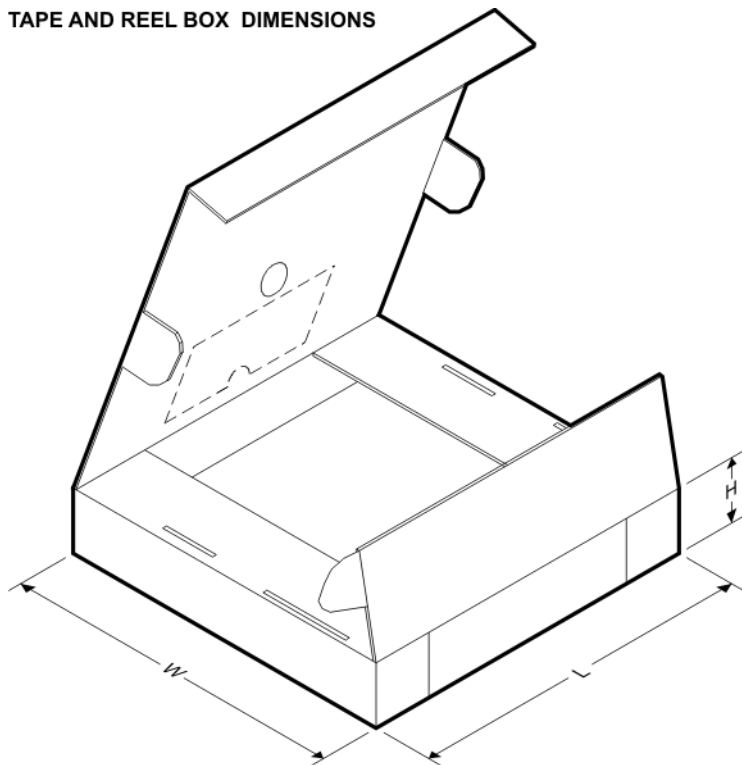
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV5630IPWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
TLV5631IDWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
TLV5631IPWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
TLV5632IDWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
TLV5632IPWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

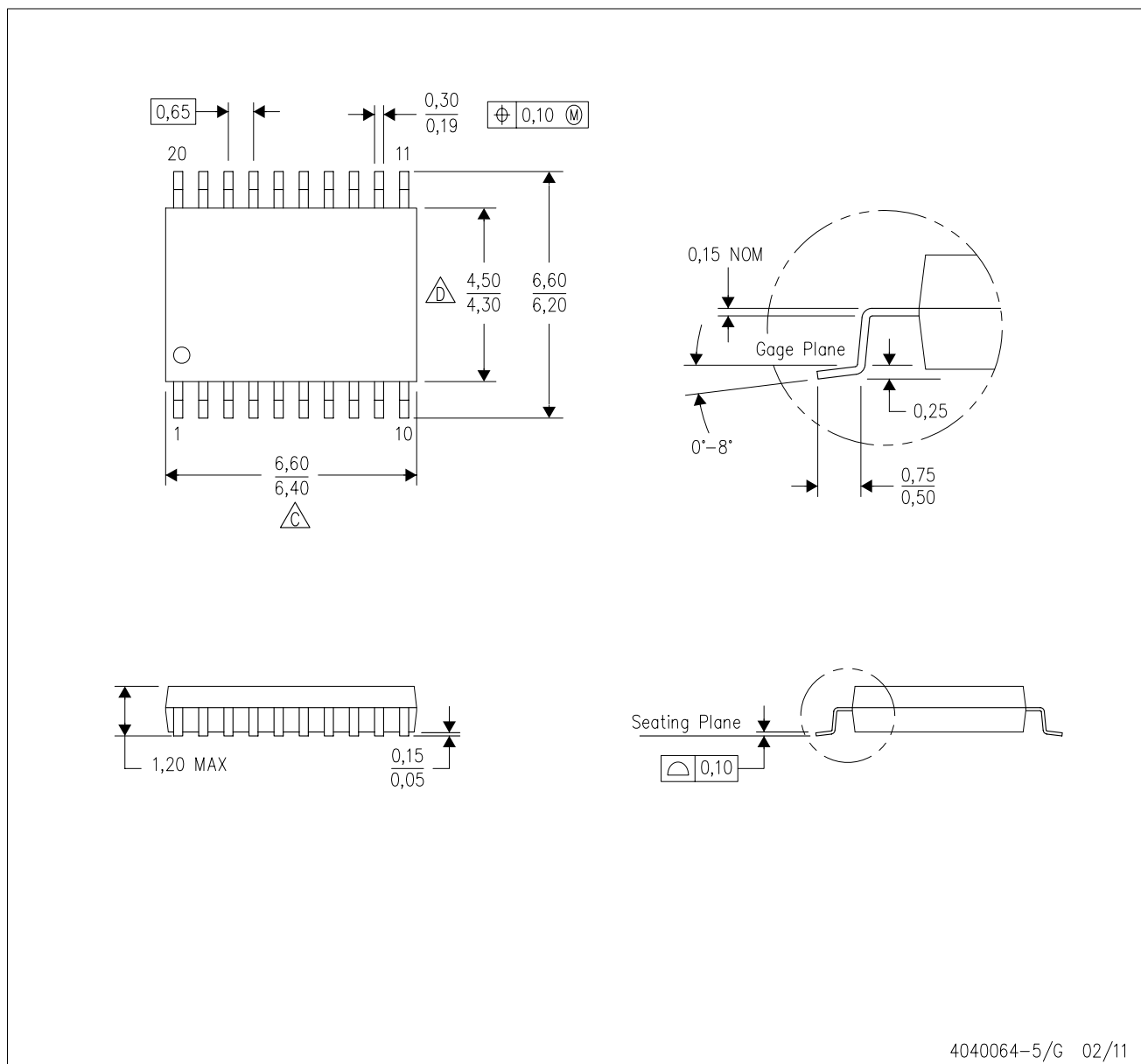


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV5630IPWR	TSSOP	PW	20	2000	367.0	367.0	38.0
TLV5631IDWR	SOIC	DW	20	2000	367.0	367.0	45.0
TLV5631IPWR	TSSOP	PW	20	2000	367.0	367.0	38.0
TLV5632IDWR	SOIC	DW	20	2000	367.0	367.0	45.0
TLV5632IPWR	TSSOP	PW	20	2000	367.0	367.0	38.0

PW (R-PDSO-G20)

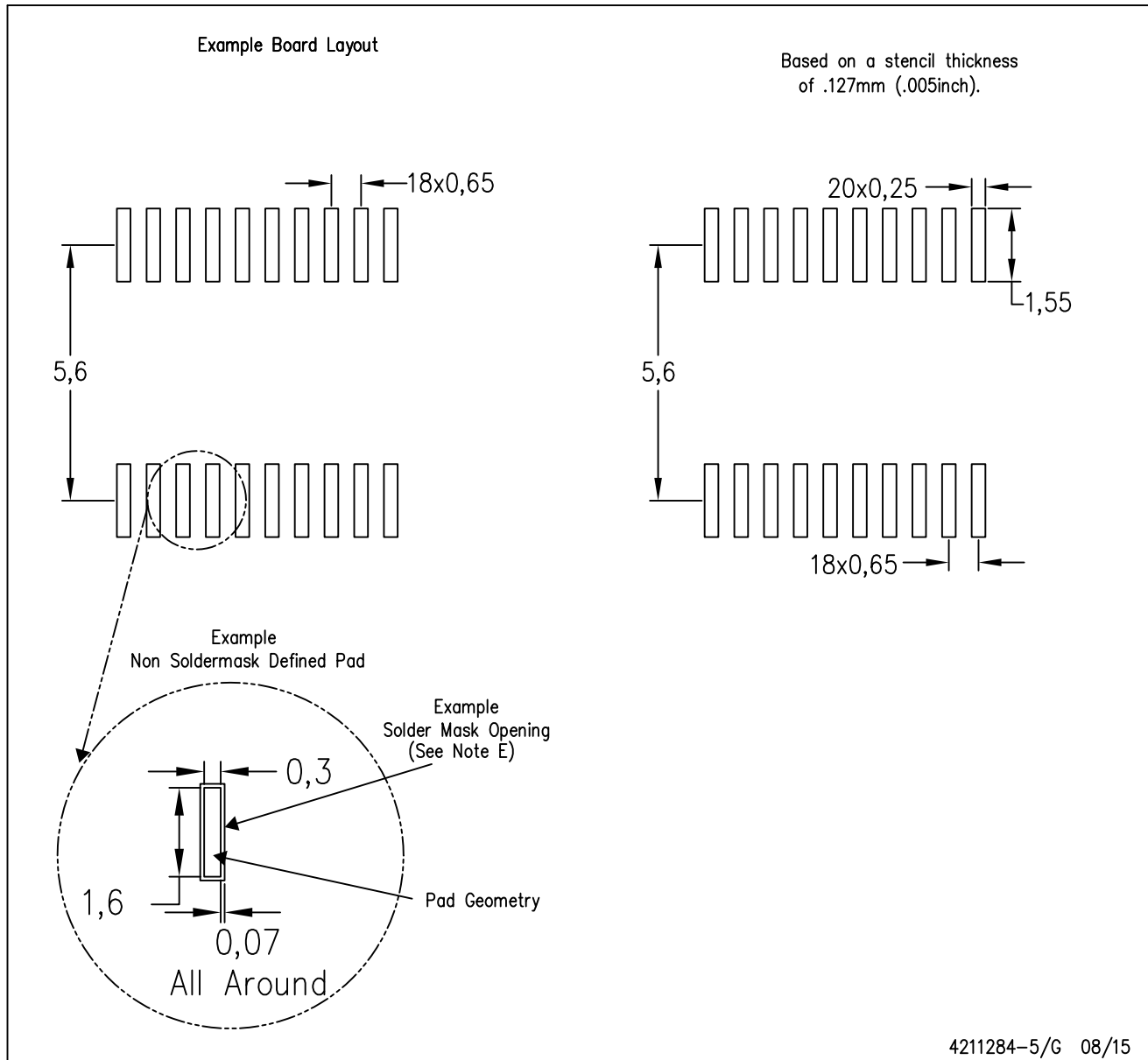
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G20)

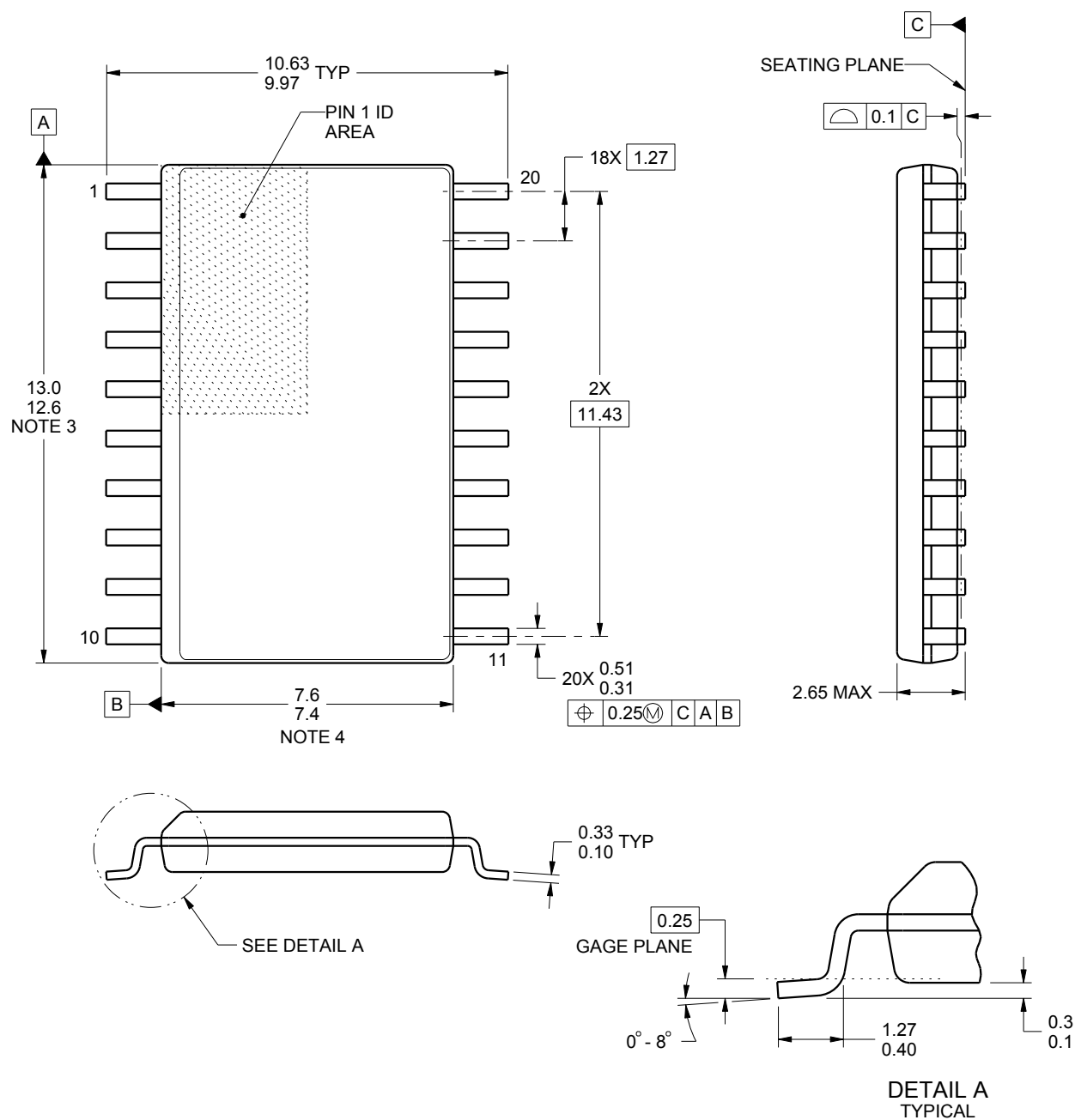
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate design.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DW0020A**PACKAGE OUTLINE****SOIC - 2.65 mm max height**

SOIC



4220724/A 05/2016

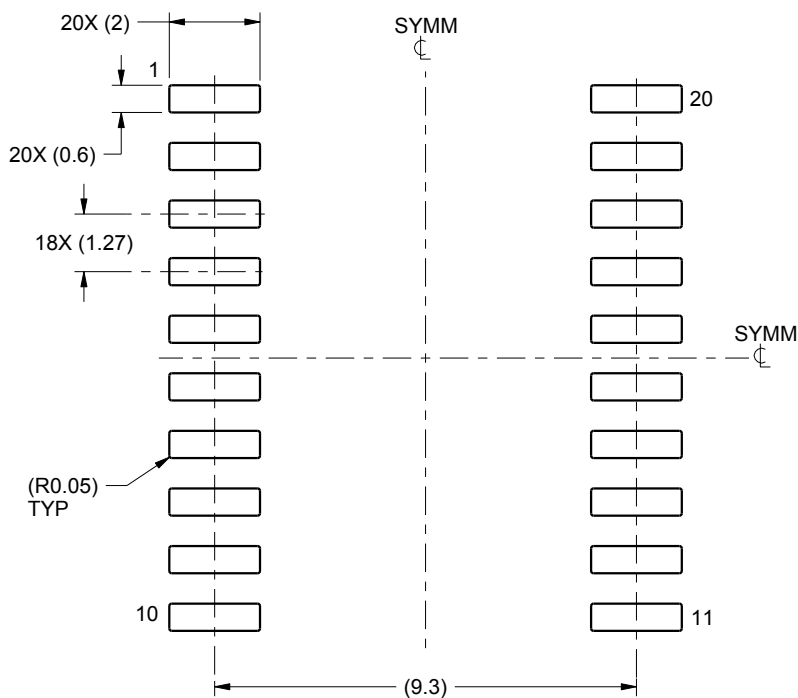
NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

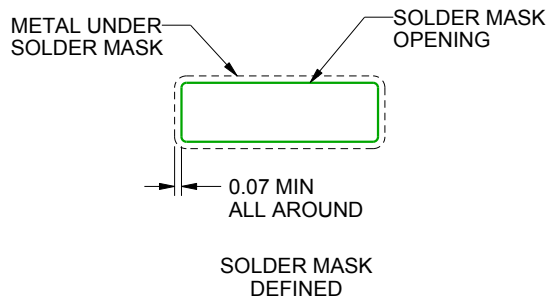
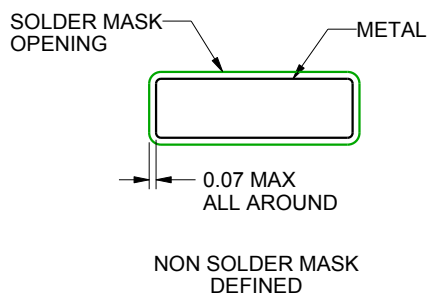
DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

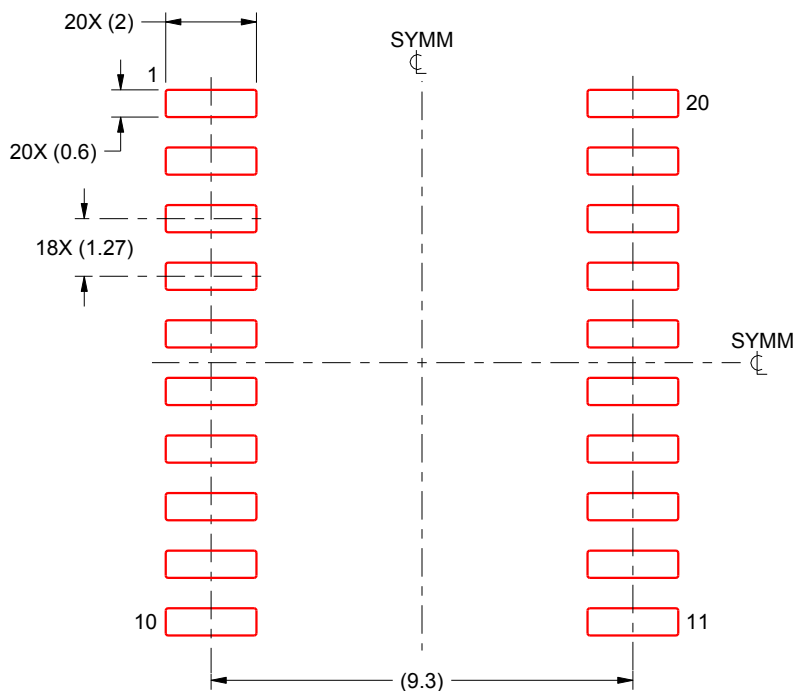
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (<http://www.ti.com/sc/docs/stdterms.htm>) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, "Designers") understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers' applications and compliance of their applications (and of all TI products used in or for Designers' applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI's provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer's company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.