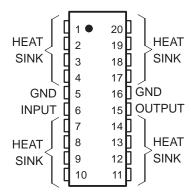
- Fully Matches Parameters for SCSI Alternative 2 Active Termination
- Fixed 2.85-V Output
- $\pm 1\%$ Maximum Output Tolerance at $T_{.1} = 25$ °C
- 0.7-V Maximum Dropout Voltage
- 620-mA Output Current
- ±2% Absolute Output Variation
- Internal Overcurrent-Limiting Circuitry
- Internal Thermal-Overload Protection
- Internal Overvoltage Protection

description

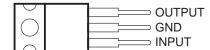
The TL-SCSI285 is a low-dropout (0.7-V) fixed-voltage regulator specifically designed for small computer systems interface (SCSI) alternative 2 active signal termination. The TL-SCSI285 0.7-V maximum dropout ensures compatibility with existing SCSI systems, while providing a wide TERMPWR voltage range. At the same time, the $\pm 1\%$ initial tolerance on its 2.85-V output voltage ensures a tighter line-driver current tolerance, thereby increasing the system noise margin.

PW PACKAGE (TOP VIEW)



HEAT SINK – These terminals have an internal resistive connection to ground and should be grounded or electrically isolated.

KC PACKAGE (TOP VIEW)



The GND terminal is in electrical contact with the mounting base.

The fixed 2.85-V output voltage of the TL-SCSI285 supports the SCSI alternative 2 termination standard, while reducing system power consumption. The 0.7-V maximum dropout voltage brings increased TERMPWR isolation, making the device ideal for battery-powered systems. The TL-SCSI285, with internal current limiting, overvoltage protection, ESD protection, and thermal protection, offers designers enhanced system protection and reliability.

When configured as a SCSI active terminator, the TL-SCSI285 low-dropout regulator eliminates the $220-\Omega$ and the $330-\Omega$ resistors required for each transmission line with a passive termination scheme, reducing significantly the continuous system power drain. When placed in series with $110-\Omega$ resistors, the device matches the impedance level of the transmission cable and eliminates reflections.

The TL-SCSI285 is characterized for operation over the virtual junction temperature range of 0°C to 125°C.

AVAILABLE OPTIONS

	PACKAGI	ED DEVICES	CHIP
ТЈ	PLASTIC POWER (KC)	SURFACE MOUNT (PW)	FORM (Y)
0°C to 125°C	TL-SCSI285KC	TL-SCSI285PWR	TL-SCSI285Y

The PW package is only available taped and reeled. Chip forms are tested at 25°C.



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absolute maximum ratings over operating virtual junction temperature range (unless otherwise noted)†

Continuous input voltage, V _I	7.5 V
Operating virtual junction temperature range, T _J	-55°C to 150°C
Package thermal impedance, θ_{JA} (see Notes 1 and 2): KC package	22°C/W
PW package	83°C/W
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: KC or PW package	260°C
Storage temperature range, Teta	-65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. Maximum power dissipation is a function of $T_J(max)$, θ_{JA} , and T_A . The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can impact reliability. Due to variations in individual device electrical characteristics and thermal resistance, the built-in thermal overload protection may be activated at power levels slightly above or below the rated dissipation.
 - 2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

recommended operating conditions

		TL-SC	SI285	UNIT
		MIN	MAX	UNIT
Input voltage, V _I	T _J = 25°C			V
Input voltage, V _I	$T_J = 0$ °C to 125°C	3.55	5.5	V
Output current le	KC package	0	620	mA
Output current, IO	PW package	0	500	IIIA
Operating virtual junction temperature range, TJ	0	125	°C	

electrical characteristics, $V_I = 4.5 \text{ V}$, $I_O = 500 \text{ mA}$, $T_J = 25^{\circ}\text{C}$ (unless otherwise noted)

PARAMETER	_	TL-SCSI285KC			UNIT				
PARAMETER	ד	MIN	TYP	MAX	UNIT				
Output voltage	$I_O = 20 \text{ mA to } 500 \text{ mA},$	$V_I = 3.55 \text{ V to } 5.5 \text{ V},$	$T_J = 25^{\circ}C$	2.82	2.85	2.88	V		
Output voltage	$I_O = 500 \text{ mA} \text{ to } 620 \text{ mA},$	$V_I = 3.65 \text{ V to } 5.5 \text{ V},$	T _J = 0 to 125°C	2.79		2.91	V		
Input regulation	V _I = 3.55 V to 5.5 V				5	15	mV		
Ripple rejection	f = 120 Hz,	V _{ripple} = 1 V _{O(PP)}			-62		dB		
Outrast samulation	I _O = 20 mA to 620 mA				5	30	m\/		
Output regulation	I _O = 20 mA to 500 mA				5	30	m∨		
Output noise voltage	f = 10 Hz to 100 kHz				500		μV		
Dropout voltage	IO = 500 mA					0.7	V		
Dropout voltage	I _O = 620 mA					0.8	V		
	IO = 0				2	5			
Bias current	IO = 27 mA, equivalent 1 line		3	6	mA				
	IO = 500 mA, equivalent 18 I		26	49					
	I _O = 620 mA				37	62			

[‡] Pulse-testing techniques are used to maintain the virtual junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.1-µF capacitor across the input and a 22.0-µF tantalum capacitor with equivalent series resistance of 1.5 Ω on the output.



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electrical characteristics, $V_I = 4.5 \text{ V}$, $I_O = 500 \text{ mA}$, $T_J = 25^{\circ}\text{C}$ (unless otherwise noted)

PARAMETER		TL-S	UNIT				
PARAWETER		TEST CONDITIONS†				MAX	UNIT
Output voltage	lo = 20 mA to 500 mA	- 00 mA to 500 mA		2.82	2.85	2.88	V
Output voltage	$I_O = 20 \text{ mA to } 500 \text{ mA}, \qquad V_I = 3.55 \text{ V to } 5.5 \text{ V}$	T _J = 0 to 125°C	2.79		2.91	V	
Input regulation	V _I = 3.55 V to 5.5 V	V _I = 3.55 V to 5.5 V					
Ripple rejection	f = 120 Hz,	$V_{ripple} = 1 V_{O(PP)}$			-62		dB
Output regulation	I _O = 20 mA to 500 mA	I _O = 20 mA to 500 mA					
Output noise voltage	f = 10 Hz to 100 kHz				500		μV
Dropout voltage	I _O = 500 mA					0.7	V
	I _O = 0				2	5	
Bias current	I _O = 27 mA, equivalent 1	line asserted			3	6	mA
	IO = 500 mA, equivalent	18 lines asserted (8-bit)			26	49	

[†] Pulse-testing techniques are used to maintain the virtual junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.1- μ F capacitor across the input and a 22.0- μ F tantalum capacitor with equivalent series resistance of $1.5~\Omega$ on the output.

electrical characteristics, $V_I = 4.5 \text{ V}$, $I_O = 500 \text{ mA}$, $T_J = 25^{\circ}\text{C}$

PARAMETER	TEST SOMBITIONS!	TL-	UNIT		
PARAMETER	TEST CONDITIONS†	MIN	TYP	MAX	UNIT
Output voltage	$I_O = 20 \text{ mA to } 500 \text{ mA}, \qquad V_I = 3.55 \text{ V to } 5.5 \text{ V}$		2.85		V
Input regulation	V _I = 3.55 V to 5.5 V		5		mV
Ripple rejection	$f = 120 \text{ Hz},$ $V_{ripple} = 1 V_{O(PP)}$		-62		dB
Output regulation	I _O = 20 mA to 620 mA	5			mV
Output regulation	I _O = 20 mA to 500 mA		5		IIIV
Output noise voltage	f = 10 Hz to 100 kHz		500		μV
	IO = 0		2		
Bias current	I _O = 27 mA, equivalent 1 line asserted	3			
Bias current	I _O = 500 mA, equivalent 18 lines asserted (8-bit)	26 mA			IIIA
	$I_{O} = 620 \text{ mA}$	37			

The Pulse-testing techniques are used to maintain the virtual junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.1- μ F capacitor across the input and a 22.0- μ F tantalum capacitor with equivalent series resistance of 1.5 Ω on the output.



APPLICATION INFORMATION

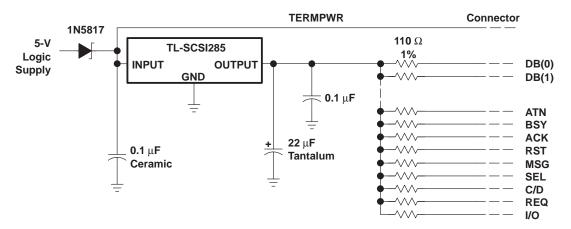


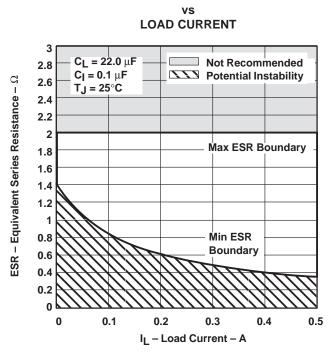
Figure 1. Typical Application Schematic



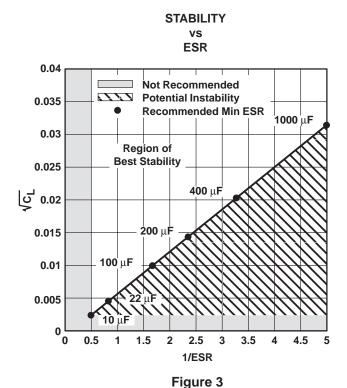
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COMPENSATION CAPACITOR SELECTION INFORMATION

The TL-SCSI285 is a low-dropout regulator. This means that the capacitance loading is important to the performance of the regulator because it is a vital part of the control loop. The capacitor value and the equivalent series resistance (ESR) both affect the control loop and must be defined for the load range and the temperature range. Figures 2 and 3 can be used to establish the capacitance value and ESR range for best regulator performance.



ESR OF OUTPUT CAPACITOR



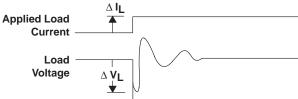


Figure 2







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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
TL-SCSI285KC	OBSOLETE	TO-220	KC	3		TBD	Call TI	Call TI	Samples Not Available
TL-SCSI285KCE3	OBSOLETE	TO-220	KC	3		TBD	Call TI	Call TI	Samples Not Available
TL-SCSI285KCSE3	ACTIVE	TO-220	KCS	3	50	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	Request Free Samples
TL-SCSI285PWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM	Contact TI Distributor or Sales Office
TL-SCSI285PWRE4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM	Contact TI Distributor or Sales Office
TL-SCSI285PWRG4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM	Contact TI Distributor or Sales Office

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

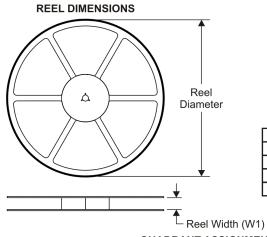
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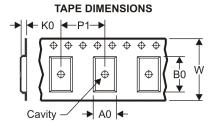
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PACKAGE MATERIALS INFORMATION

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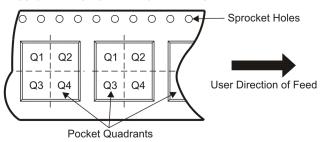
TAPE AND REEL INFORMATION





		Dimension designed to accommodate the component width
		Dimension designed to accommodate the component length
P	〈 0	Dimension designed to accommodate the component thickness
		Overall width of the carrier tape
П	P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing			Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL-SCSI285PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

www.ti.com 5-May-2011



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL-SCSI285PWR	TSSOP	PW	20	2000	346.0	346.0	33.0

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



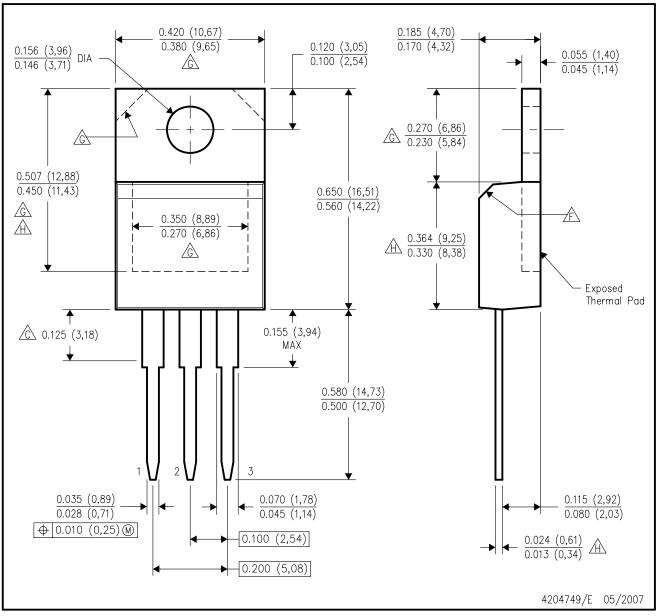
NOTES:

- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M—1994.
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
- E. Falls within JEDEC MO-153



KCS (R-PSFM-T3)

PLASTIC FLANGE-MOUNT PACKAGE



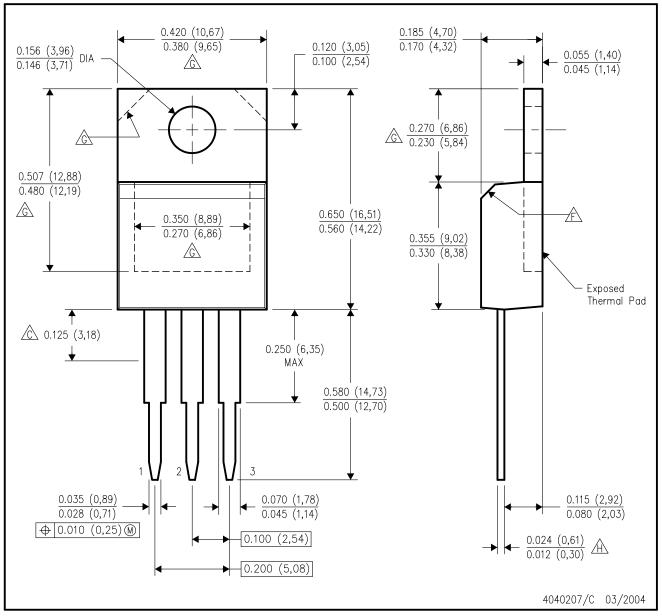
NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Lead dimensions are not controlled within this area.
- D. All lead dimensions apply before solder dip.
- E. The center lead is in electrical contact with the mounting tab.
- The chamfer is optional.
- Thermal pad contour optional within these dimensions.
- Falls within JEDEC TO-220 variation AB, except minimum lead thickness, minimum exposed pad length, and maximum body length.



KC (R-PSFM-T3)

PLASTIC FLANGE-MOUNT PACKAGE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- This drawing is subject to change without notice.
- Lead dimensions are not controlled within this area.
- D. All lead dimensions apply before solder dip.
- E. The center lead is in electrical contact with the mounting tab.
- The chamfer is optional.
- Thermal pad contour optional within these dimensions.
- Falls within JEDEC TO-220 variation AB, except minimum lead thickness.



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