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Please note: As part of the Fairchild Semiconductor integration, some of the Fairchild orderable part numbers will need to change in order to meet ON Semiconductor's system requirements. Since the ON Semiconductor product management systems do not have the ability to manage part nomenclature that utilizes an underscore (_), the underscore (_) in the Fairchild part numbers will be changed to a dash (-). This document may contain device numbers with an underscore (_). Please check the ON Semiconductor website to verify the updated device numbers. The most current and up-to-date ordering information can be found at www.onsemi.com. Please email any questions regarding the system integration to Fairchild_questions@onsemi.com.

FAIRCHILD™

April 2016

FDMC9430L_F085
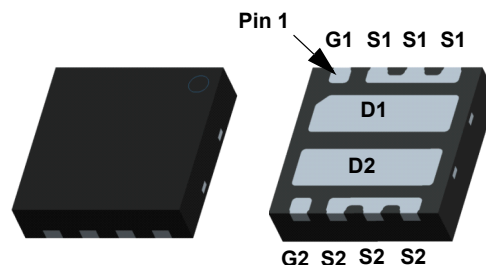
Dual N-Channel Logic Level PowerTrench® MOSFET
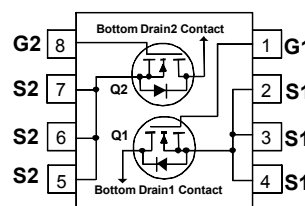
40 V, 12 A, 8.2 mΩ

Features

■ Typical $R_{DS(on)}$ = 6.3 mΩ at V_{GS} = 10V, I_D = 12 A

■ Typical $Q_{g(tot)}$ = 15 nC at V_{GS} = 10V, I_D = 12 A

■ UIS Capability

■ RoHS Compliant

■ Qualified to AEC Q101

Applications

■ Battery Protection

■ Load Switching

■ Point of Load

Pin 1 → G1 S1 S1 S1
D1
D2
G2 S2 S2 S2

Power 33

100% RoHS COMPLIANT

G2	8	Bottom Drain2 Contact	1	G1
S2	7	Q2	2	S1
S2	6	Q1	3	S1
S2	5	Bottom Drain1 Contact	4	S1

For current package drawing, please refer to the Fairchild website at http://www.fairchildsemi.com/package-drawings/ML/MLP08X.pdf.

MOSFET Maximum Ratings T_J = 25°C unless otherwise noted.

Symbol	Parameter		Ratings	Units
V_{DSS}	Drain-to-Source Voltage		40	V
V_{GS}	Gate-to-Source Voltage		±12	V
I_D	Drain Current - Continuous (V_{GS}=10) (Note 1) T_C = 25°C		12	A
	Pulsed Drain Current T_C = 25°C		See Figure 4	
E_{AS}	Single Pulse Avalanche Energy (Note 2)		21.6	mJ
P_D	Power Dissipation		11.4	W
	Derate Above 25°C		0.1	W/°C
T_J, T_{STG}	Operating and Storage Temperature		-55 to + 150	°C
$R_{θJC}$	Thermal Resistance, Junction to Case		13	°C/W
$R_{θJA}$	Maximum Thermal Resistance, Junction to Ambient (Note 3)		65	°C/W

Notes:

1: Current is limited by bondwire configuration.

2: Starting T_J = 25°C, L = 0.3mH, I_{AS} = 12A, V_{DD} = 40V during inductor charging and V_{DD} = 0V during time in avalanche.

3: $R_{θJA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{θJC}$ is guaranteed by design, while $R_{θJA}$ is determined by the board design. The maximum rating presented here is based on mounting on a 1 in^2 pad of 2oz copper.

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMC9430L	FDMC9430L_F085	Power 33	13"	12mm	3000 units

Electrical Characteristics T_J = 25°C unless otherwise noted.

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Units
Off Characteristics							
B_{VDSS}	Drain-to-Source Breakdown Voltage	I_D = 250µA, V_{GS} = 0V		40	-	-	V
I_{DSS}	Drain-to-Source Leakage Current	V_{DS}=40V, V_{GS} = 0V	T_J = 25°C	-	-	1	µA
			T_J = 150°C (Note 4)	-	-	0.2	mA
I_{GSS}	Gate-to-Source Leakage Current	V_{GS} = ±12V		-	-	±100	nA
On Characteristics							
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250µA		1	1.8	3	V
$R_{DS(on)}$	Drain to Source On Resistance	I_D = 10A, V_{GS}= 4.5V		-	8.9	11.5	mΩ
		I_D = 12A, V_{GS}= 10V	T_J = 25°C	-	6.3	8.0	mΩ
			T_J = 150°C (Note 4)	-	10.2	13.0	mΩ
Dynamic Characteristics							
C_{iss}	Input Capacitance	V_{DS} = 20V, V_{GS} = 0V, f = 1MHz		-	984	-	pF
C_{oss}	Output Capacitance			-	315	-	pF
C_{rss}	Reverse Transfer Capacitance			-	18	-	pF
R_g	Gate Resistance	V_{GS} = 0.5V, f = 1MHz		-	1.1	-	Ω
$Q_{g(ToT)}$	Total Gate Charge	V_{GS} = 0 to 10V	V_{DD} = 32V I_D = 12A	-	15	22	nC
$Q_{g(th)}$	Threshold Gate Charge	V_{GS} = 0 to 1V		-	0.9	-	nC
Q_{gs}	Gate-to-Source Gate Charge			-	2.6	-	nC
Q_{gd}	Gate-to-Drain "Miller" Charge			-	2.1	-	nC
Switching Characteristics							
t_{on}	Turn-On Time	V_{DD} = 20V, I_D = 12A, V_{GS} = 10V, R_{GEN} = 6Ω		-	-	13	ns
$t_{d(on)}$	Turn-On Delay			-	7	-	ns
t_r	Rise Time			-	2	-	ns
$t_{d(off)}$	Turn-Off Delay			-	17	-	ns
t_f	Fall Time			-	2	-	ns
t_{off}	Turn-Off Time			-	-	28	ns
Drain-Source Diode Characteristics							
V_{SD}	Source-to-Drain Diode Voltage	I_{SD} = 12A, V_{GS} = 0V		-	-	1.2	V
		I_{SD} = 6A, V_{GS} = 0V		-	-	1.1	V
t_{rr}	Reverse-Recovery Time	V_{DD} = 32V, I_F = 12A, dI_{SD}/dt = 100A/µs		-	32	48	ns
Q_{rr}	Reverse-Recovery Charge			-	16	24	nC

Note:

4: The maximum value is specified by design at T_J = 150°C. Product is not tested to this condition in production.

<div style="text-align: right">**FDMC9430L_F085 Dual N-Channel Logic Level PowerTrench® MOSFET**</div>

Typical Characteristics

POWER DISSIPATION MULTIPLIER

T_C, CASE TEMPERATURE(°C)
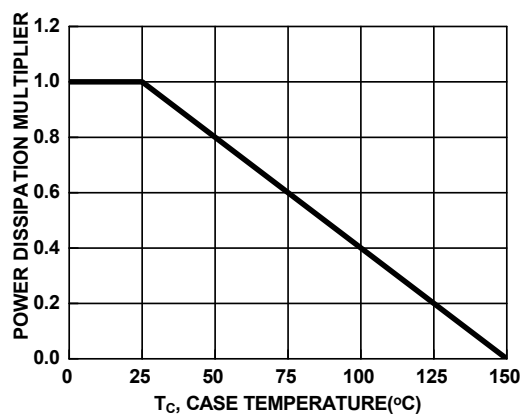
Figure 1. Normalized Power Dissipation vs. Case Temperature

I_D, DRAIN CURRENT (A)

CURRENT LIMITED BY SILICON

$V_{GS} = 10V$

CURRENT LIMITED BY PACKAGE

T_C, CASE TEMPERATURE(°C)
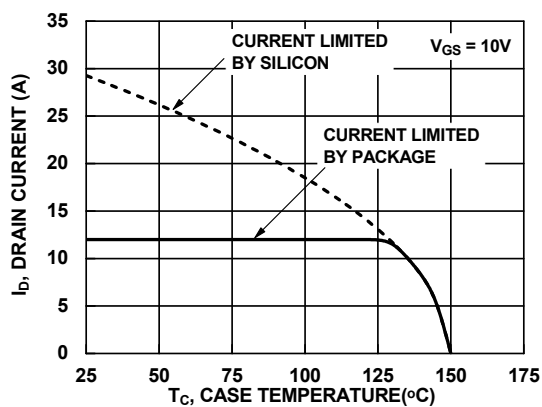
Figure 2. Maximum Continuous Drain Current vs. Case Temperature

NORMALIZED THERMAL IMPEDANCE, $Z_{\theta JC}$

DUTY CYCLE - DESCENDING ORDER

D = 0.50
0.20
0.10
0.05
0.02
0.01

SINGLE PULSE

P_{DM}

t_1

t_2

NOTES:
DUTY FACTOR: $D = t_1/t_2$
PEAK $T_J = P_{DM} \times Z_{\theta JA} \times R_{\theta JA} + T_C$

t, RECTANGULAR PULSE DURATION(s)
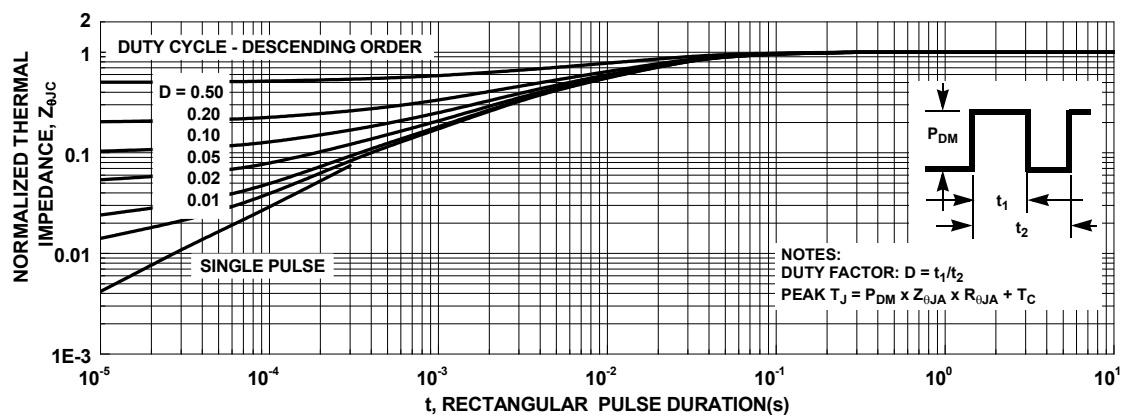
Figure 3. Normalized Maximum Transient Thermal Impedance

$V_{GS} = 10V$

$T_C = 25°C$

FOR TEMPERATURES ABOVE 25°C DERATE PEAK CURRENT AS FOLLOWS:

$$I = I_2 \left[\sqrt{\frac{150 - T_C}{125}} \right]$$

I_{DM}, PEAK CURRENT (A)

SINGLE PULSE

t, RECTANGULAR PULSE DURATION(s)
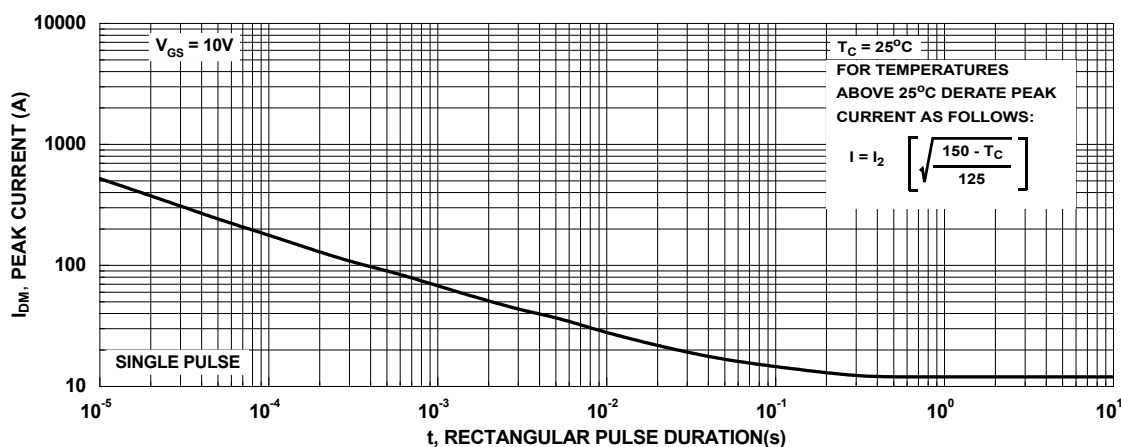
Figure 4. Peak Current Capability

Typical Characteristics
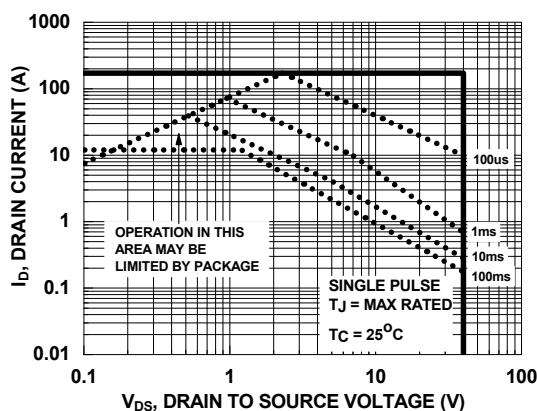
Figure 5. Forward Bias Safe Operating Area
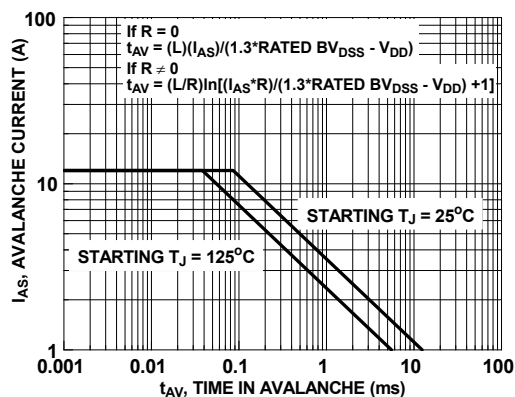
NOTE: Refer to Fairchild Application Notes AN7514 and AN7515

Figure 6. Unclamped Inductive Switching Capability
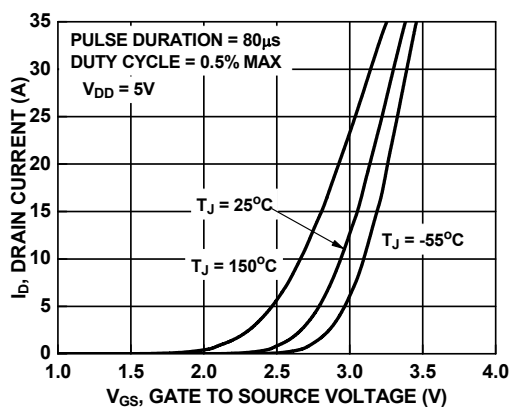
Figure 7. Transfer Characteristics
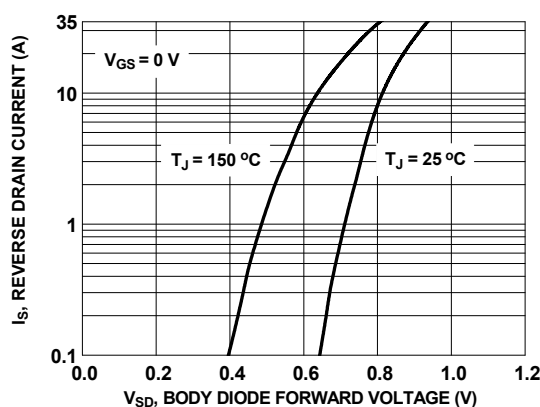
Figure 8. Forward Diode Characteristics
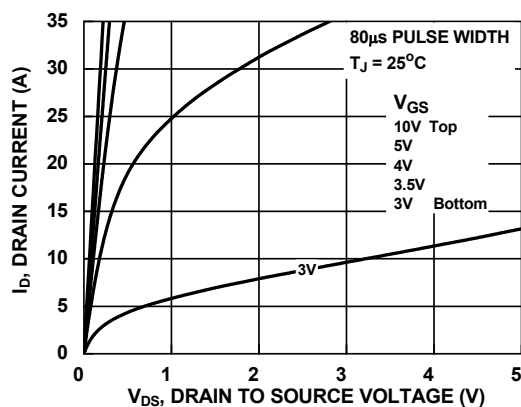
Figure 9. Saturation Characteristics
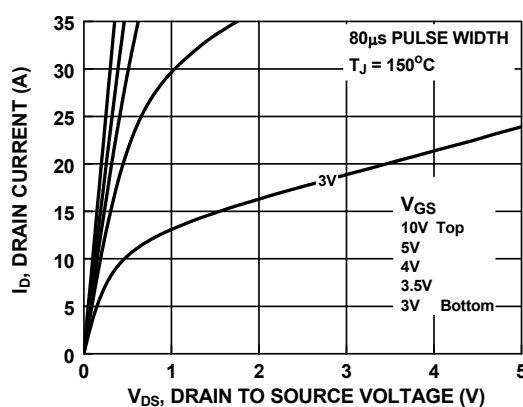
Figure 10. Saturation Characteristics

Typical Characteristics
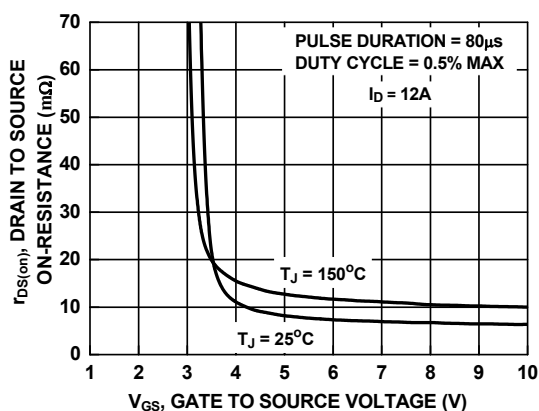
Figure 11. R_{DSON} vs. Gate Voltage
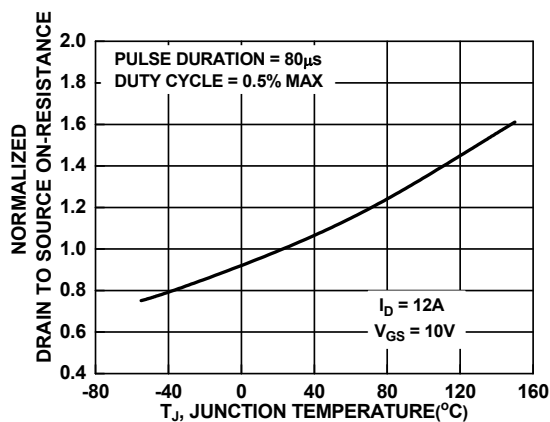
Figure 12. Normalized R_{DSON} vs. Junction Temperature
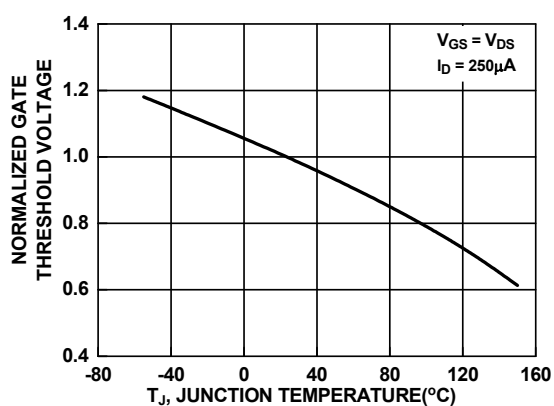
Figure 13. Normalized Gate Threshold Voltage vs. Temperature
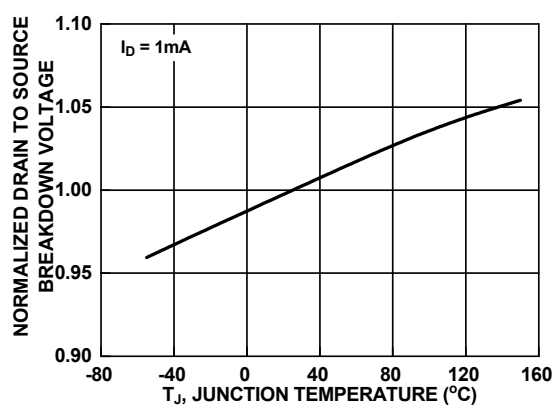
Figure 14. Normalized Drain to Source Breakdown Voltage vs. Junction Temperature
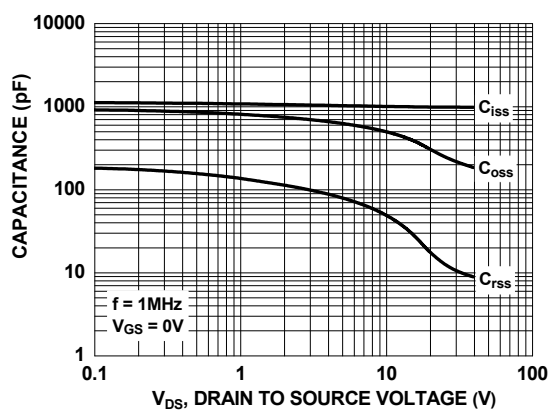
Figure 15. Capacitance vs. Drain to Source Voltage
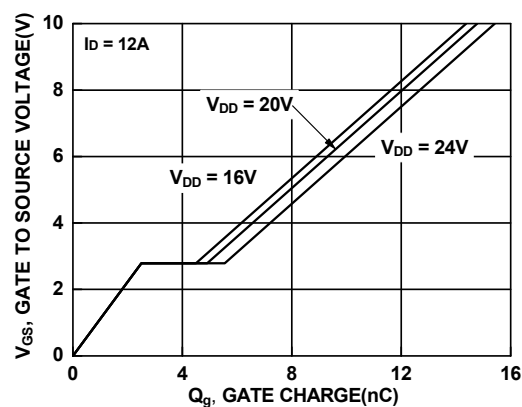
Figure 16. Gate Charge vs. Gate to Source Voltage

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No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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