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April 2016

FDMC9430L F085

Dual N-Channel Logic Level PowerTrench® MOSFET

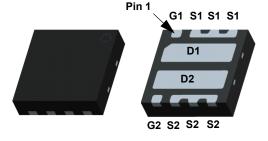
40 V, 12 A, 8.2 mΩ

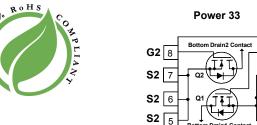
Features

- Typical $R_{DS(on)}$ = 6.3 m Ω at V_{GS} = 10V, I_D = 12 A
- Typical $Q_{g(tot)}$ = 15 nC at V_{GS} = 10V, I_D = 12 A
- UIS Capability
- RoHS Compliant
- Qualified to AEC Q101

Applications

- Battery Protection
- Load Switching
- Point of Load





For current package drawing, please refer to the Fairchild website at http://www.fairchildsemi.com/package-drawings/ML/

2 **S1**

3 **S1**

4 S1

MOSFET Maximum Ratings $T_J = 25$ °C unless otherwise noted.

Symbol	Parameter		Ratings	Units
V_{DSS}	Drain-to-Source Voltage		40	V
V_{GS}	Gate-to-Source Voltage		±12	V
	Drain Current - Continuous (V _{GS} =10) (Note 1)	$T_C = 25^{\circ}C$	12	А
ID	Pulsed Drain Current	T _C = 25°C	See Figure 4	_ A
E _{AS}	Single Pulse Avalanche Energy	(Note 2)	21.6	mJ
D	Power Dissipation		11.4	W
P_D	Derate Above 25°C		0.1	W/°C
T _J , T _{STG}	Operating and Storage Temperature		-55 to + 150	°C
$R_{\theta JC}$	Thermal Resistance, Junction to Case		13	°C/W
$R_{\theta JA}$	Maximum Thermal Resistance, Junction to Ambient	(Note 3)	65	°C/W

- 1: Current is limited by bondwire configuration.
- 2: Starting T $_J$ = 25°C, L = 0.3mH, I $_{AS}$ = 12A, V $_{DD}$ = 40V during inductor charging and V $_{DD}$ = 0V during time in avalanche. 3: R $_{0,JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design, while $R_{\theta JA}$ is determined by the board design. The maximum rating presented here is based on mounting on a 1 in² pad of 2oz copper.

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMC9430L	FDMC9430L_F085	Power 33	13"	12mm	3000 units

Units

Max.

Electrical Characteristics $T_J = 25^{\circ}C$ unless otherwise noted.

Parameter

Off Ch	Off Characteristics							
B _{VDSS}	Drain-to-Source Breakdown Voltage	$I_D = 250 \mu A$	V _{GS} = 0V	40	-	-	V	
I _{DSS} Drain-to-Source Leakage Current	V _{DS} =40V,	$T_J = 25^{\circ}C$	-	-	1	μΑ		
	Dialii-to-Source Leakage Current	$V_{GS} = 0V$	$T_J = 150^{\circ}C \text{ (Note 4)}$	-	-	0.2	mA	
loce	Gate-to-Source Leakage Current	Voc = +12\	1	_	_	+100	nΑ	

Test Conditions

Min.

Тур.

On Characteristics

Symbol

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_{D} = 250 \mu A$		1	1.8	3	V
		I_D = 10A, V_G	_S = 4.5V	-	8.9	11.5	mΩ
R _{DS(on)}	Drain to Source On Resistance	I _D = 12A,	$T_J = 25^{\circ}C$	-	6.3	8.0	mΩ
		V _{GS} = 10V	$T_J = 150^{\circ}C \text{ (Note 4)}$	-	10.2	13.0	mΩ

Dynamic Characteristics

C _{iss}	Input Capacitance	.,		-	984	-	pF
C _{oss}	Output Capacitance	¬ v _{DS} = 20v, v _{GS} = 0 −f = 1MHz	$V_{DS} = 20V, V_{GS} = 0V,$		315	-	pF
C _{rss}	Reverse Transfer Capacitance	-1 - 1WITZ		-	18	-	pF
R_g	Gate Resistance	$V_{GS} = 0.5V, f = 1M$	Hz	-	1.1	-	Ω
$Q_{g(ToT)}$	Total Gate Charge	$V_{GS} = 0$ to 10V	V _{DD} = 32V	-	15	22	nC
$Q_{g(th)}$	Threshold Gate Charge	$V_{GS} = 0 \text{ to } 1V$	I _D = 12A	-	0.9	-	nC
Q_{gs}	Gate-to-Source Gate Charge		_	-	2.6	-	nC
Q_{gd}	Gate-to-Drain "Miller" Charge			-	2.1	-	nC

Switching Characteristics

t _{on}	Turn-On Time		-	-	13	ns
t _{d(on)}	Turn-On Delay		-	7	-	ns
t _r	Rise Time	V _{DD} = 20V, I _D = 12A,	-	2	-	ns
t _{d(off)}	Turn-Off Delay	V_{DD} = 20V, I_{D} = 12A, V_{GS} = 10V, R_{GEN} = 6 Ω	-	17	-	ns
t _f	Fall Time		-	2	-	ns
t _{off}	Turn-Off Time		-	-	28	ns

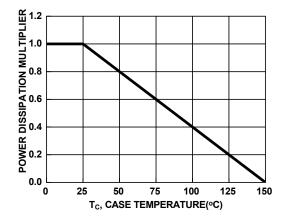
Drain-Source Diode Characteristics

V Source	Source-to-Drain Diode Voltage	I_{SD} = 12A, V_{GS} = 0V	= 12A, V _{GS} = 0V	-	1.2	V
V_{SD}	Source-to-Drain Diode Voltage	$I_{SD} = 6A$, $V_{GS} = 0V$	-	-	1.1	V
t _{rr}	Reverse-Recovery Time	V _{DD} = 32V, I _F = 12A,	-	32	48	ns
Q _{rr}	Reverse-Recovery Charge	dl _{SD} /dt = 100A/μs	-	16	24	nC

Note:

4: The maximum value is specified by design at T_J = 150°C. Product is not tested to this condition in production.

Typical Characteristics



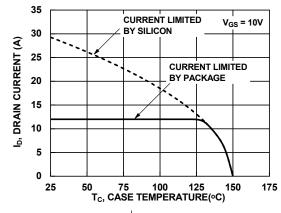


Figure 1. Normalized Power Dissipation vs. Case Temperature

Figure 2. Maximum Continuous Drain Current vs.

Case Temperature

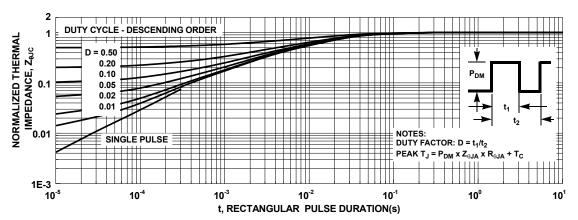


Figure 3. Normalized Maximum Transient Thermal Impedance

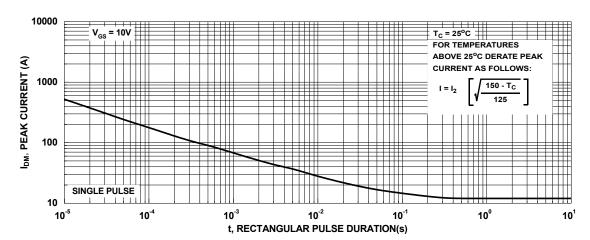


Figure 4. Peak Current Capability

Typical Characteristics

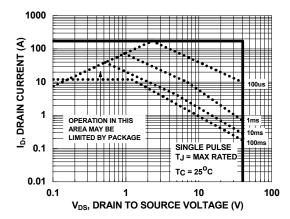
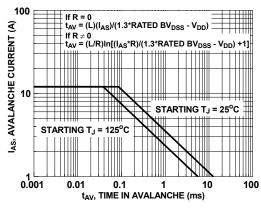


Figure 5. Forward Bias Safe Operating Area



NOTE: Refer to Fairchild Application Notes AN7514 and AN7515

Figure 6. Unclamped Inductive Switching

Capability

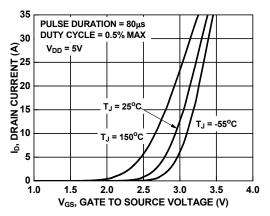


Figure 7. Transfer Characteristics

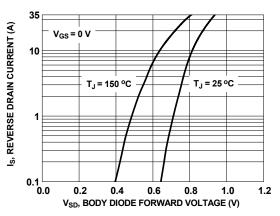


Figure 8. Forward Diode Characteristics

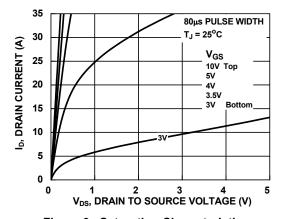


Figure 9. Saturation Characteristics

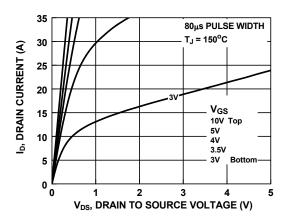


Figure 10. Saturation Characteristics

Typical Characteristics

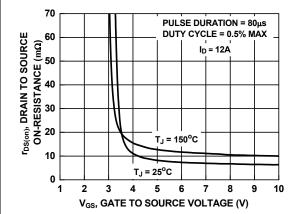


Figure 11. R_{DSON} vs. Gate Voltage

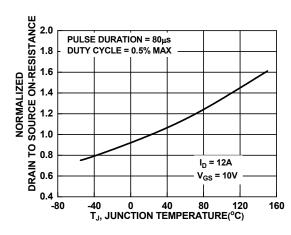


Figure 12. Normalized R_{DSON} vs. Junction Temperature

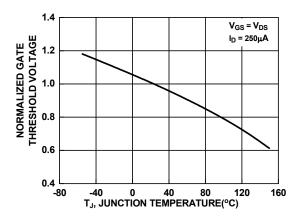


Figure 13. Normalized Gate Threshold Voltage vs. Temperature

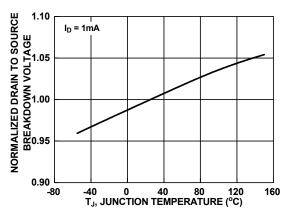


Figure 14. Normalized Drain to Source Breakdown Voltage vs. Junction Temperature

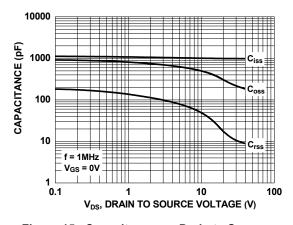


Figure 15. Capacitance vs. Drain to Source Voltage

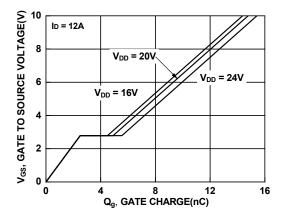


Figure 16. Gate Charge vs. Gate to Source Voltage







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