

DualCool™ N-Channel NexFET™ Power MOSFETs

Check for Samples: [CSD16321Q5C](#)

FEATURES

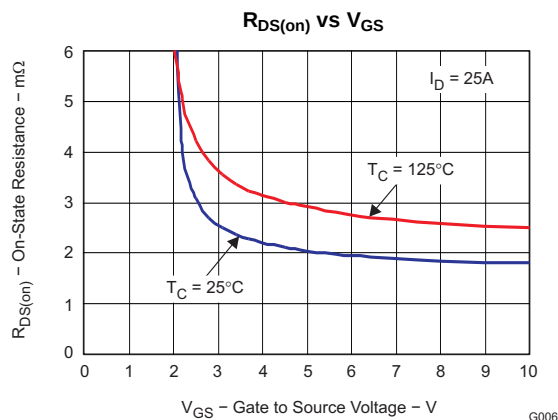
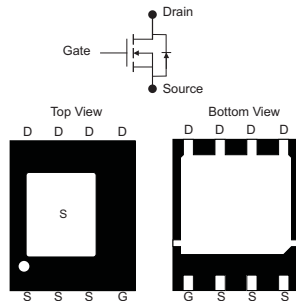
- DualCool™ Package SON 5×6mm
- Optimized for Two Sided Cooling
- Optimized for 5V Gate Drive
- Ultralow Q_g and Q_{gd}
- Low Thermal Resistance
- Avalanche Rated
- Pb Free Terminal Plating
- RoHS Compliant and Halogen Free

APPLICATIONS

- Point-of-Load Synchronous Buck in Networking, Telecom and Computing Systems
- Optimized for Synchronous FET Applications

DESCRIPTION

The NexFET™ power MOSFET has been designed to minimize losses in power conversion applications and optimized for 5V gate drive applications.



PRODUCT SUMMARY

V_{DS}	Drain to Source Voltage	25	V
Q_g	Gate Charge Total (4.5V)	14	nC
Q_{gd}	Gate Charge Gate to Drain	2.5	nC
$R_{DS(on)}$	Drain to Source On Resistance	$V_{GS} = 3V$	2.8 mΩ
		$V_{GS} = 4.5V$	2.1 mΩ
		$V_{GS} = 8V$	1.9 mΩ
$V_{GS(th)}$	Threshold Voltage	1.1	V

ORDERING INFORMATION

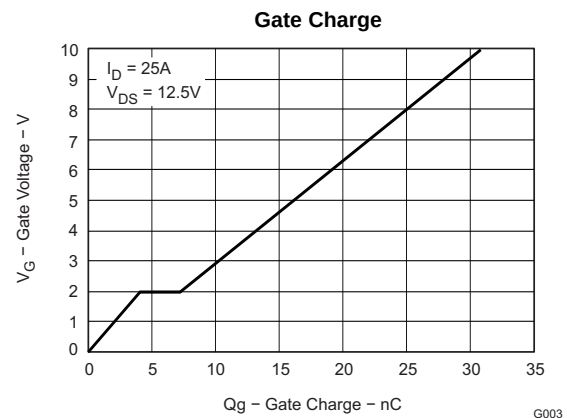
Device	Package	Media	Qty	Ship
CSD16321Q5C	SON 5×6-mm Plastic Package	13-Inch Reel	2500	Tape and Reel

ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ C$ unless otherwise stated		VALUE	UNIT
V_{DS}	Drain to Source Voltage	25	V
V_{GS}	Gate to Source Voltage	+10 / -8	V
I_D	Continuous Drain Current, $T_C = 25^\circ C$	100	A
	Continuous Drain Current ⁽¹⁾	31	A
I_{DM}	Pulsed Drain Current, $T_A = 25^\circ C$ ⁽²⁾	200	A
P_D	Power Dissipation ⁽¹⁾	3.1	W
T_J, T_{STG}	Operating Junction and Storage Temperature Range	-55 to 150	$^\circ C$
E_{AS}	Avalanche Energy, single pulse $I_D = 66A, L = 0.1mH, R_G = 25\Omega$	218	mJ

(1) Typical $R_{\theta JA} = 39^\circ C/W$ on 1-in² Cu (2-oz.) on a 0.060" thick FR4 PCB

(2) Pulse duration $\leq 300\mu s$, duty cycle $\leq 2\%$



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ELECTRICAL CHARACTERISTICS

(T_A = 25°C unless otherwise stated)

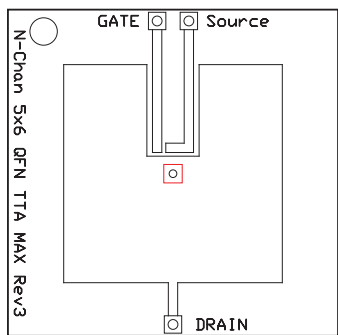
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Static Characteristics						
BV _{DSS}	Drain to Source Voltage	V _{GS} = 0V, I _D = 250μA	25			V
I _{DSS}	Drain to Source Leakage	V _{GS} = 0V, V _{DS} = 20V	1			μA
I _{GSS}	Gate to Source Leakage	V _{DS} = 0V, V _{GS} = +10/–8V	100			nA
V _{GS(th)}	Gate to Source Threshold Voltage	V _{DS} = V _{GS} , I _D = 250μA	0.9	1.1	1.4	V
R _{DS(on)}	Drain to Source On Resistance	V _{GS} = 3V, I _D = 25A		2.8	3.8	mΩ
		V _{GS} = 4.5V, I _D = 25A		2.1	2.6	mΩ
		V _{GS} = 8.0V, I _D = 25A		1.9	2.4	mΩ
g _{fs}	Transconductance	V _{DS} = 12.5V, I _D = 25A	150			S
Dynamic Characteristics						
C _{iss}	Input Capacitance	V _{GS} = 0V, V _{DS} = 12.5V, f = 1MHz	2360	3100	pF	
C _{oss}	Output Capacitance		1700	2200	pF	
C _{rss}	Reverse Transfer Capacitance		115	150	pF	
R _G	Series Gate Resistance		1.5	3	Ω	
Q _g	Gate Charge Total (4.5V)	V _{DS} = 12.5V, I _{DS} = 25A	14	19	nC	
Q _{gd}	Gate Charge – Gate to Drain		2.5	nC		
Q _{gs}	Gate Charge – Gate to Source		4	nC		
Q _{g(th)}	Gate Charge at V _{th}		2.1	nC		
Q _{oss}	Output Charge	V _{DS} = 13.3V, V _{GS} = 0V	36	nC		
t _{d(on)}	Turn On Delay Time	V _{DS} = 12.5V, V _{GS} = 4.5V, I _{DS} = 25A, R _G =2Ω	9	ns		
t _r	Rise Time		15	ns		
t _{d(off)}	Turn Off Delay Time		27	ns		
t _f	Fall Time		17	ns		
Diode Characteristics						
V _{SD}	Diode Forward Voltage	I _{DS} = 25A, V _{GS} = 0V	0.8	1	V	
Q _{rr}	Reverse Recovery Charge	V _{DD} = 13.3V, I _F = 25A, di/dt = 300A/μs	33	nC		
t _{rr}	Reverse Recovery Time		32	ns		

THERMAL CHARACTERISTICS

(T_A = 25°C unless otherwise stated)

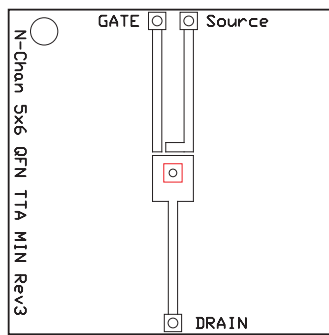
PARAMETER		MIN	TYP	MAX	UNIT
R _{θJC}	Thermal Resistance Junction to Case (Top Source) ⁽¹⁾			1.2	°C/W
R _{θJC}	Thermal Resistance Junction to Case (Bottom drain) ⁽¹⁾			1.1	°C/W
R _{θJA}	Thermal Resistance Junction to Ambient ⁽¹⁾⁽²⁾			48	°C/W

- (1) R_{θJC} is determined with the device mounted on a 1-inch² 2-oz. Cu pad on a 1.5 × 1.5-inch 0.060-inch thick FR4 board. R_{θJC} is specified by design, whereas R_{θCA} is determined by the user's board design.
- (2) Device mounted on FR4 material with 1-inch² of 2-oz. Cu.



M0137-01

Max $R_{\theta JA} = 48^{\circ}\text{C/W}$
when mounted on 1 in²
of 2-oz. Cu.

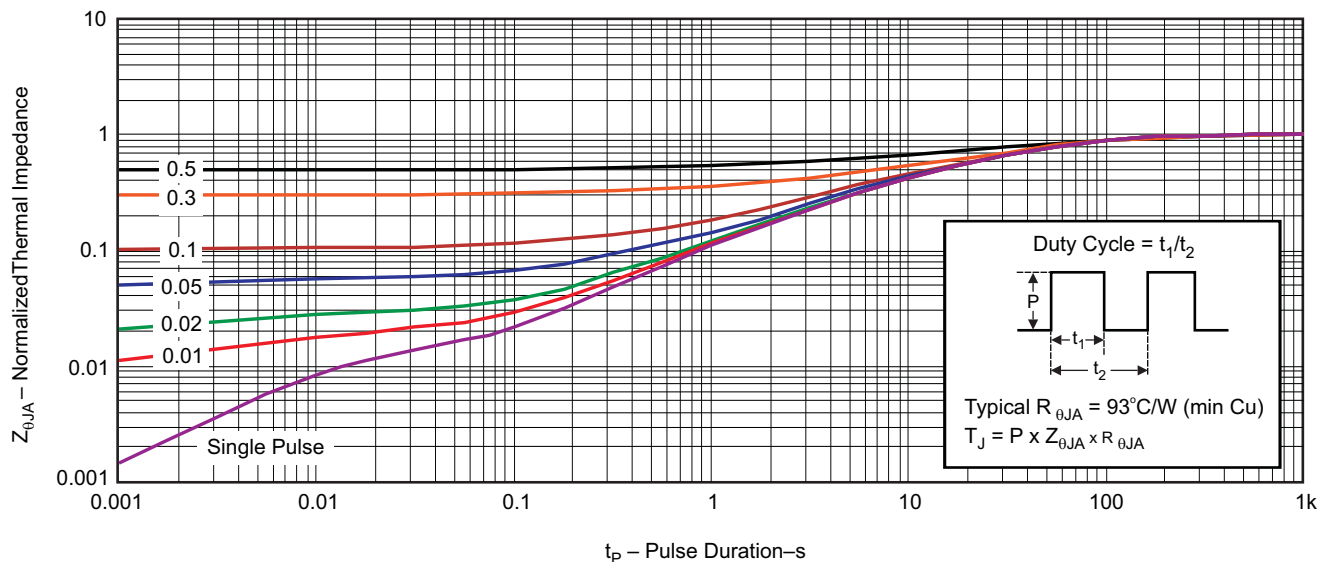


M0137-02

Max $R_{\theta JA} = 115^{\circ}\text{C/W}$
when mounted on
minimum pad area of
2-oz. Cu.

TYPICAL MOSFET CHARACTERISTICS

($T_A = 25^{\circ}\text{C}$ unless otherwise stated)



G012

Figure 1. Transient Thermal Impedance

TYPICAL MOSFET CHARACTERISTICS (continued)

($T_A = 25^\circ\text{C}$ unless otherwise stated)

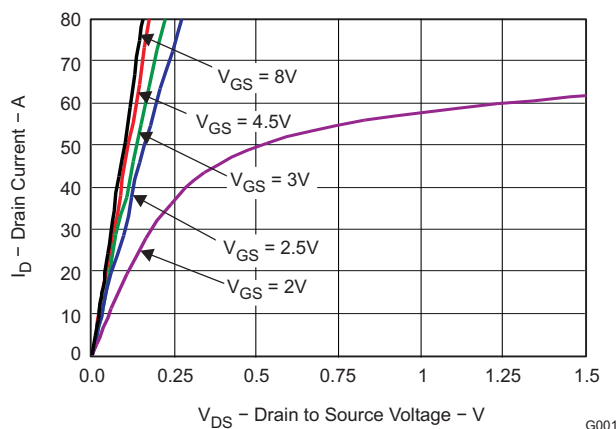


Figure 2. Saturation Characteristics

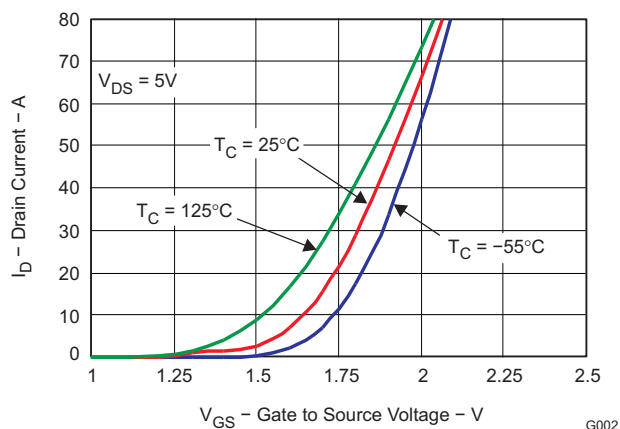


Figure 3. Transfer Characteristics

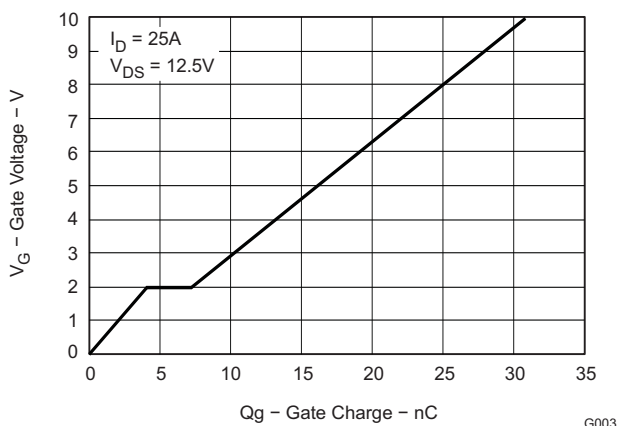


Figure 4. Gate Charge

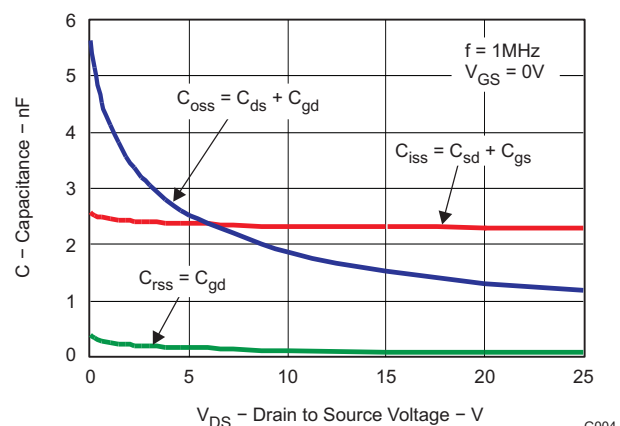


Figure 5. Capacitance

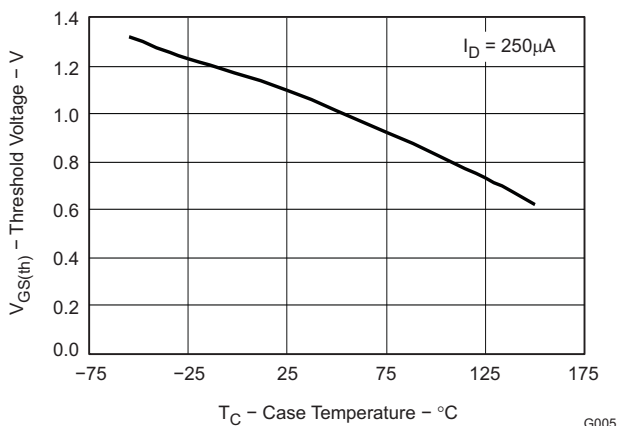


Figure 6. Threshold Voltage vs. Temperature

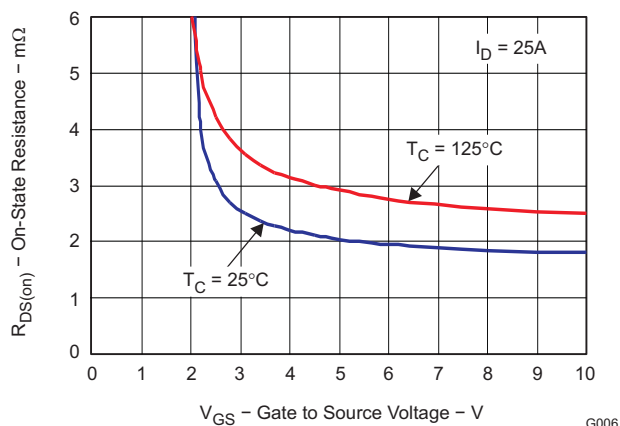


Figure 7. On Resistance vs. Gate Voltage

TYPICAL MOSFET CHARACTERISTICS (continued)

($T_A = 25^\circ\text{C}$ unless otherwise stated)

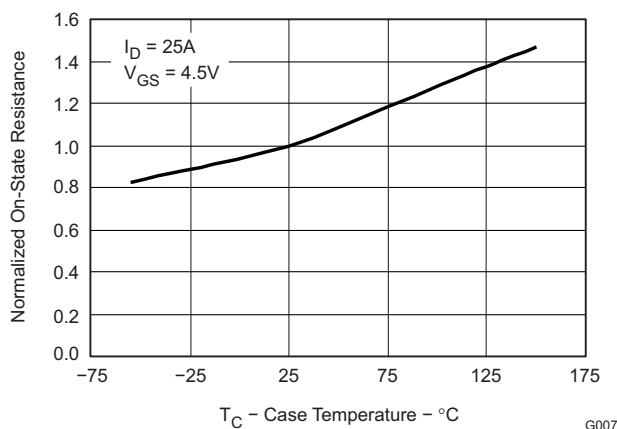


Figure 8. On Resistance vs. Temperature

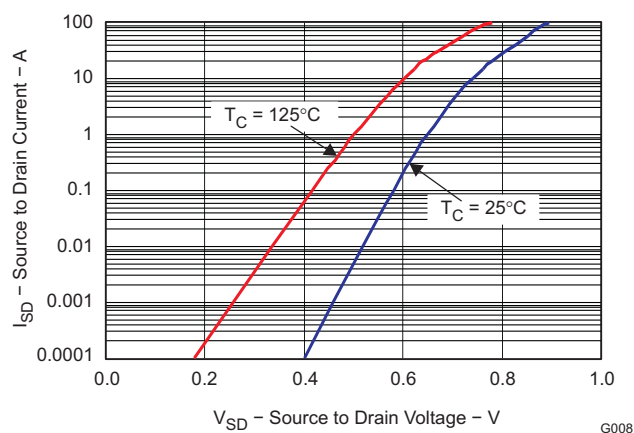


Figure 9. Typical Diode Forward Voltage

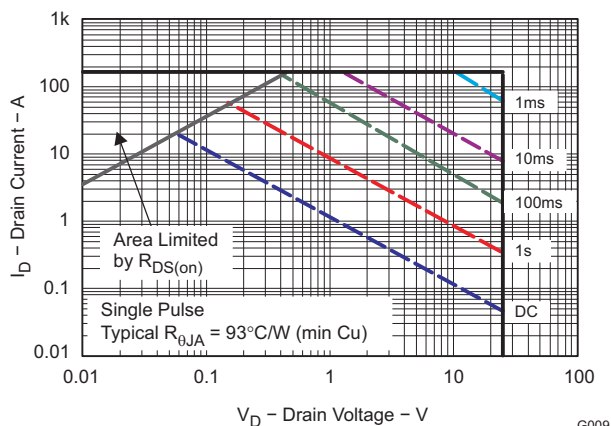


Figure 10. Maximum Safe Operating Area

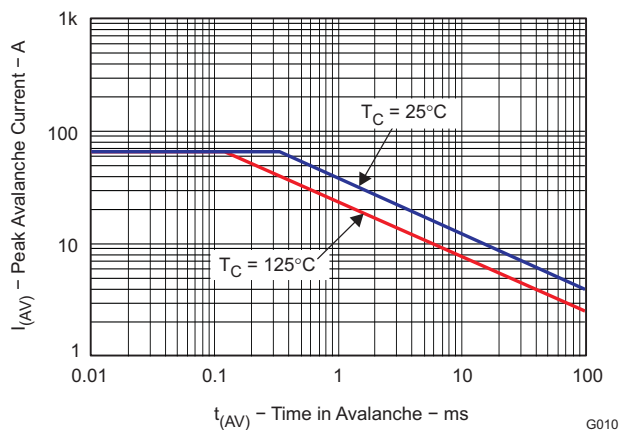


Figure 11. Single Pulse Unclamped Inductive Switching

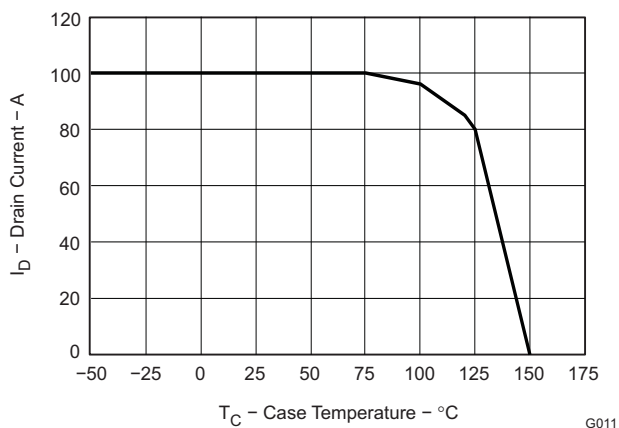
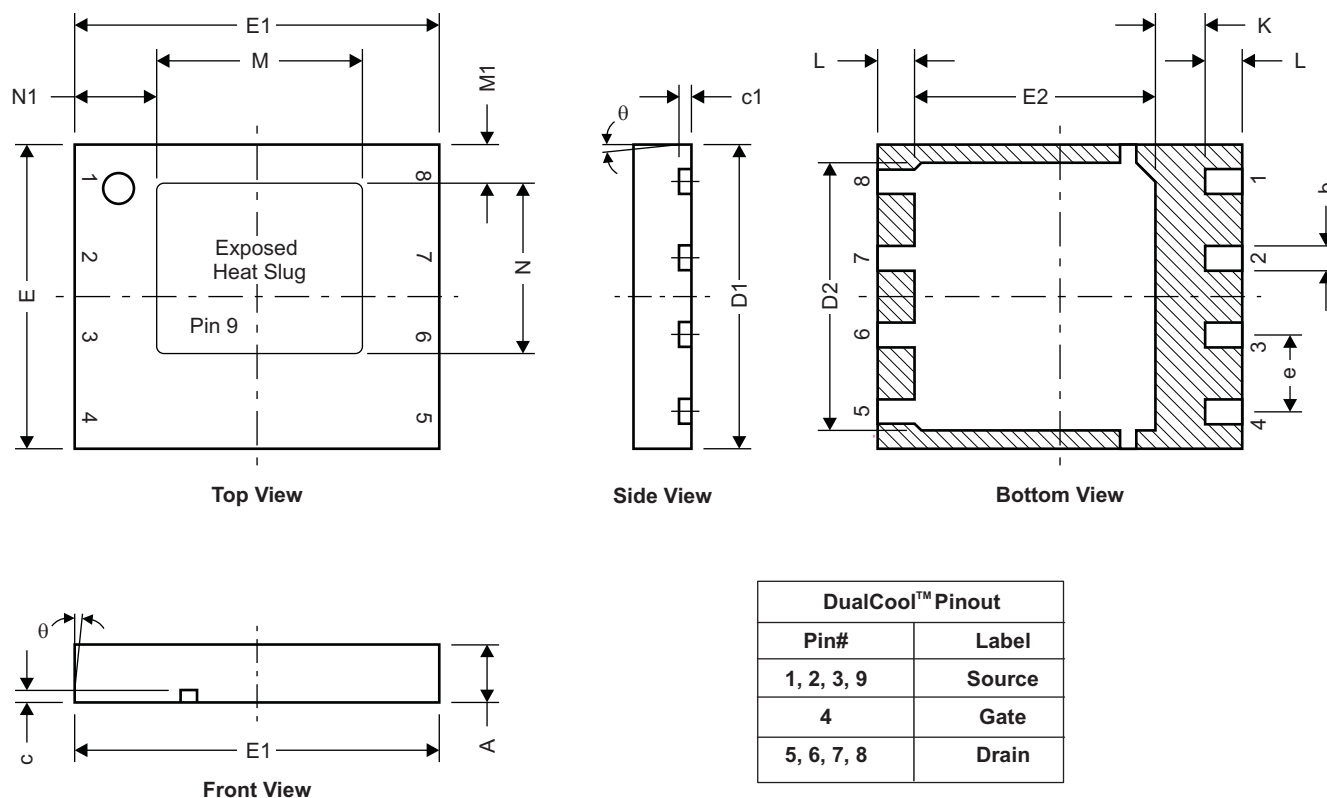


Figure 12. Maximum Drain Current vs. Temperature

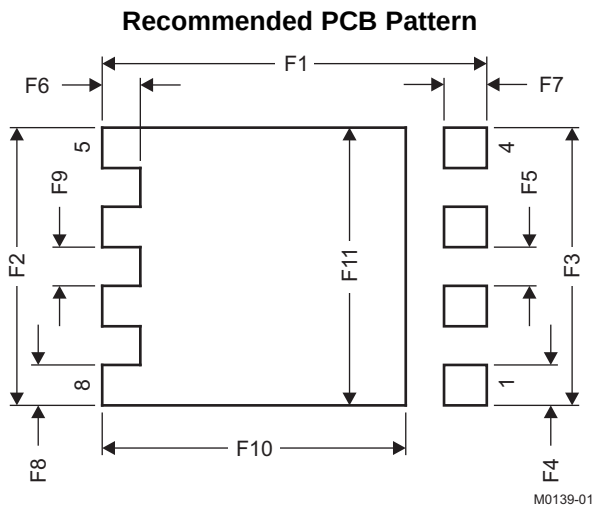
MECHANICAL DATA

Q5C Package Dimensions



M0162-01

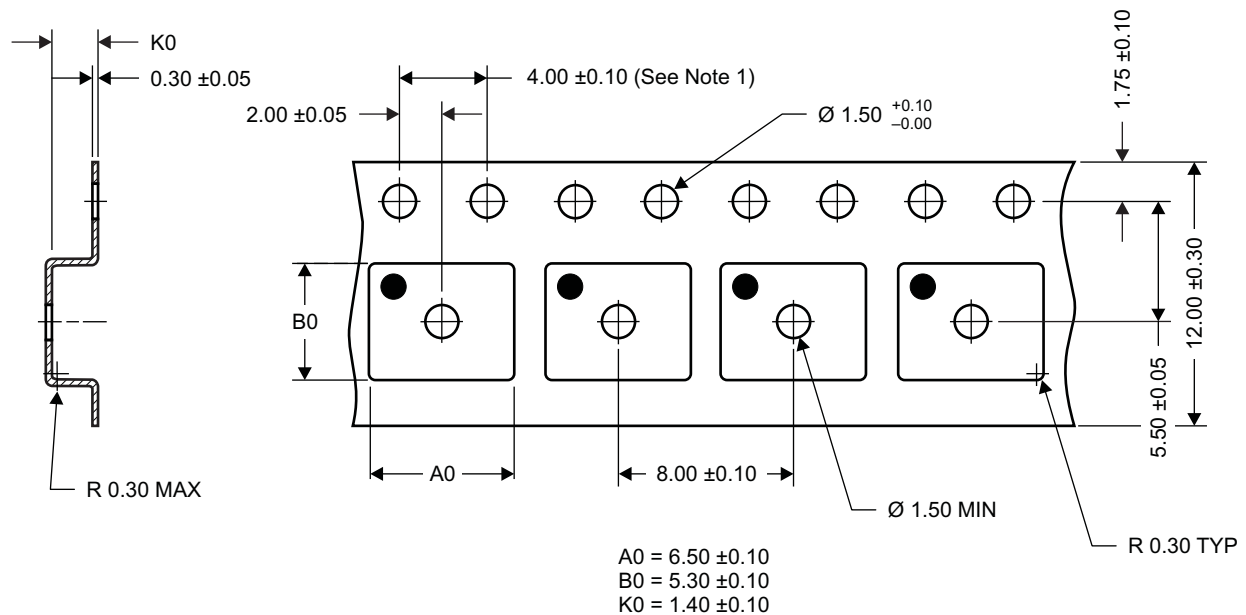
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.950	1.050	0.037	0.039
b	0.360	0.460	0.014	0.018
c	0.150	0.250	0.006	0.010
c1	0.150	0.250	0.006	0.010
D1	4.900	5.100	0.193	0.201
D2	4.320	4.520	0.170	0.178
E	4.900	5.100	0.193	0.201
E1	5.900	6.100	0.232	0.240
E2	3.920	4.12	0.154	0.162
e	1.27 TYP		0.050	
L	0.510	0.710	0.020	0.028
θ	–	–	–	–
K	0.760	–	0.030	–
M	3.260	3.460	0.128	0.136
M1	0.520	0.720	0.020	0.028
N	2.720	2.920	0.107	0.115
N1	1.227	1.427	0.048	0.056



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
F1	6.205	6.305	0.244	0.248
F2	4.46	4.56	0.176	0.18
F3	4.46	4.56	0.176	0.18
F4	0.65	0.7	0.026	0.028
F5	0.62	0.67	0.024	0.026
F6	0.63	0.68	0.025	0.027
F7	0.7	0.8	0.028	0.031
F8	0.65	0.7	0.026	0.028
F9	0.62	0.67	0.024	0.026
F10	4.9	5	0.193	0.197
F11	4.46	4.56	0.176	0.18

For recommended circuit layout for PCB designs, see application note [SLPA005 – Reducing Ringing Through PCB Layout Techniques](#).

Q5C Tape and Reel Information



Notes:

- 10-sprocket hole-pitch cumulative tolerance ± 0.2
- Camber not to exceed 1mm in 100mm, noncumulative over 250mm
- Material: black static-dissipative polystyrene
- All dimensions are in mm, unless otherwise specified.
- A0 and B0 measured on a plane 0.3mm above the bottom of the pocket
- MSL1 260°C (IR and convection) PbF reflow compatible

REVISION HISTORY

Changes from Original (December 2009) to Revision A	Page
Changed the Mechanical Data dimensions table. Added dimensions for M, M1, N and N1	6
Changes from Revision A (January 2010) to Revision B	Page
- Changed $R_{DS(on)}$ - $V_{GS} = 3V$, $I_D = 25A$ MAX value From: 3.5 To: 3.8 - Deleted the Package Marking Information section	2 7

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