ISL9120

Compact High Efficiency Low Power Buck-Boost Regulator

FN8659
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The ISL9120 is a highly integrated buck-boost switching regulator that accepts input voltages either above or below the regulated output voltage. This regulator automatically transitions between buck and boost modes without significant output disturbance. The ISL9120 also has automatic bypass functionality. When the input voltage is generally within 1% to 2% of the output voltage, there will be a direct bypass connection between the VIN and VOUT pins. In addition to the automatic bypass functionality, the ISL9120 also has forced bypass functionality with the use of the BYP pin.

This device is capable of delivering up to 800mA of output current (V_{IN} = 2.5V, V_{OUT} = 3.3V) and provides excellent efficiency due to its adaptive current limit Pulse Frequency Modulation (PFM) control architecture.

The ISL9120 is designed for stand-alone applications and supports a 3.3V fixed output voltage or variable output voltages with an external resistor divider. The forced bypass power saving mode can be chosen if voltage regulation is not required. The device consumes less than 3.5µA of current over the operating temperature range in forced bypass mode.

The ISL9120 requires only a single inductor and very few external components. Power supply solution size is minimized by a 1.41mmx1.41mm WLCSP.

Features

- Accepts input voltages above or below regulated output voltage
- Automatic bypass mode functionality
- Automatic and seamless transitions between buck and boost modes
- Input voltage range: 1.8V to 5.5V
- Selectable forced bypass power saving mode
- Adaptive multilevel current limit scheme to optimize efficiency at low and high currents
- Output current: up to 800mA (V_{IN} = 2.5V, V_{OUT} = 3.3V)
- High efficiency: up to 98%
- 41µA quiescent current maximizes light-load efficiency
- Fully protected for over-temperature and undervoltage
- Small 1.41m x 1.41mm WLCSP

Applications

- Smartphones and tablets
- Portable consumer and wearable devices

Related Literature

- For a full list of related documents, visit our website
  - ISL9120 product page

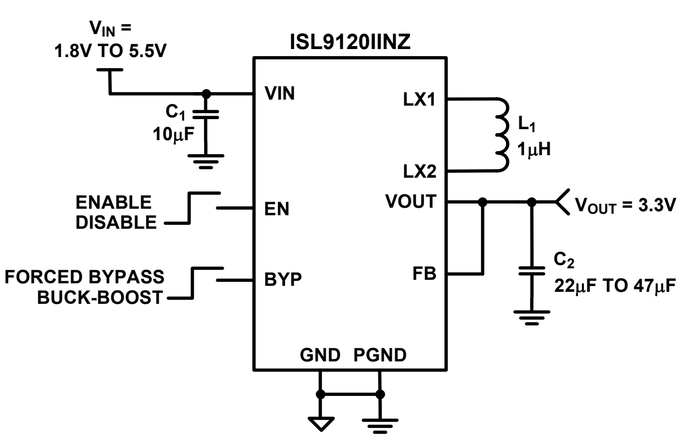


FIGURE 1. TYPICAL FIXED OUTPUT APPLICATION

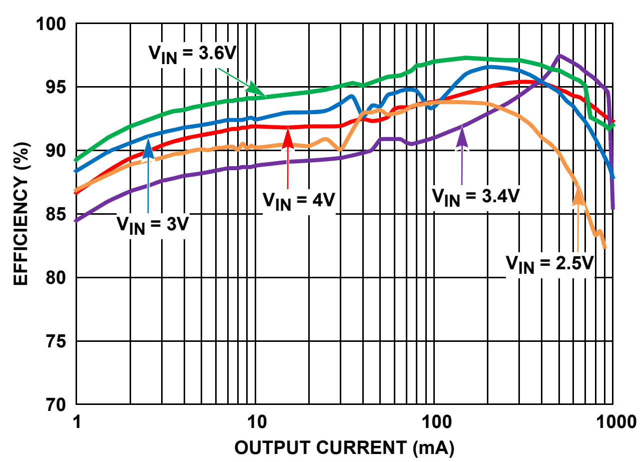


FIGURE 2. EFFICIENCY: V_{OUT} = 3.3V, T_A = +25°C

Block Diagram

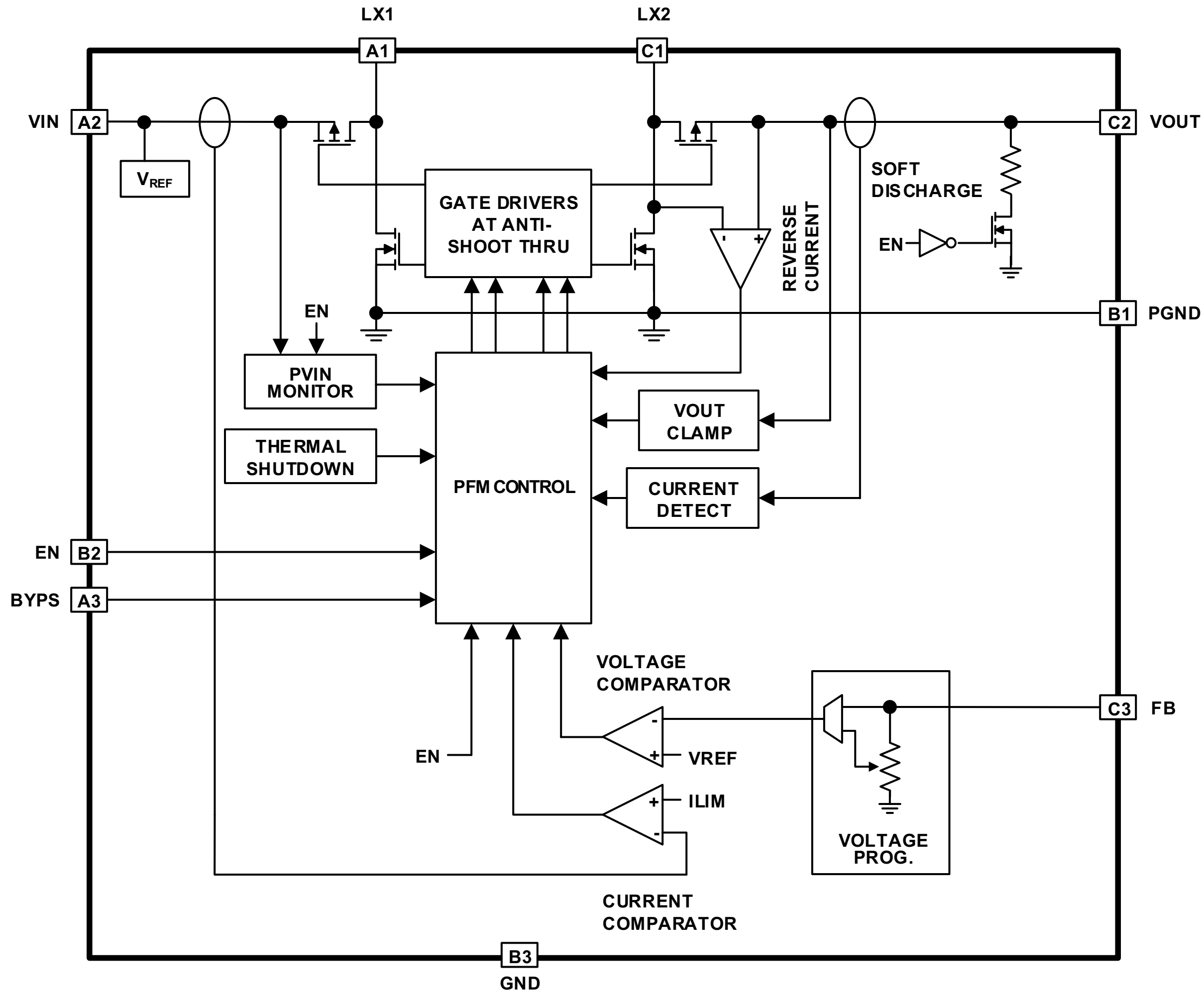
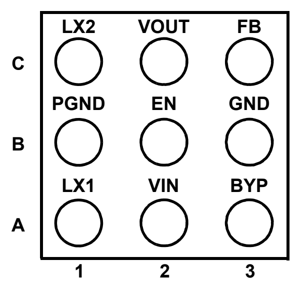


FIGURE 3. BLOCK DIAGRAM

Pin Configuration

ISL9120
9 BUMP WLCSP
BOTTOM VIEW



Pin Descriptions

PIN #	PIN NAMES	DESCRIPTION
C1	LX2	Inductor connection, output side.
C2	VOUT	Buck-boost output. Connect a 22µF or 47µF capacitor to PGND.
C3	FB	Voltage feedback pin, connect directly to VOUT pin for fixed output version.
B1	PGND	Power ground for high switching current.
B2	EN	Logic input, drive HIGH to enable device. Do not leave floating.
B3	GND	Analog ground pin.
A1	LX1	Inductor connection, input side.
A2	VIN	Power supply input. Range: 1.8V to 5.5V. Connect a 10µF capacitor to PGND.
A3	BYP	Forced bypass mode enable pin. Logic high for forced bypass mode operation. Logic low for buck-boost mode operation. Do not leave floating.

Ordering Information

PART NUMBER (Notes 1, 2, 3)	PART MARKING	VOUT (V)	TEMP RANGE (°C)	TAPE AND REEL QUANTITY (UNITS)	PACKAGE (RoHS Compliant)	PKG. DWG. #
ISL9120IINZ-T	120N	3.3	-40 to +85	3k	9 Bump WLCSP	W3x3.9E
ISL9120IIAZ-T	120A	ADJ.	-40 to +85	3k	9 Bump WLCSP	W3x3.9E
ISL9120IINZ-T7A	120N	ADJ.	-40 to +85	250	9 Bump WLCSP	W3x3.9E
ISL9120IIAZ-T7A	120A	ADJ.	-40 to +85	250	9 Bump WLCSP	W3x3.9E
ISL9120IIN-EVZ	Evaluation Board for ISL9120IINZ					
ISL9120IIA-EVZ	Evaluation Board for ISL9120IIAZ					

NOTES:

1. Refer to TB347 for details on reel specifications.
2. These Intersil Pb-free WLCSP and BGA packaged products employ special Pb-free material sets, molding compounds/die attach materials, and SnAgCu -e1 solder ball terminals, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free WLCSP and BGA packaged products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), see the product information page for ISL9120. For more information on MSL, see TB363.

Absolute Maximum Ratings

VIN . . . . -0.3V to 6.5V
LX1, LX2. . . . . -0.3V to 6.5V
FB (Adjustable Version) . . . . -0.3V to 2.7V
FB (Fixed V_{OUT} Version) . . . . -0.3V to 6.5V
GND, PGND . . . . -0.3V to 0.3V
All Other Pins . . . . -0.3V to 6.5V
ESD Rating
Human Body Model (Tested per JESD22-A114F). 2.5kV
Machine Model (Tested per JESD22-A115C) 200V
Charged Device Model (Tested per JESD22-C101F). 2kV
Latch-Up (Tested per JESD78D; Class 2) 100mA

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JB} (°C/W)
1.41x1.41 WLCSP (Notes 4, 5).	95	27

Maximum Junction Temperature . . . .+125°C
Storage Temperature Range. . . . .-65°C to +150°C
Pb-Free Reflow Profile . . . . see TB493

Recommended Operating Conditions

Temperature Range . . . .-40°C to +85°C
Supply Voltage (V_{IN}) Range. . . . . 1.8V to 5.5V
Load Current (I_{OUT}) Range (DC) . . . . 0A to 800mA

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board with “direct attach” features. See TB379
5. For $\theta_{JB,}$ the "board temp" is taken on the board near the edge of the package, on a copper trace at the center of one side. See TB379.

Analog Specifications

V_{IN} = V_{EN} = 3.6V, V_{OUT} = 3.3V, L_1 = 1µH, C_1 = 10µF, C_2 = 47µF, T_A = +25°C. **Boldface limits apply across the recommended operating temperature range, -40°C to +85°C and input voltage range (1.8V to 5.5V).**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
POWER SUPPLY						
Input Voltage Range	V_{IN}		**1.8**		**5.5**	V
V_{IN} Undervoltage Lockout Threshold	V_{UVLO}	Rising		1.725	**1.790**	V
		Falling	**1.550**	1.650		V
V_{IN} Supply Current	I_{VIN}	V_{OUT} = 3.7V (Note 7)		41	**55**	µA
V_{IN} Supply Current, Shutdown	I_{SD}	EN = GND		0.005	**1**	µA
V_{IN} Supply Current, Bypass Mode	I_{BYP}	BYP = Logic high, V_{IN} ≤5V		0.8	**3.5**	µA
OUTPUT VOLTAGE REGULATION						
Output Voltage Range	V_{OUT}	ISL9120IIAZ, I_{OUT} = 100mA	**1.00**		**5.20**	V
Output Voltage Accuracy		V_{IN} = 3.7V, I_{OUT} = 1mA	**-3**		**+4**	%
FB Pin Voltage Regulation	V_{FB}	For adjustable output version (ISL9120IIAZ)		0.80		V
FB Pin Bias Current	I_{FB}	For adjustable output version (ISL9120IIAZ)			**0.025**	µA
Line Regulation, 500mA	$\Delta V_{OUT}/ \Delta V_{IN}$	I_{OUT} = 500mA, V_{OUT} = 3.3V, V_{IN} step from 2.3V to 5.5V		0.00681		mV/mV
Load Regulation, 500mA	$\Delta V_{OUT}/ \Delta I_{OUT}$	V_{IN} = 3.7V, V_{OUT} = 3.3V, I_{OUT} step from 0mA to 500mA		0.0072		mV/mA
Line Regulation, 100mA	$\Delta V_{OUT}/\Delta V_I$	I_{OUT} = 100mA, V_{OUT} = 3.3V, V_{IN} step from 2.3V to 5.5V		0.00273		mV/mV
Load Regulation, 100mA	$\Delta V_{OUT}/ \Delta I_{OUT}$	V_{IN} = 3.7V, V_{OUT} = 3.3V, I_{OUT} step from 0mA to 100mA		0.05		mV/mA
Output Voltage Clamp	V_{CLAMP}	Rising	**5.32**		**5.82**	V
Output Voltage Clamp Hysteresis				400		mV
DC/DC SWITCHING SPECIFICATIONS						
LX1 Pin Leakage Current	$I_{PFETLEAK}$		**-0.05**		**+0.05**	µA
LX2 Pin Leakage Current	$I_{NFETLEAK}$	V_{IN} = 3.6V	**-0.05**		**+0.05**	µA

Analog Specifications

$V_{IN} = V_{EN}$ = 3.6V, V_{OUT} = 3.3V, L_1 = 1µH, C_1 = 10µF, C_2 = 47µF, T_A = +25°C. **Boldface limits apply across the recommended operating temperature range, -40°C to +85°C and input voltage range (1.8V to 5.5V). (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
SOFT-START AND SOFT DISCHARGE						
Soft-Start Time	t_{SS}	Time from when EN signal asserts to when output voltage ramp starts.		1		ms
		Time from when output voltage ramp starts to when output voltage reaches 95% of its nominal value with device operating in buck mode. V_{IN} = 4V, I_{OUT} = 500mA		1		ms
		Time from when output voltage ramp starts to when output voltage reaches 95% of its nominal value with device operating in boost mode. V_{IN} = 3V, I_{OUT} = 500mA		1		ms
VOUT Soft-Discharge ON-Resistance	r_{DISCHG}	EN < V_{IL}		110		Ω
POWER MOSFET						
P-Channel MOSFET ON-Resistance	r_{DSON_P}	I_{OUT} = 200mA, measured with internal test mode		50		mΩ
N-Channel MOSFET ON-Resistance	r_{DSON_N}	I_{OUT} = 200mA, measured with internal test mode		50		mΩ
INDUCTOR PEAK CURRENT LIMIT						
Maximum Peak Current Limit	I_{LIM_MAX}			2		A
THERMAL PROTECTION						
Thermal Shutdown				150		°C
Thermal Shutdown Hysteresis				35		°C
LOGIC INPUTS						
Input Leakage	I_{LEAK}			0.013	**0.500**	µA
Input HIGH Voltage	V_{IH}		**1.4**			V
Input LOW Voltage	V_{IL}				**0.4**	V

NOTES:

6. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
7. Quiescent current measurements are taken when the output is not switching.

Typical Performance Curves

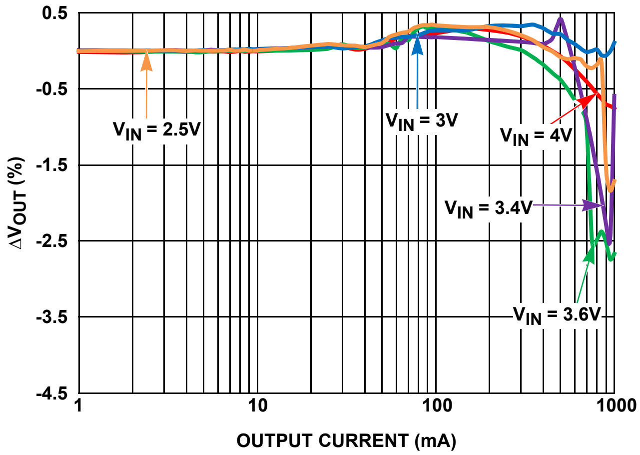


FIGURE 4. OUTPUT VOLTAGE vs OUTPUT CURRENT

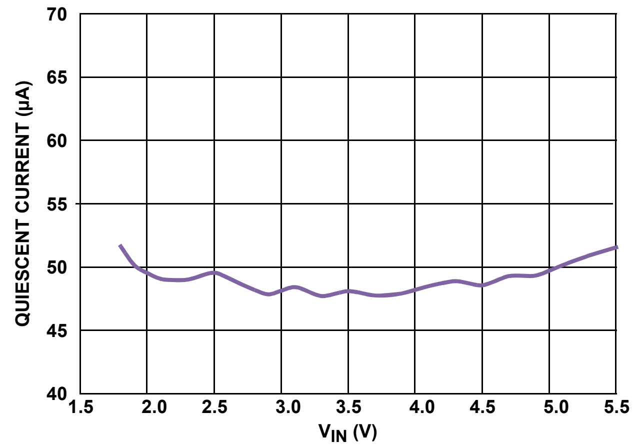


FIGURE 5. QUIESCENT CURRENT vs INPUT VOLTAGE (EN = HIGH)

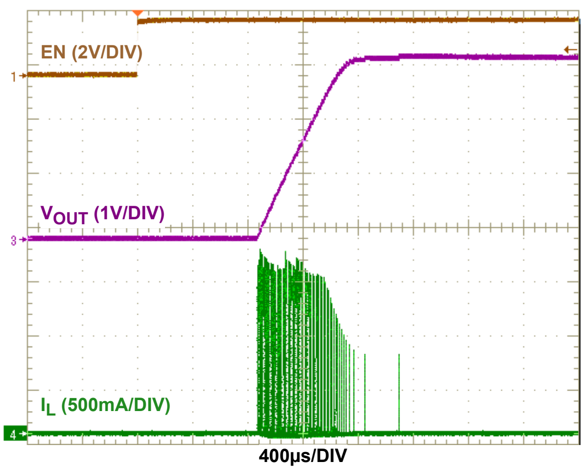


FIGURE 6. SOFT-START (V_{IN} = 4V, V_{OUT} = 3.3V, NO LOAD)

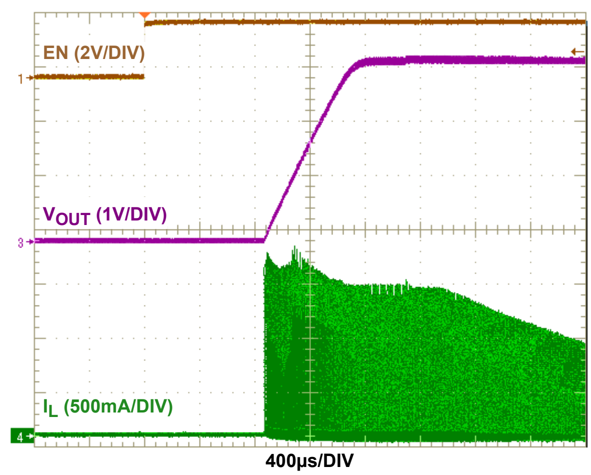


FIGURE 7. SOFT-START (V_{IN} = 4V, V_{OUT} = 3.3V, 0.5A R_{LOAD})

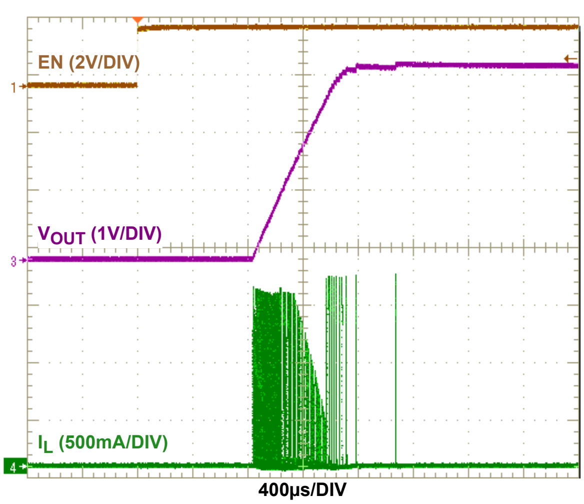


FIGURE 8. SOFT-START (V_{IN} = 3V, V_{OUT} = 3.3V, NO LOAD)

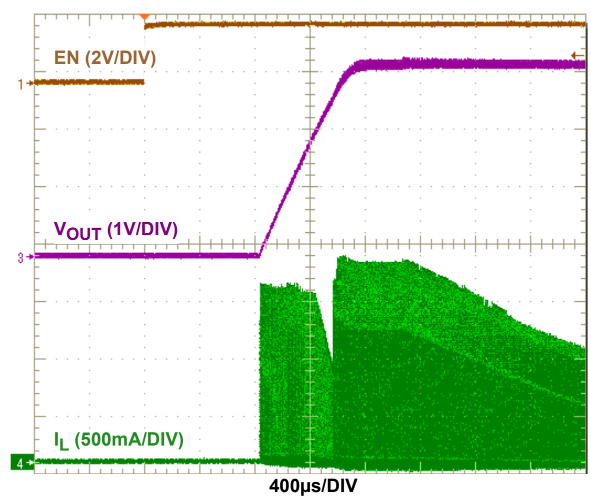


FIGURE 9. SOFT-START (V_{IN} = 3V, V_{OUT} = 3.3V, 0.5A R_{LOAD})

Typical Performance Curves (Continued)

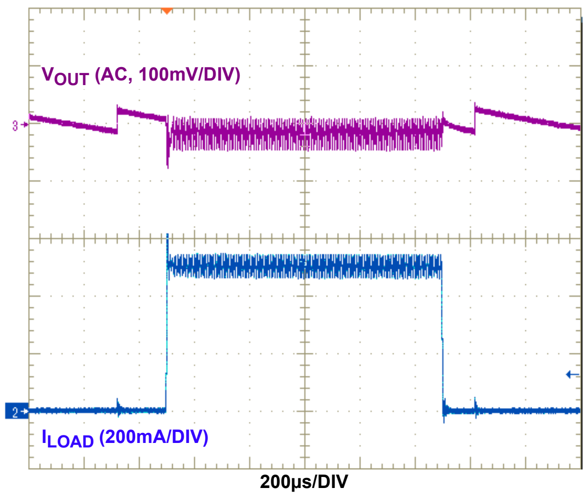


FIGURE 10. 0A TO 0.5A LOAD TRANSIENT (V_{IN} = 4V, V_{OUT} = 3.3V)

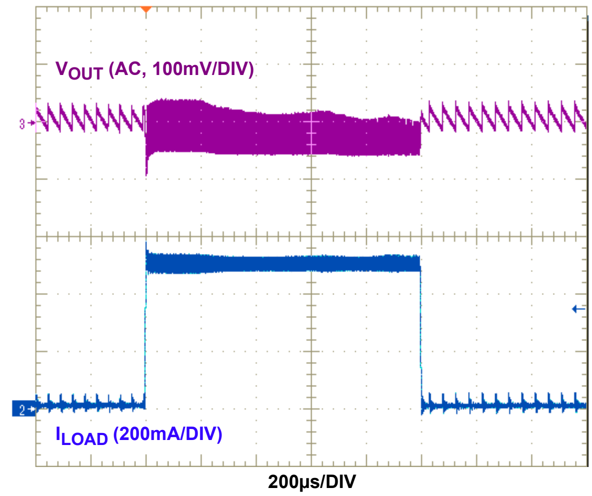


FIGURE 11. 0.01A TO 0.5A LOAD TRANSIENT (V_{IN} = 4V, V_{OUT} = 3.3V)

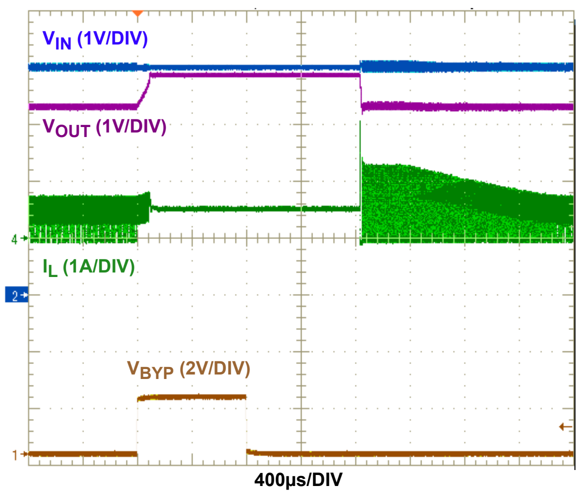


FIGURE 12. BYPASS FUNCTIONALITY (V_{IN} = 4V, V_{OUT} = 3.3, 0.5A R_{LOAD})

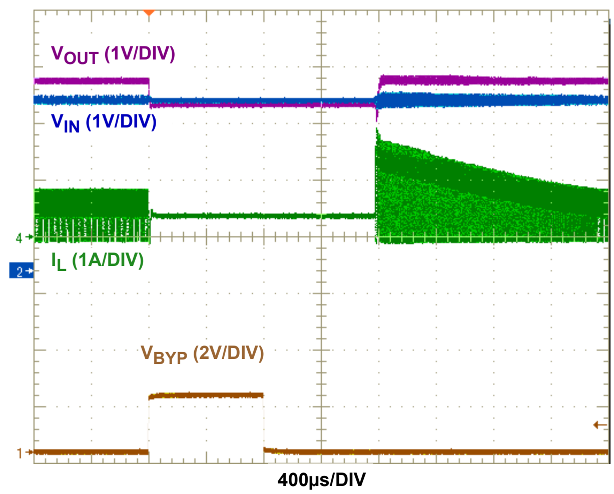


FIGURE 13. BYPASS FUNCTIONALITY (V_{IN} = 3V, V_{OUT} = 3.3, 0.5A R_{LOAD})

Functional Description

Functional Overview

The ISL9120 implements a complete buck-boost switching regulator with a PFM controller, internal switches, references, protection circuitry, and control inputs. Refer to the "Block Diagram" on page 2.

The PFM controller automatically switches between buck and boost modes as necessary to maintain a steady output voltage with changing input voltages and dynamic external loads.

Internal Supply and References

As shown in the "Block Diagram" on page 2, the VIN pin supplies input power to the DC/DC converter and also provides the operating voltage source required for stable V_{REF} generation. Separate ground pins (GND and PGND) are provided to avoid problems caused by ground shift due to the high switching currents.

Enable Input

A master enable pin, EN, allows the device to be enabled. Driving EN logic low invokes a power-down mode, where most internal device functions, including input and output power-good detection, are disabled.

Bypass Input

The BYP pin allows the device to provide a direct connection from the VIN pin to the VOUT pin. The connection between the VIN and VOUT pins is through the external inductor and two internal power transistors. This function, called forced bypass mode operation, provides a very low quiescent current state.

For forced bypass mode operation, the minimum time required while in forced bypass operation is 800µs. Also when exiting forced bypass operation, the minimum time required before reentering forced bypass mode operation is 1ms.

Soft Discharge

When the device is disabled by driving EN logic low, an internal resistor between the VOUT and GND pins is activated. This internal resistor has a typical resistance of 110Ω.

POR Sequence and Soft-Start

Bringing the EN pin logic high allows the device to power-up. A number of events occur during the start-up sequence. The internal voltage reference powers up and stabilizes. The device then starts operating. There is a 1ms (typical) delay between assertion of the EN pin and the start of the switching regulator soft-start ramp.

The soft-start feature minimizes output voltage overshoot and input inrush currents. During soft-start, the reference voltage is ramped to provide a ramping output voltage.

When the target output voltage is higher than the input voltage, there will be a transition from buck mode to boost mode during the soft-start sequence. At the time of this transition, the ramp rate of the reference voltage is decreased, such that the output voltage slew rate is decreased. This provides a slower output voltage slew rate.

Undervoltage Lockout

The Undervoltage Lockout (UVLO) feature prevents abnormal operation if the supply voltage is too low to guarantee proper operation. When the VIN pin voltage falls below the UVLO threshold, the regulator is disabled.

Thermal Shutdown

A built-in thermal protection feature protects the ISL9120 if the die temperature reaches +150°C (typical). At this die temperature, the regulator is completely shut down. The die temperature continues to be monitored in this thermal shutdown mode. When the die temperature falls to +115°C (typical), the device will resume normal operation.

When exiting thermal shutdown, the ISL9120 will execute its soft-start sequence.

Buck-Boost Conversion Topology

The ISL9120 operates in either buck or boost mode. When operating in conditions where V_{IN} is close to V_{OUT}, the ISL9120 alternates between buck mode, boost mode, and automatic bypass modes of operation as necessary to provide a regulated output voltage.

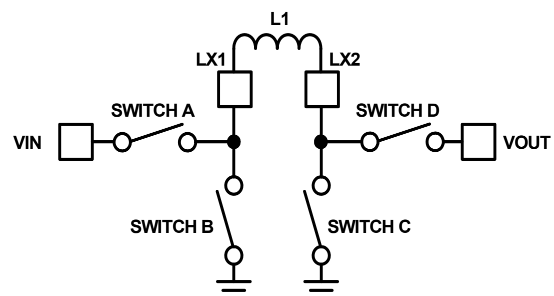


FIGURE 14. BUCK-BOOST TOPOLOGY

Figure 14 shows a simplified diagram of the internal switches and external inductor.

PFM Operation

During PFM operation in buck mode, Switch D is continuously closed and Switch C is continuously open. Switches A and B operate in discontinuous mode during PFM operation. During PFM operation in boost mode, the ISL9120 closes Switch A and Switch C to ramp-up the current in the inductor. When the inductor current reaches the current limit, the device turns OFF Switches A and C, then turns ON Switches B and D. With Switches B and D closed, output voltage increases as the inductor current ramps down.

As shown in Figure 15, depending on output current, there will be multiple PFM pulses to charge up the output capacitor. These pulses continue until V_{OUT} has reached the upper threshold of the PFM hysteretic, which is at 1.5% above the nominal output voltage. Switching then stops and remains stopped until V_{OUT} decays to the lower threshold of the voltage hysteretic, which is the nominal output voltage. Then the PFM operation repeats.

Variable Peak Current Limit Scheme

To optimize efficiency across the output current range, the ISL9120 implements a multilevel current limit scheme with 32 levels between 350mA and 2A. The transition from one level to the other is determined by the number of pulses in a PFM burst (pulse count) as shown in Figure 16. At a given peak current limit level, the pulse count increases as the output current increases. When the pulse count reaches the upper threshold at the existing current limit, the current limit will switch to the next higher level. Similarly, if the pulse count reaches the lower threshold at the existing current limit, the device will switch to the next lower level of peak current limit. If the pulse count reaches the upper threshold at the highest current limit, the current limit will not rise any further. Increasing the output current beyond this point may cause the output to lose voltage regulation.

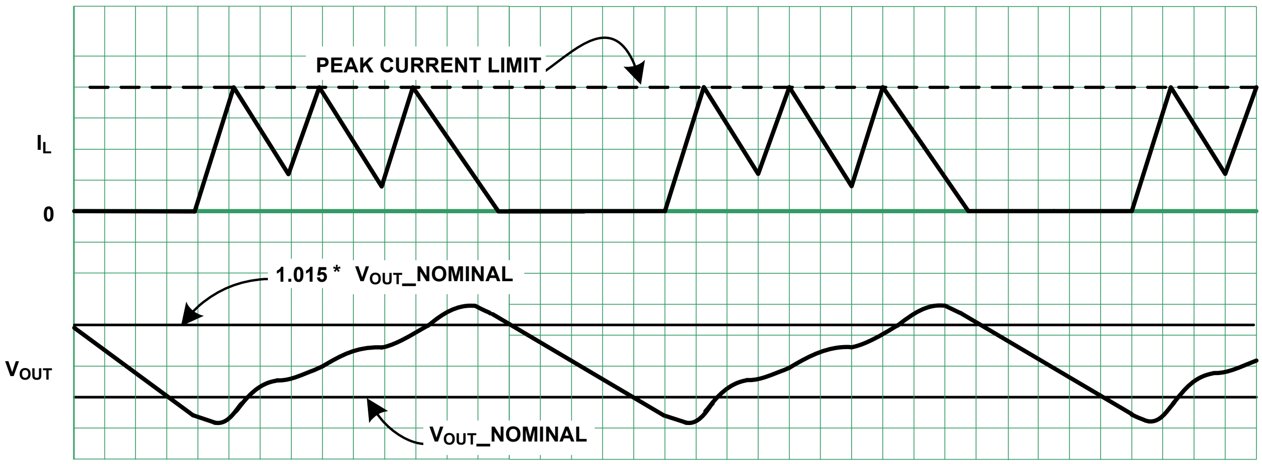


FIGURE 15. PFM MODE OPERATION CONCEPT

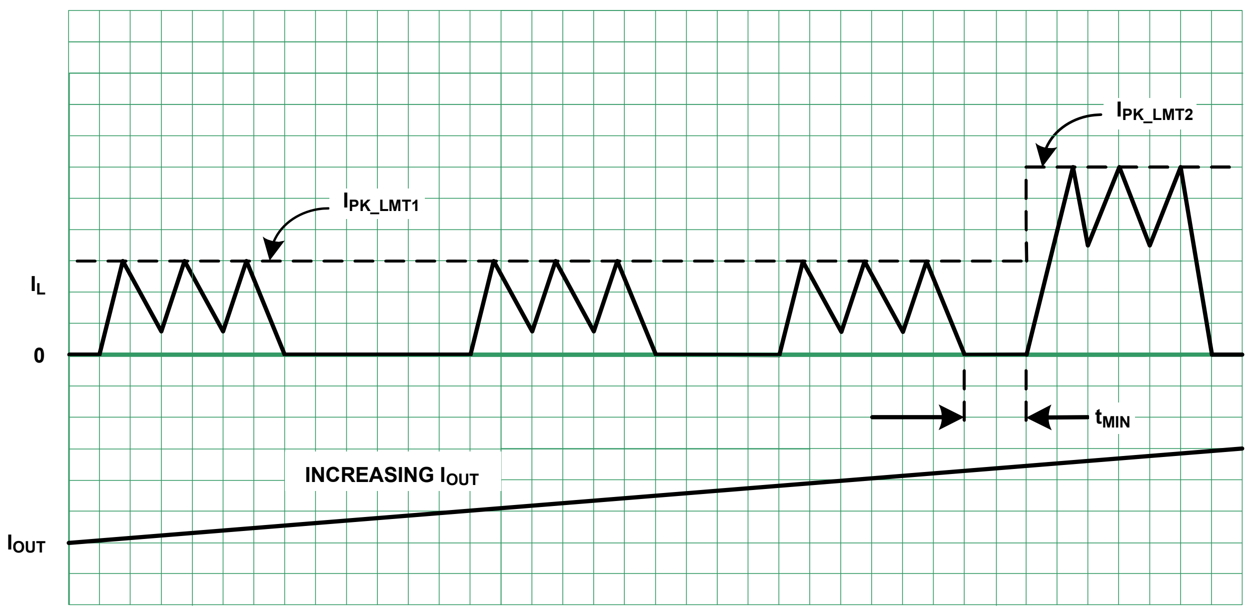


FIGURE 16. PEAK CURRENT LIMIT STEP UP TRANSITION

Automatic Bypass Mode Operation

When the output voltage is close to the input voltage, generally within 1% to 2%, the ISL9120 will engage automatic bypass mode operation, which produces a direct connection between the VIN and VOUT pins. This behavior provides excellent efficiency and very low output voltage ripple.

Forced Bypass Mode Operation

Forced bypass mode operation is intended for applications where the output regulation is not important but the device quiescent current consumption is important. One example is when the buck-boost regulator is providing power to an LDO and the LDO is in standby mode with near zero output current. Under this condition, putting the buck-boost regulator in bypass mode will have essentially no impact on the LDO but save the 41µA quiescent current consumption on the buck-boost regulator.

Because the bypass mode is an extreme power saving mode, there is no overcurrent protection. Therefore, caution must be taken not to overload or short-circuit the device. Power-up at bypass mode is not recommended.

Output Voltage Programming

The ISL9120 is available in fixed and adjustable output voltage versions. To use the fixed output version (ISL9120IINZ), the VOUT pin must be connected directly to the FB pin.

In the adjustable output voltage version (ISL9120IIAZ), an external resistor divider is required to program the output voltage.

Applications Information

Component Selection

The fixed-output version of the ISL9120 requires only three external power components to implement the buck-boost converter: an inductor, an input capacitor, and an output capacitor.

The adjustable ISL9120 versions require three additional components to program the output voltage. Two external resistors program the output voltage and a small capacitor is added to improve transient response.

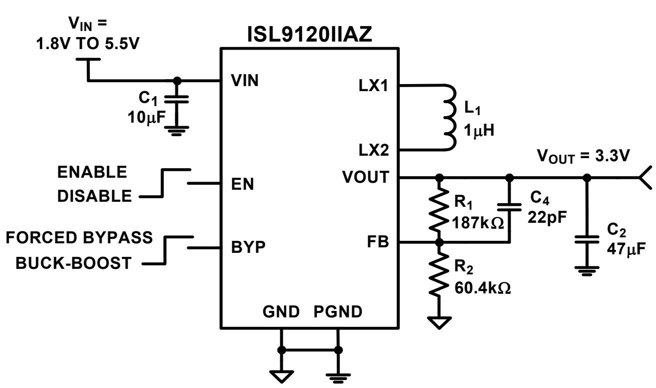


FIGURE 17. TYPICAL ISL9120IIAZ APPLICATION

Output Voltage Programming, Adjustable Version

Setting and controlling the output voltage of the ISL9120IIAZ (adjustable output version) can be accomplished by selecting the external resistor values.

Equation 1 can be used to derive the R_1 and R_2 resistor values:

$$VOUT = 0.8V \bullet \left(1 + \frac{R_1}{R_2}\right) \quad \text{(EQ. 1)}$$

When designing a PCB, include a GND guard band around the FB resistor network to reduce noise and improve accuracy and stability. Resistors R_1 and R_2 should be positioned close to the FB pin. The suggested value of the R_1 resistor is 187k.

Feed-Forward Capacitor Selection

A small capacitor (C_4 in Figure 17) in parallel with resistor R_1 is required to provide the specified load and line regulation. The suggested value of this capacitor is 22pF for R_1 = 187k. An NPO type capacitor is recommended.

Non-Adjustable Version FB Pin Connection

The fixed output versions of the ISL9120 do not require external resistors or a capacitor on the FB pin. Simply connect VOUT to FB, as shown in Figure 18.

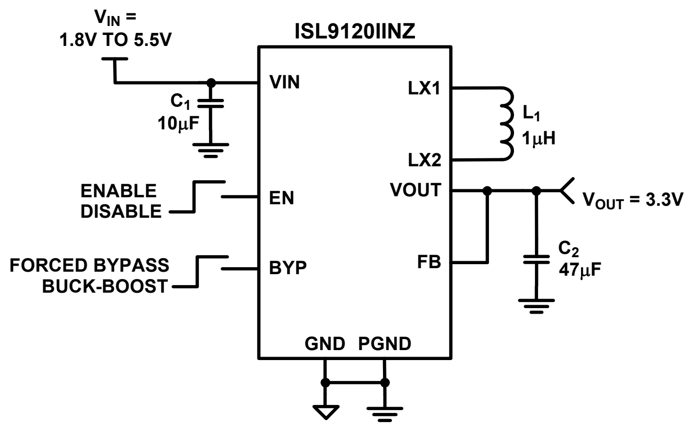


FIGURE 18. TYPICAL ISL9120IINZ APPLICATION

Inductor Selection

An inductor with high frequency core material (for example, ferrite core) should be used to minimize core losses and provide good efficiency. The inductor must be able to handle the peak switching currents without saturating.

A 1µH inductor with ≥2A saturation current rating is recommended. Select an inductor with low DCR to provide good efficiency. In applications where radiated noise must be minimized, a toroidal or shielded inductor can be used.

TABLE 1. INDUCTOR VENDOR INFORMATION

MANUFACTURER	SERIES	DIMENSION (mm)	DCR (mΩ) TYP	I_{SAT} (A) TYP
Toko	DFE201610R-H-1R0M	2.0x1.6x1.0	66	2.7
Cyntec	PIFE20161T-1R0MS	2.0x1.6x1.0	65	2.8
TDK	TFM201610GHM-1R0MTAA	2.0x1.6x1.0	50	3.8

Capacitor Selection

The input and output capacitors should be ceramic X5R type with low ESL and ESR. The recommended input capacitor value is 10µF. The recommended 10µF input capacitor should have the following minimum characteristics: 0603 case size, X5R temperature range, and 10V voltage rating. The recommended V_{OUT} capacitor values are 22µF or 47µF. The recommended 47µF output capacitor should have the following minimum characteristics: 0603 case size, X5R temperature range, and 6.3V voltage rating. The recommended 22µF output capacitor should have the following minimum characteristics: 0603 case size, X5R temperature range, and 10V voltage rating.

TABLE 2. CAPACITOR VENDOR INFORMATION

MANUFACTURER	SERIES	WEBSITE
AVX	X5R	www.avx.com
Murata	X5R	www.murata.com
TDK	X5R	www.tdk.com

Recommended PCB Layout

Correct PCB layout is critical for proper operation of the ISL9120. The input and output capacitors should be positioned as closely to the IC as possible. The ground connections of the input and output capacitors should be kept as short as possible and should be on the component layer to avoid problems that are caused by high switching currents flowing through PCB vias.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please visit our website to make sure you have the latest revision.

DATE	REVISION	CHANGE
May 23, 2017	FN8659.2	In the “Absolute Maximum Ratings” table, corrected the voltage rating as follows: - FB (Adjustable Version) -0.3V to 2.7V - FB (Fixed VOUT Version) -0.3V to 6.5V Reordered pin descriptions in the “Pin Descriptions” table. Added ISL9120IINZ-T7A and ISL9120IIAZ-T7A to the “Ordering Information” table. Applied new header/footer template.
January 29, 2016	FN8659.1	Page 1 - In “Description”, 3rd paragraph changed the value from 1µA to 3.5µA. Ordering information table Page 3, added column for Tape and Reel quantity. Page 4 - Analog Specifications: Under Power Supply - VIN Undervoltage Lockout Threshold, changed Max value from 1.775 to 1.790 VIN Supply Current, Bypass Mode changed Typ from 0.035 to 0.8 and Max from 1 to 3.5. Under Output Voltage Regulation - Output Voltage Accuracy, changed Min/Max from -2 and +2 to -3 and +4.
May 28, 2015	FN8659.0	Initial Release

About Intersil

Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing, and high-end consumer markets.

For the most updated datasheet, application notes, related documentation, and related parts, see the respective product information page found at www.intersil.com.

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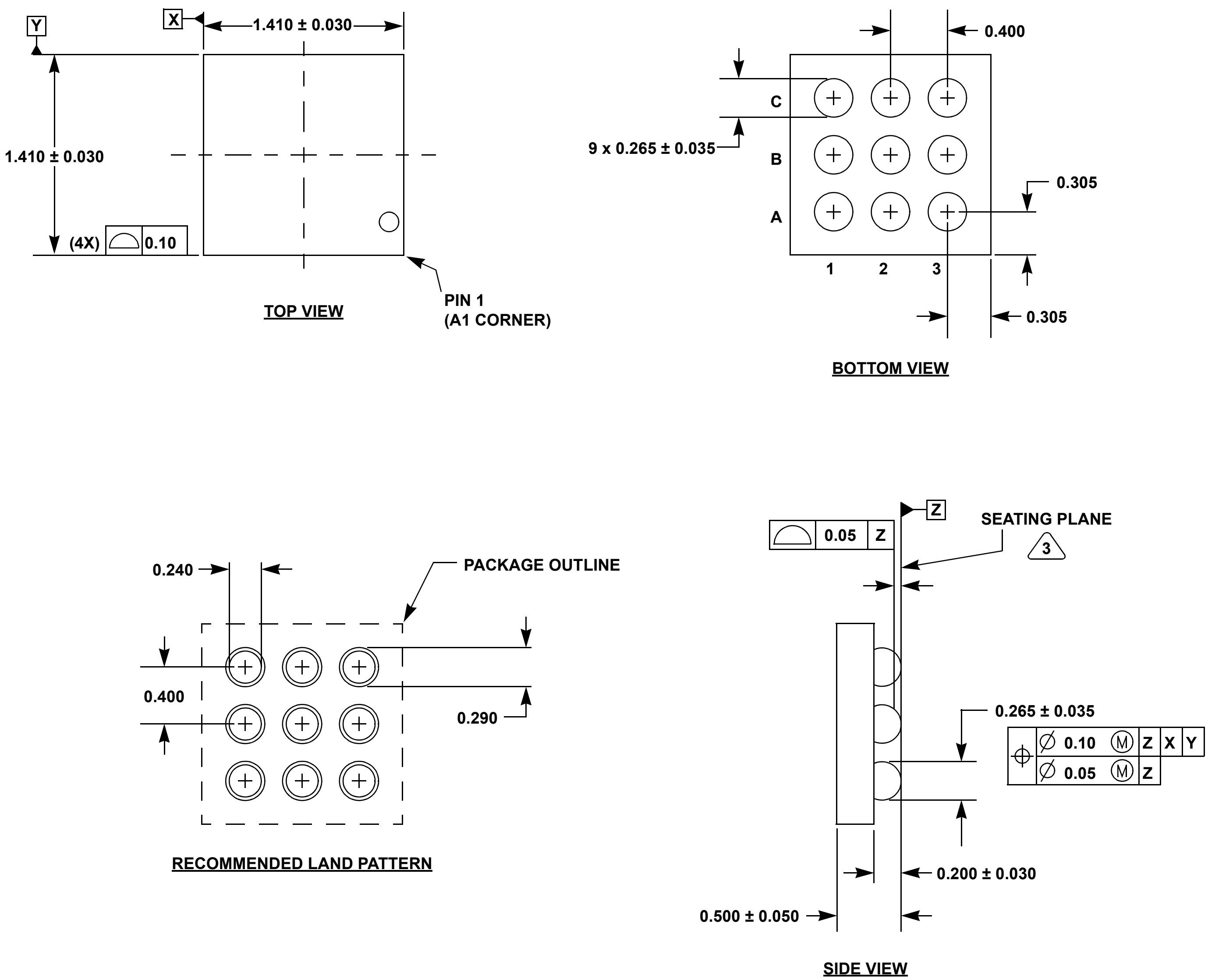
Package Outline Drawing

For the most recent package outline drawing, see W3x3.9E.

W3x3.9E

3x3 ARRAY 9 BALLS WITH 0.40 PITCH WAFER LEVEL CHIP SCALE PACKAGE

Rev 0, 8/14



NOTES:

1. All dimensions are in millimeters.
2. Dimensions and tolerance per ASMEY 14.5 - 1994, and JESD 95-1 SPP-010.
3. NSMD refers to non-solder mask defined pad design per Intersil Techbrief TB451.