



Thyristor/Diode and Thyristor/Thyristor, 135 A to 160 A (INT-A-PAK Power Modules)



INT-A-PAK

PRIMARY CHARACTERISTICS

$I_{T(AV)}$	135 A to 160 A
Type	Modules - thyristor, standard
Package	INT-A-PAK

FEATURES

- High voltage
- Electrically isolated by DBC ceramic (Al_2O_3)
- 3500 V_{RMS} isolating voltage
- Industrial standard package
- High surge capability
- Glass passivated chips
- Modules uses high voltage power thyristor/diodes in three basic configurations
- Simple mounting
- UL approved file E78996 
- Designed and qualified for multiple level
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912


RoHS
COMPLIANT

APPLICATIONS

- DC motor control and drives
- Battery charges
- Welders
- Power converters
- Lighting control
- Heat and temperature control

MAJOR RATINGS AND CHARACTERISTICS

SYMBOL	CHARACTERISTICS	VSK.136..	VSK.142..	VSK.162..	UNITS
$I_{T(AV)}$	85 °C	135	140	160	A
$I_{T(RMS)}$		300	310	355	A
I_{TSM}	50 Hz	3200	4500	4870	
	60 Hz	3360	4712	5100	
I^2t	50 Hz	51.5	102	119	kA^2s
	60 Hz	47	92.5	108	
$I^2\sqrt{t}$		515.5	1013	1190	$kA^2\sqrt{s}$
V_{RRM}	Range	400 to 1600	400 to 1600	400 to 1600	V
T_J	Range	-40 to +125			°C

ELECTRICAL SPECIFICATIONS

VOLTAGE RATINGS

TYPE NUMBER	VOLTAGE CODE	V_{RRM}/V_{DRM} , MAXIMUM REPETITIVE PEAK REVERSE VOLTAGE V	V_{RSM}/V_{DSM} , MAXIMUM NON-REPETITIVE PEAK REVERSE VOLTAGE V	I_{RRM}/I_{DRM} AT 125 °C mA
VS-VSK.136 VS-VSK.142 VS-VSK.162	04	400	500	50
	08	800	900	
	12	1200	1300	
	14	1400	1500	
	16	1600	1700	



ON-STATE CONDUCTION								
PARAMETER	SYMBOL	TEST CONDITIONS			VSK.136	VSK.142	VSK.162	UNITS
Maximum average on-state current at case temperature	I _{T(AV)}	180° conduction, half sine wave			135	140	160	A
					85	85	85	°C
Maximum RMS on-state current	I _{T(RMS)}	As AC switch			300	310	355	A
Maximum peak, one-cycle on-state, non-repetitive surge current	I _{TSM}	t = 10 ms	No voltage reapplied	Sine half wave, initial T _J = T _J maximum	3200	4500	4870	
		t = 8.3 ms			3360	4712	5100	
		t = 10 ms	100 % V _{RRM} reapplied		2700	3785	4100	
		t = 8.3 ms			2800	3963	4300	
Maximum I ² t for fusing	I ² t	t = 10 ms	No voltage reapplied		51.5	102	119	kA ² s
		t = 8.3 ms			47	92.5	108	
		t = 10 ms	100 % V _{RRM} reapplied		36.5	71.6	84	
		t = 8.3 ms			33.3	65.4	76.7	
Maximum I ² √t for fusing	I ² √t	t = 0.1 ms to 10 ms, no voltage reapplied			515.5	1013	1190	kA ² √s
Low level value of threshold voltage	V _{T(TO)1}	(16.7 % × π × I _{T(AV)}) < I < π × I _{T(AV)} , T _J maximum			0.86	0.83	0.8	V
High level value of threshold voltage	V _{T(TO)2}	(I > π × I _{T(AV)}), T _J maximum			1.05	1	0.98	
Low level value on-state slope resistance	r _{t1}	(16.7 % × π × I _{T(AV)}) < I < π × I _{T(AV)} , T _J maximum			2.02	1.78	1.67	mΩ
High level value on-state slope resistance	r _{t2}	(I > π × I _{T(AV)}), T _J maximum			1.65	1.43	1.38	
Maximum on-state voltage drop	V _{TM}	I _{TM} = π × I _{T(AV)} , T _J = 25 °C, 180° conduction			1.57	1.55	1.54	V
Maximum forward voltage drop	V _{FM}	I _{TM} = π × I _{T(AV)} , T _J = 25 °C, 180° conduction			1.57	1.55	1.54	V
Maximum holding current	I _H	Anode supply = 6 V initial I _T = 30 A, T _J = 25 °C			200			mA
Maximum latching current	I _L	Anode supply = 6 V resistive load = 1 Ω Gate pulse: 10 V, 100 μs, T _J = 25 °C			400			

SWITCHING					
PARAMETER	SYMBOL	TEST CONDITIONS		VALUES	UNITS
Typical delay time	t_{gd}	$T_J = 25\text{ }^{\circ}\text{C}$	Gate current = 1 A, $di_g/dt = 1\text{ A}/\mu\text{s}$ $V_d = 0.67\text{ \% }V_{\text{DRM}}$	1	μs
Typical rise time	t_{gr}			2	
Typical turn-off time	t_q	$I_{\text{TM}} = 300\text{ A}$, $-di/dt = 15\text{ A}/\mu\text{s}$; $T_J = T_J$ maximum $V_R = 50\text{ V}$; $dV/dt = 20\text{ V}/\mu\text{s}$; gate 0 V, 100 Ω		50 to 200	

BLOCKING				
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum peak reverse and off-state leakage current	I_{RRM} , I_{DRM}	$T_J = 125\text{ }^{\circ}\text{C}$	50	mA
RMS insulation voltage	V_{INS}	50 Hz, circuit to base, all terminals shorted, $t = 1\text{ s}$	3500	V
Critical rate of rise of off-state voltage	dV/dt	$T_J = T_J$ maximum, exponential to 67 % rated V_{DRM}	1000	V/ μ s



TRIGGERING						
PARAMETER	SYMBOL	TEST CONDITIONS		VALUES	UNITS	
Maximum peak gate power	P _{GM}	t _p ≤ 5 ms, T _J = T _J maximum		12	W	
Maximum average gate power	P _{G(AV)}	f = 50 Hz, T _J = T _J maximum		3		
Maximum peak gate current	I _{GM}	t _p ≤ 5 ms, T _J = T _J maximum		3	A	
Maximum peak negative gate voltage	- V _{GT}			10	V	
Maximum required DC gate voltage to trigger	V _{GT}	T _J = - 40 °C	Anode supply = 6 V, resistive load; R _a = 1 Ω	4		
		T _J = 25 °C		2.5		
		T _J = T _J maximum		1.7		
Maximum required DC gate current to trigger	I _{GT}	T _J = - 40 °C		270	mA	
		T _J = 25 °C		150		
		T _J = T _J maximum		80		
Maximum gate voltage that will not trigger	V _{GD}	T _J = T _J maximum, rated V _{DRM} applied		0.3	V	
Maximum gate current that will not trigger	I _{GD}			10	mA	
Maximum rate of rise of turned-on current	di/dt	T _J = T _J maximum, I _{TM} = 400 A rated V _{DRM} applied		300	A/μs	

THERMAL AND MECHANICAL SPECIFICATIONS						
PARAMETER	SYMBOL	TEST CONDITIONS	VSK.136	VSK.142	VSK.162	UNITS
Maximum junction operating temperature range	T _J		-40 to +125			°C
Maximum storage temperature range	T _{Stg}		-40 to +150			
Maximum thermal resistance, junction to case per junction	R _{thJC}	DC operation	0.18	0.18	0.16	K/W
Maximum thermal resistance, case to heatsink per module	R _{thCS}	Mounting surface, smooth, flat and greased	0.05			
Mounting torque ± 10 %	IAP to heatsink busbar to IAP	A mounting compound is recommended and the torque should be rechecked after a period of 3 hours to allow for the spread of the compound. Lubricated threads.	4 to 6			Nm
Approximate weight			200			g
			7.1			oz.
Case style			INT-A-PAK			

ΔR CONDUCTION PER JUNCTION											
DEVICES	SINUSOIDAL CONDUCTION AT T _J MAXIMUM					RECTANGULAR CONDUCTION AT T _J MAXIMUM					UNITS
	180°	120°	90°	60°	30°	180°	120°	90°	60°	30°	
VSK.136	0.007	0.01	0.013	0.0155	0.017	0.009	0.012	0.014	0.015	0.017	K/W
VSK.142	0.0019	0.0019	0.0020	0.0020	0.0021	0.0018	0.0022	0.0023	0.0023	0.0020	
VSK.162	0.0030	0.0031	0.0032	0.0033	0.0034	0.0029	0.0036	0.0039	0.0041	0.0040	

Note

- Table shows the increment of thermal resistance R_{thJC} when devices operate at different conduction angles than DC

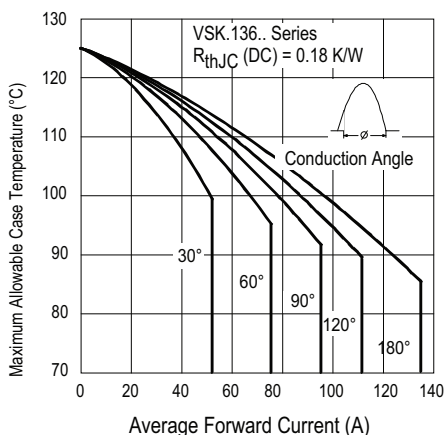


Fig. 1 - Current Ratings Characteristics

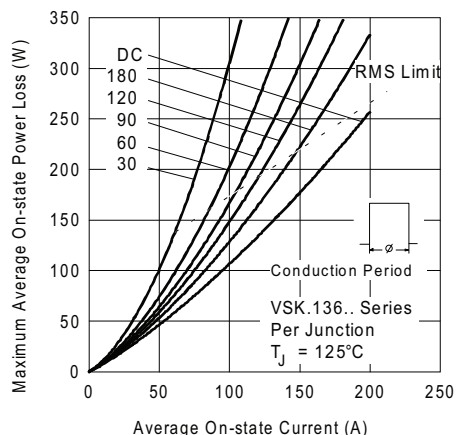


Fig. 4 - On-State Power Loss Characteristics

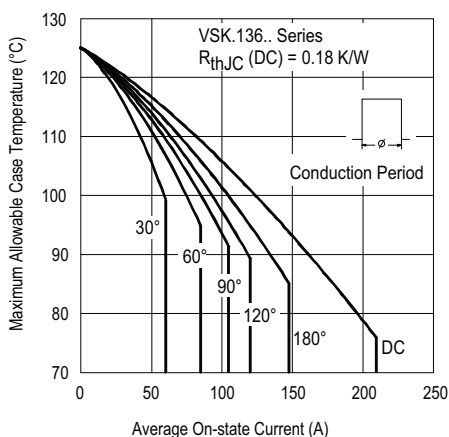


Fig. 2 - Current Ratings Characteristics

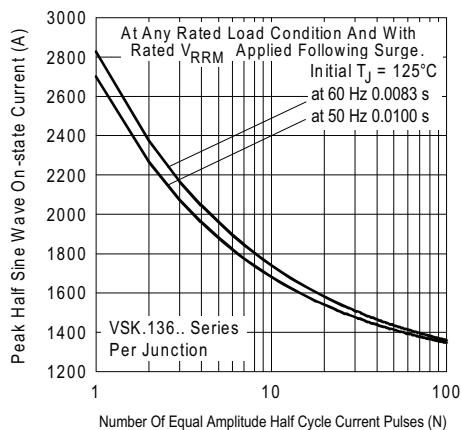


Fig. 5 - Maximum Non-Repetitive Surge Current

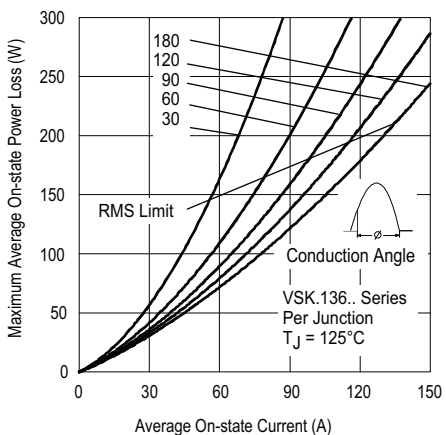


Fig. 3 - On-State Power Loss Characteristics

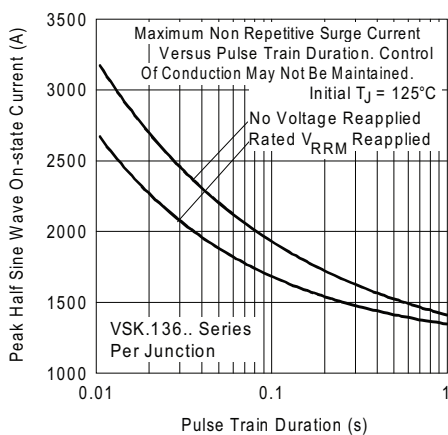


Fig. 6 - Maximum Non-Repetitive Surge Current

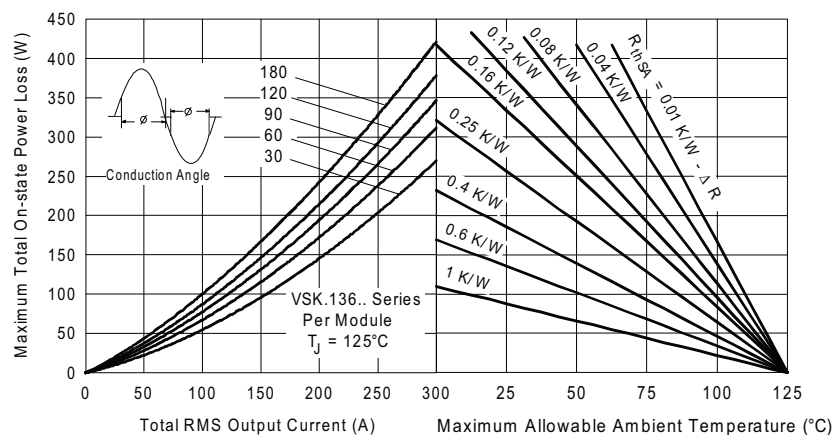


Fig. 7 - On-State Power Loss Characteristics

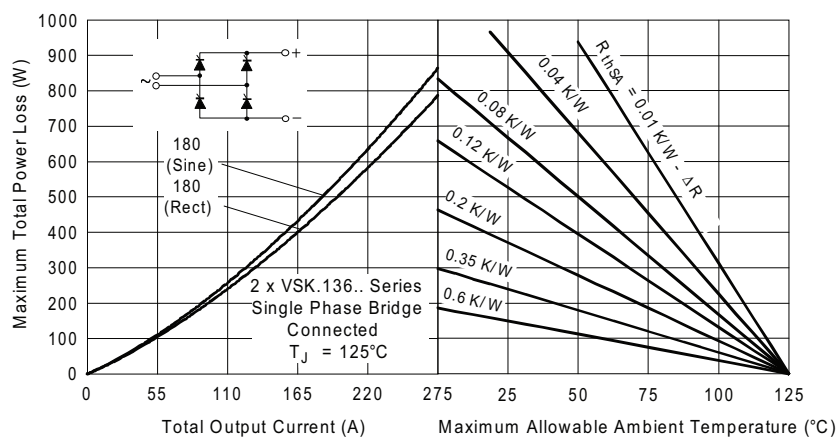


Fig. 8 - On-State Power Loss Characteristics

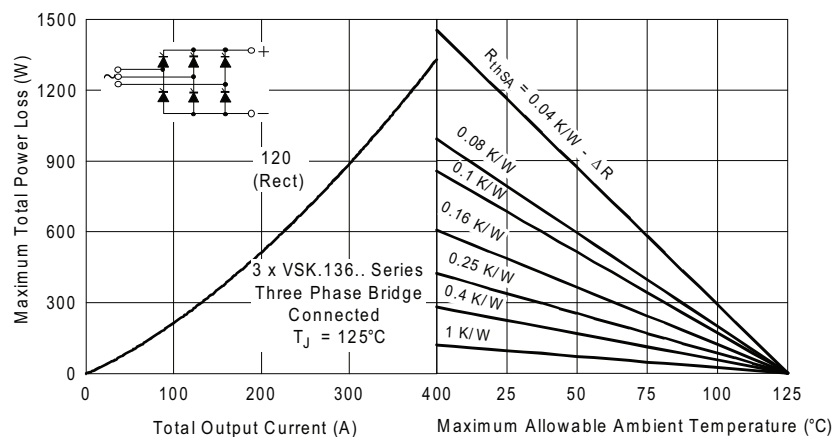


Fig. 9 - On-State Power Loss Characteristics

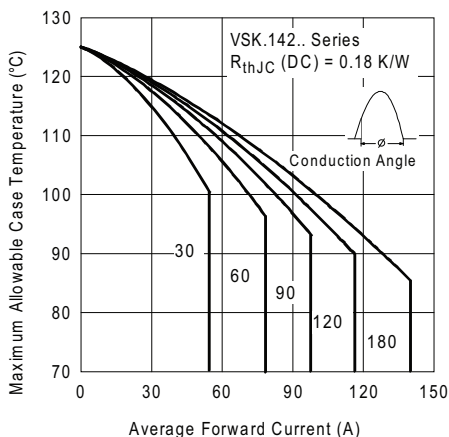


Fig. 10 - Current Ratings Characteristics

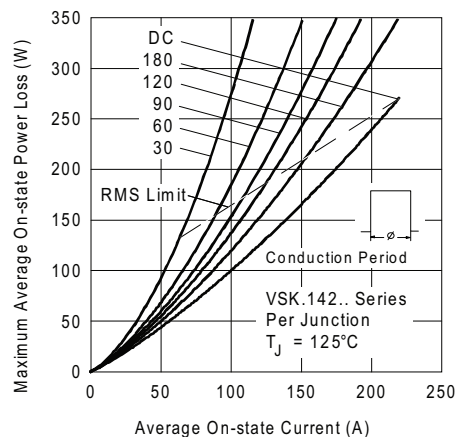


Fig. 13 - On-State Power Loss Characteristics

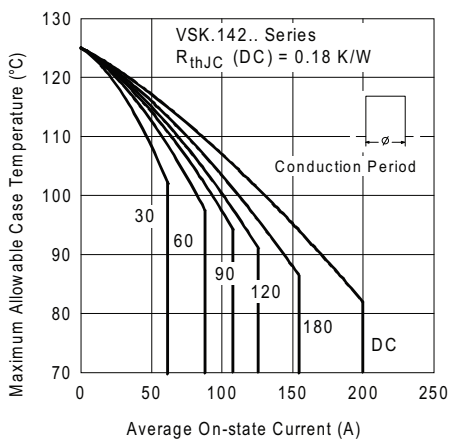


Fig. 11 - Current Ratings Characteristics

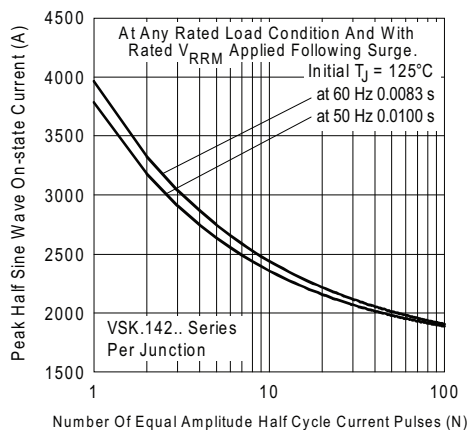


Fig. 14 - Maximum Non-Repetitive Surge Current

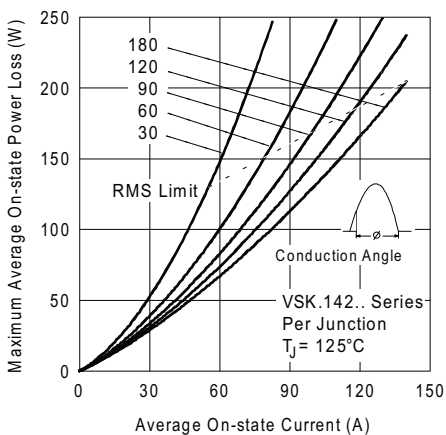


Fig. 12 - On-State Power Loss Characteristics

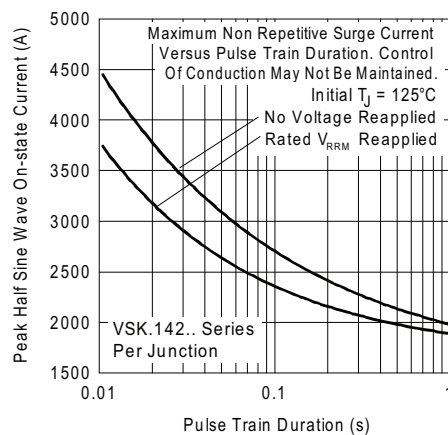


Fig. 15 - Maximum Non-Repetitive Surge Current

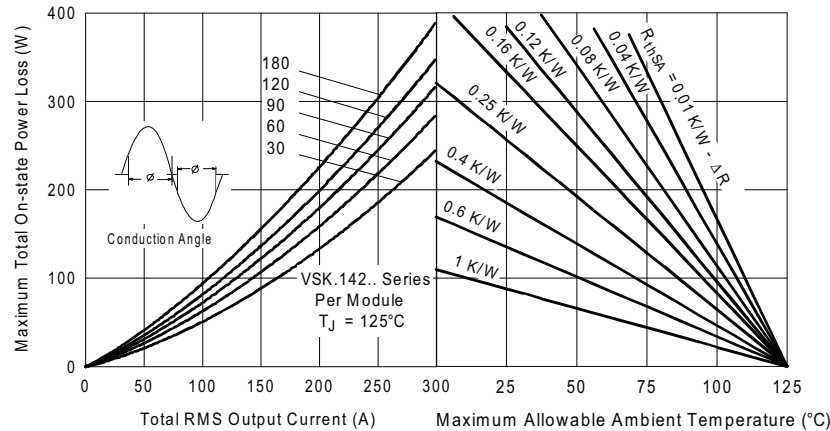


Fig. 16 - On-State Power Loss Characteristics

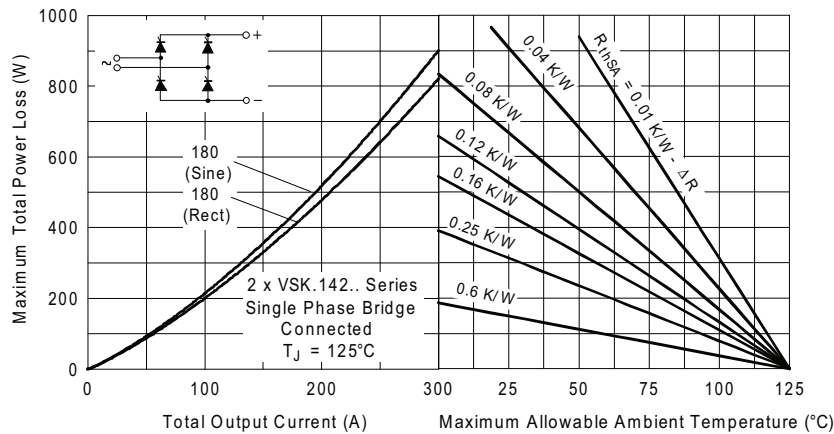


Fig. 17 - On-State Power Loss Characteristics

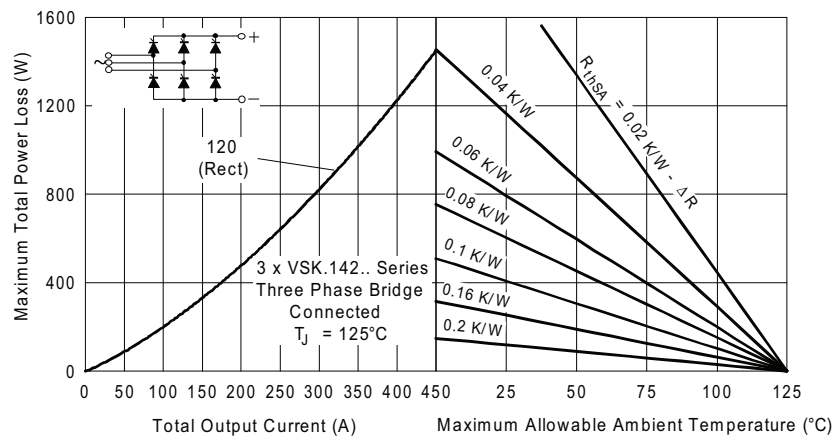


Fig. 18 - On-State Power Loss Characteristics

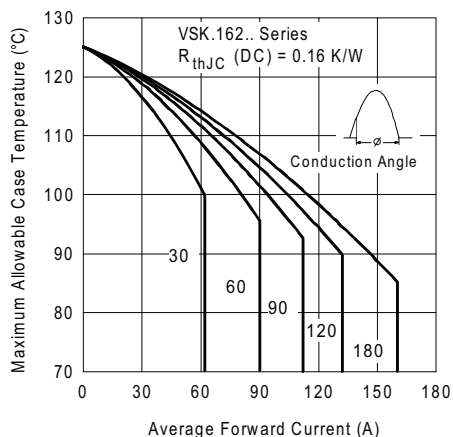


Fig. 19 - Current Ratings Characteristics

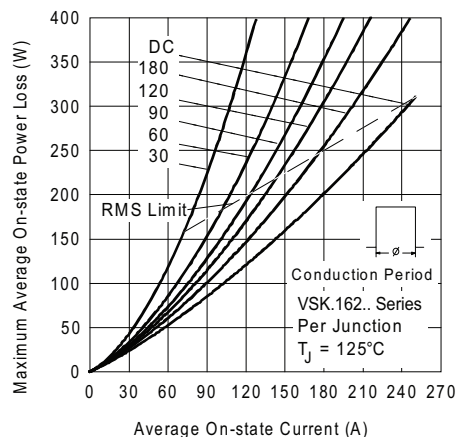


Fig. 22 - On-State Power Loss Characteristics

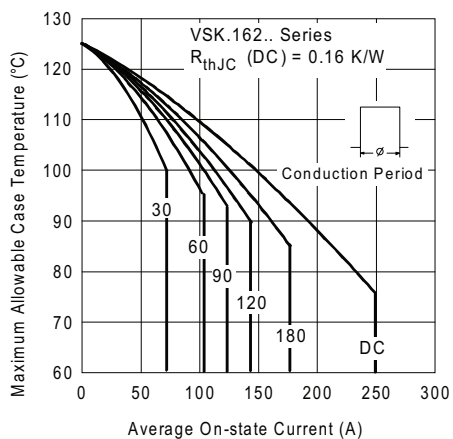


Fig. 20 - Current Ratings Characteristics

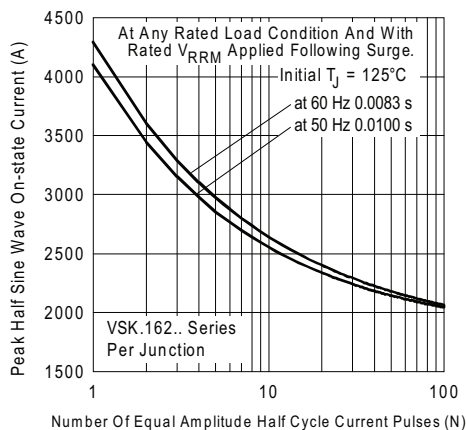


Fig. 23 - Maximum Non-Repetitive Surge Current

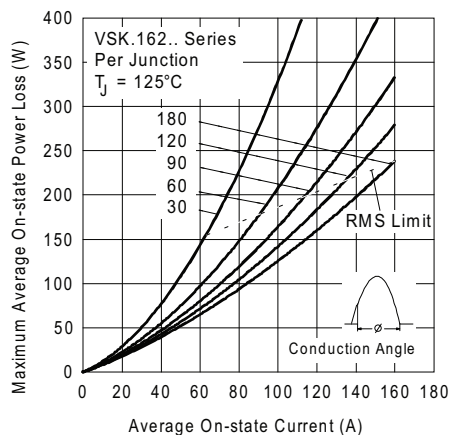


Fig. 21 - On-State Power Loss Characteristics

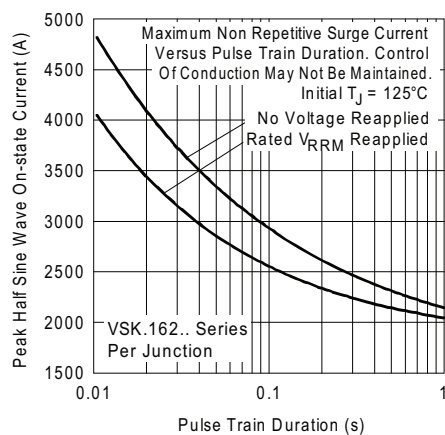


Fig. 24 - Maximum Non-Repetitive Surge Current

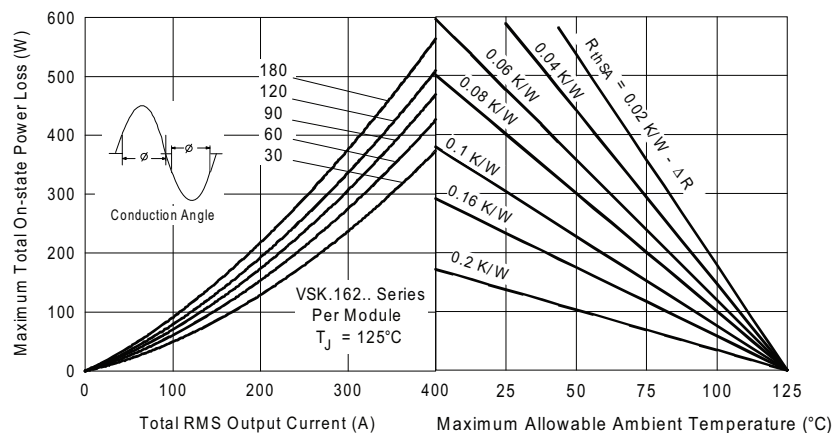


Fig. 25 - On-State Power Loss Characteristics

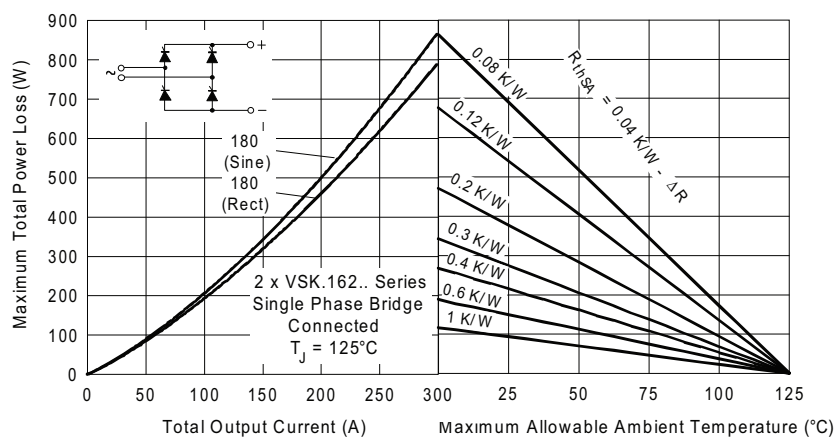


Fig. 26 - On-State Power Loss Characteristics

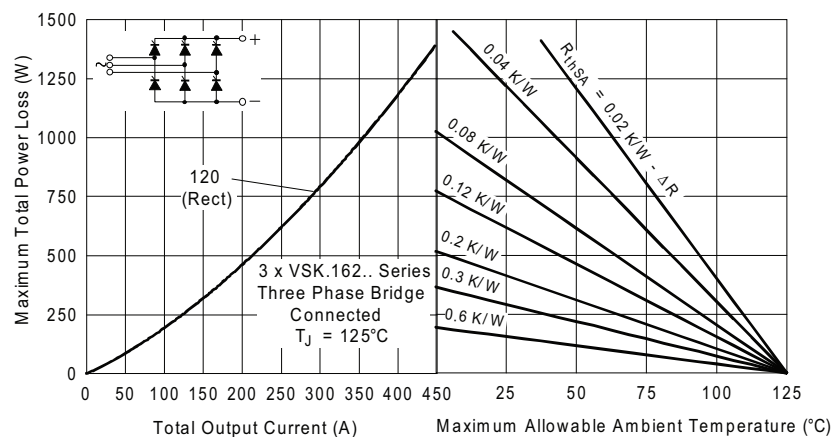


Fig. 27 - On-State Power Loss Characteristics

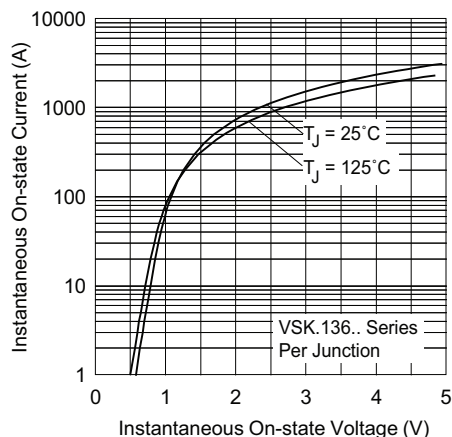


Fig. 28 - On-State Voltage Drop Characteristics

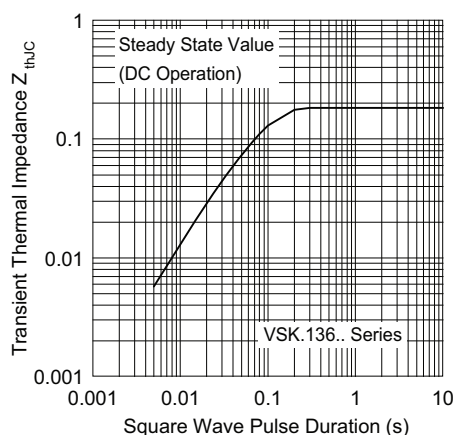


Fig. 31 - Thermal Impedance Z_{thJC} Characteristics

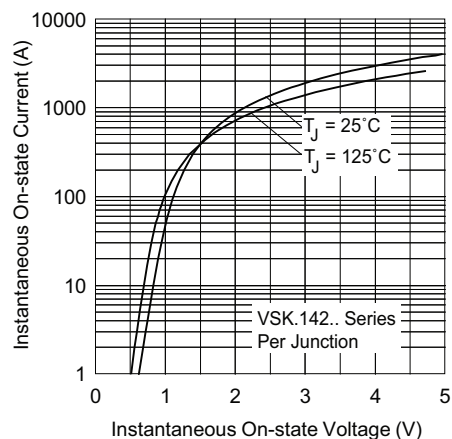


Fig. 29 - On-State Voltage Drop Characteristics

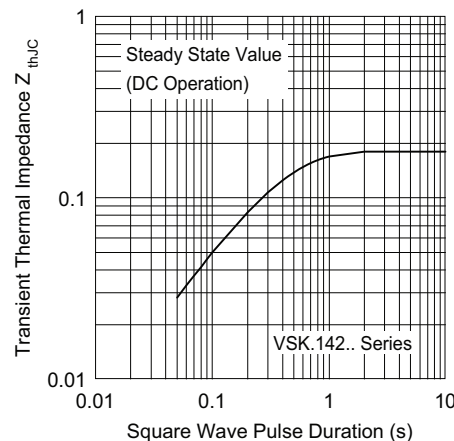


Fig. 32 - Thermal Impedance Z_{thJC} Characteristics

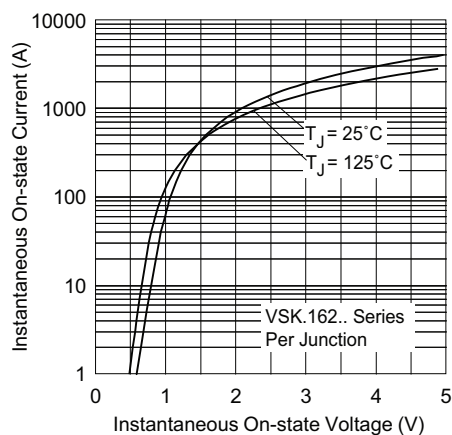


Fig. 30 - On-State Voltage Drop Characteristics

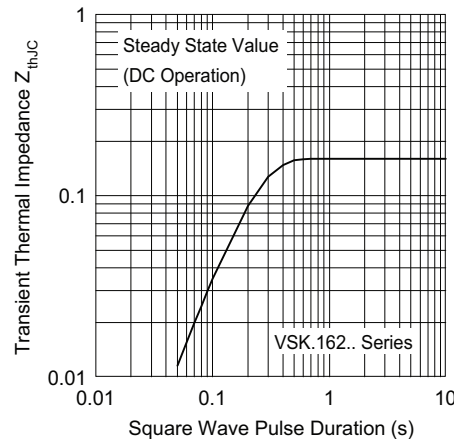
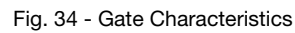


Fig. 33 - Thermal Impedance Z_{thJC} Characteristics





CIRCUIT CONFIGURATION		
CIRCUIT DESCRIPTION	CIRCUIT CONFIGURATION CODE	CIRCUIT DRAWING
Two SCRs doubler circuit	T	
SCR/diode doubler circuit, positive control	H	
SCR/diode doubler circuit, negative control	L	

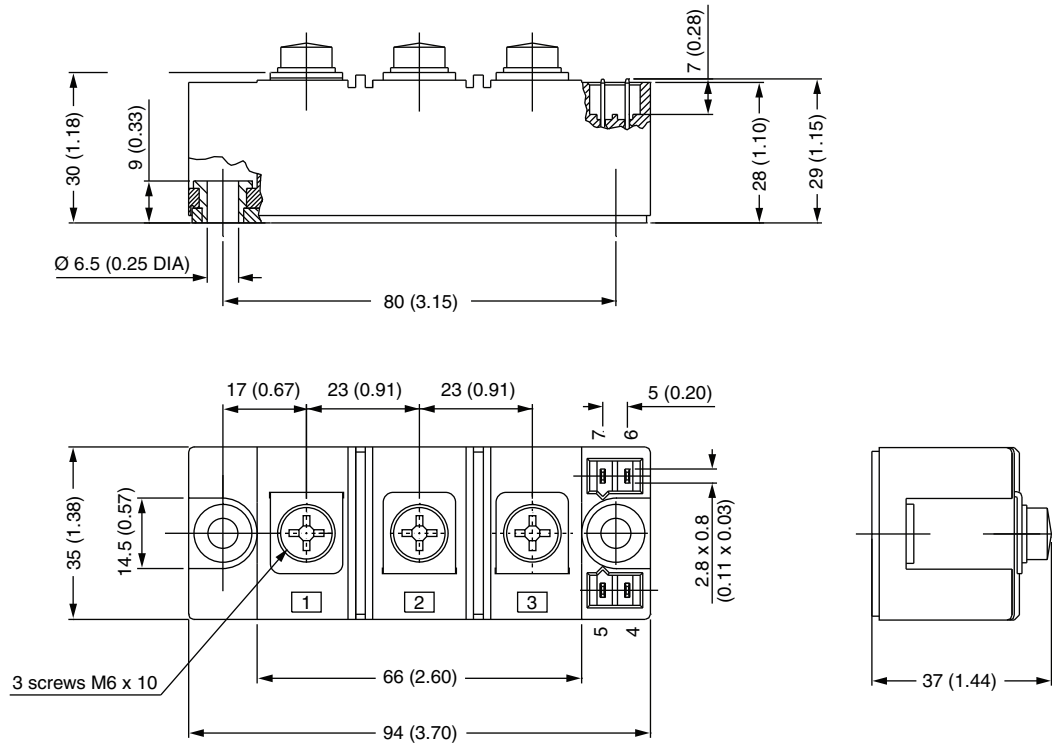
LINKS TO RELATED DOCUMENTS

Dimensions

www.vishay.com/doc?95067

INT-A-PAK IGBT/Thyristor

DIMENSIONS in millimeters (inches)





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