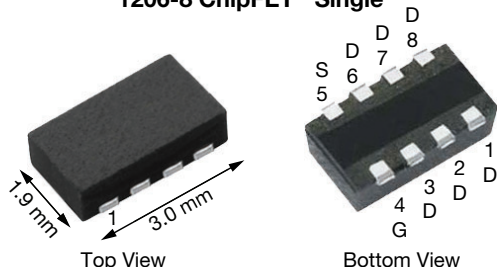


N-Channel 30 V (D-S) MOSFET

PRODUCT SUMMARY

V _{DS} (V)	R _{DS(on)} (Ω)	I _D (A) ^a	Q _g (TYP.)
30	0.019 at V _{GS} = 10 V	6	9 nC
	0.024 at V _{GS} = 4.5 V	6	

1206-8 ChipFET® Single



Marking Code: AI

Ordering Information:

Si5440DC-T1-GE3 (lead (Pb)-free and halogen-free)

FEATURES

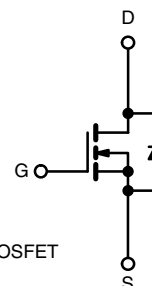
- TrenchFET® power MOSFET
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

APPLICATIONS

- Load switches
- Notebook PC



RoHS
COMPLIANT
HALOGEN
FREE



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V _{DS}	30	V
Gate-Source Voltage	V _{GS}	± 20	
Continuous Drain Current (T _J = 150 °C)	I _D	6 ^a	A
		6 ^a	
		6 ^{a, b, c}	
		6 ^{a, b, c}	
Pulsed Drain Current	I _{DM}	30	A
Continuous Source-Drain Diode Current	I _S	5.2	
		2.1 ^{b, c}	
Maximum Power Dissipation	P _D	6.3	W
		4	
		2.5 ^{b, c}	
		1.6 ^{b, c}	
Operating Junction and Storage Temperature Range	T _J , T _{stg}	-55 to +150	°C
Soldering Recommendations (Peak Temperature) ^{e, f}		260	

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	TYPICAL	MAXIMUM	UNIT
Maximum Junction-to-Ambient ^{a, c, d}	R _{thJA}	40	50	°C/W
Maximum Junction-to-Foot (Drain)	R _{thJF}	15	20	

Notes

- Package limited, T_C = 25 °C.
- Surface mounted on 1" x 1" FR4 board.
- t = 10 s
- Maximum under steady state conditions is 95 °C/W.
- The ChipFET is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.



SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA	30	-	-	V
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	I _D = 250 μA	-	31	-	mV/°C
V _{GS(th)} Temperature Coefficient	ΔV _{GS(th)} /T _J		-	-5.1	-	
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	1.2	-	2.5	V
Gate-Source Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20 V	-	-	± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 30 V, V _{GS} = 0 V	-	-	1	μA
		V _{DS} = 30 V, V _{GS} = 0 V, T _J = 55 °C	-	-	5	
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = 10 V	20	-	-	A
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = 10 V, I _D = 9.1 A	-	0.016	0.019	Ω
		V _{GS} = 4.5 V, I _D = 8.1 A	-	0.019	0.024	
Forward Transconductance ^a	g _{fs}	V _{DS} = 15 V, I _D = 9.1 A	-	30	-	S
Dynamic ^b						
Input Capacitance	C _{iss}	V _{DS} = 10 V, V _{GS} = 0 V, f = 1 MHz	-	1200	-	pF
Output Capacitance	C _{oss}		-	180	-	
Reverse Transfer Capacitance	C _{rss}		-	80	-	
Total Gate Charge	Q _g	V _{DS} = 10 V, V _{GS} = 10 V, I _D = 9.1 A	-	19	29	nC
		V _{DS} = 10 V, V _{GS} = 4.5 V, I _D = 9.1 A	-	9	14	
			Gate-Source Charge	Q _{gs}	-	
Gate-Drain Charge	Q _{gd}	-	2.3	-		
Gate Resistance	R _g	f = 1 MHz	-	3	-	Ω
Turn-On Delay Time	t _{d(on)}	V _{DD} = 15 V, R _L = 2.1 Ω I _D ≅ 7.3 A, V _{GEN} = 4.5 V, R _g = 1 Ω	-	20	30	ns
Rise Time	t _r		-	12	20	
Turn-Off Delay Time	t _{d(off)}		-	20	30	
Fall Time	t _f		-	10	15	
Turn-On Delay Time	t _{d(on)}	V _{DD} = 15 V, R _L = 2.1 Ω I _D ≅ 7.3 A, V _{GEN} = 10 V, R _g = 1 Ω	-	10	15	
Rise Time	t _r		-	10	15	
Turn-Off Delay Time	t _{d(off)}		-	20	30	
Fall Time	t _f		-	10	15	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C	-	-	5.2	A
Pulse Diode Forward Current	I _{SM}		-	-	30	
Body Diode Voltage	V _{SD}	I _S = 7.3 A, V _{GS} = 0 V	-	0.8	1.2	V
Body Diode Reverse Recovery Time	t _{rr}	I _F = 7.3 A, di/dt = 100 A/μs, T _J = 25 °C	-	20	40	ns
Body Diode Reverse Recovery Charge	Q _{rr}		-	10	20	nC
Reverse Recovery Fall Time	t _a		-	11	-	ns
Reverse Recovery Rise Time	t _b		-	9	-	

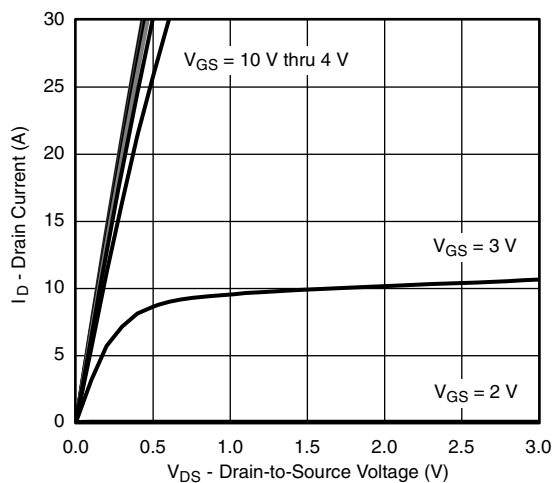
Notes

- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
b. Guaranteed by design, not subject to production testing.

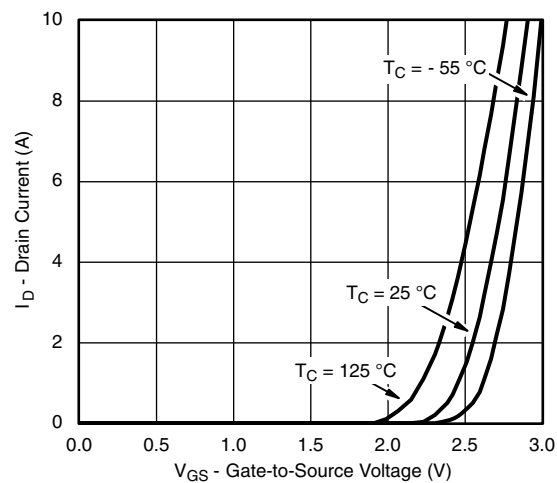
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



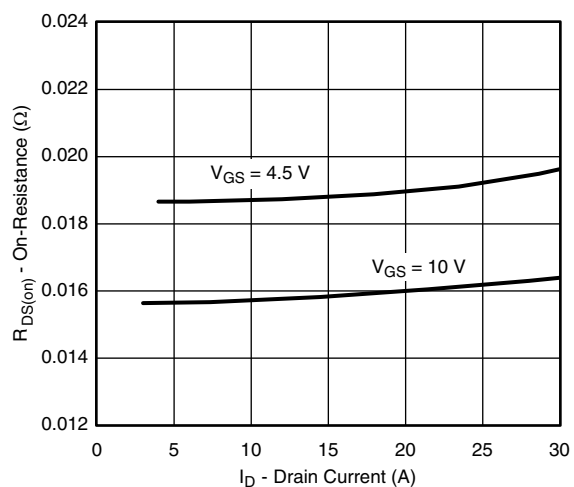
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



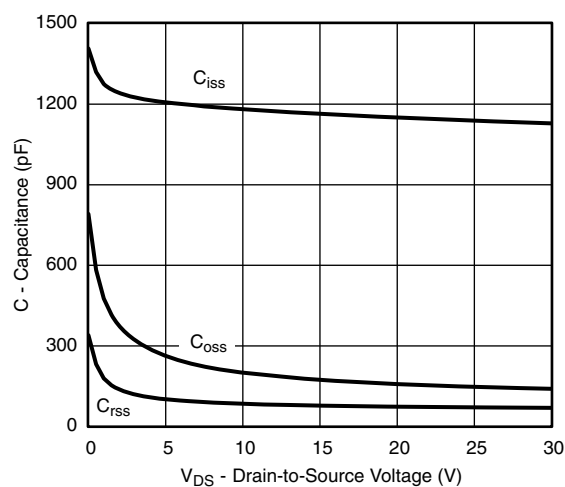
Output Characteristics



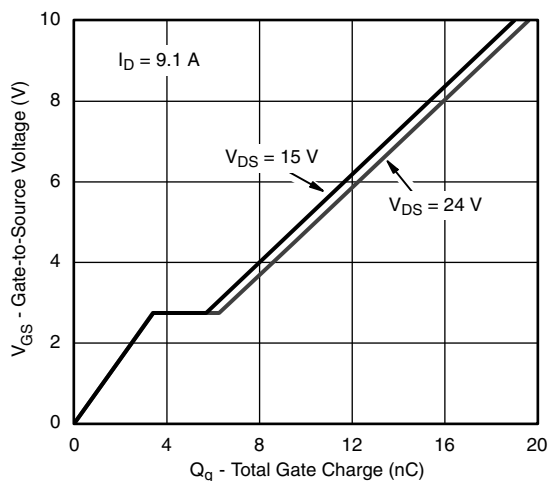
Transfer Characteristics



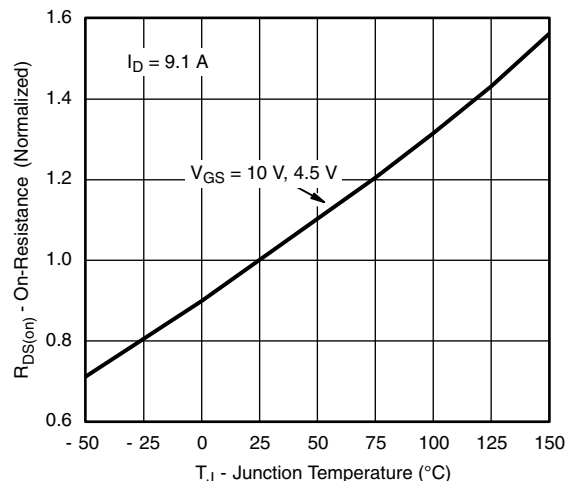
On-Resistance vs. Drain Current



Capacitance



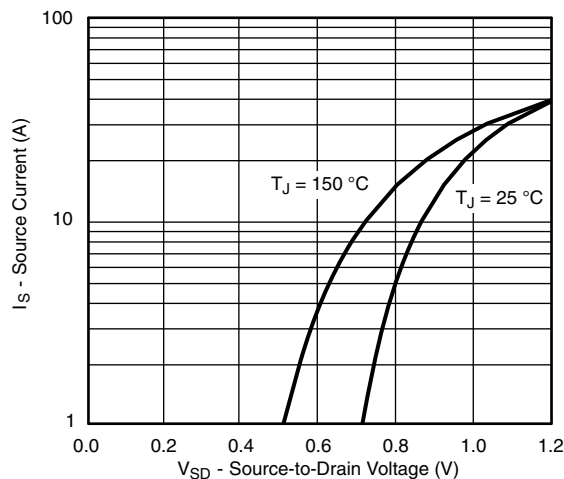
Gate Charge



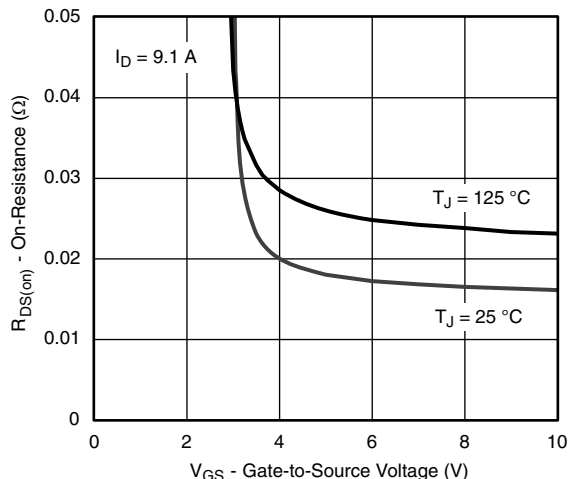
On-Resistance vs. Junction Temperature



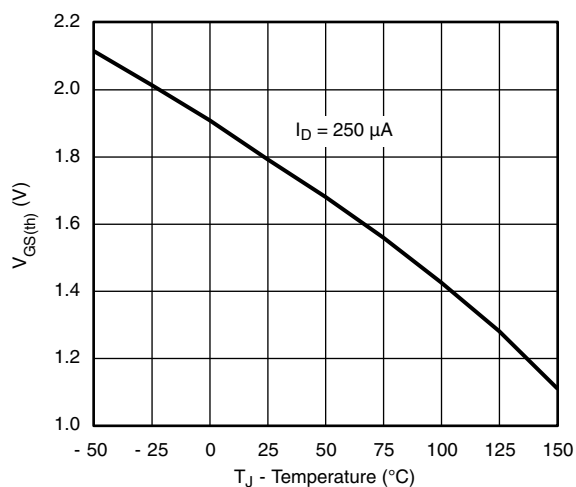
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



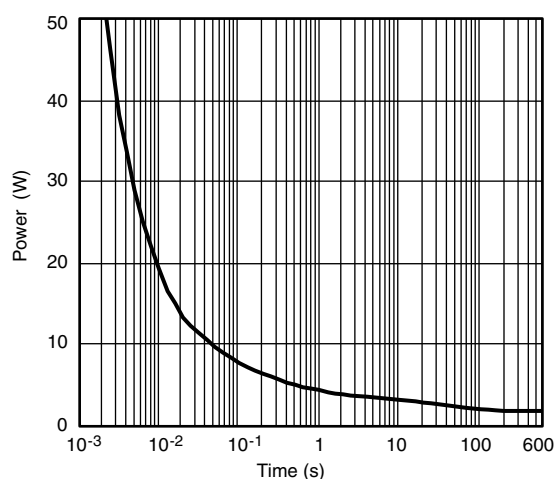
Source-Drain Diode Forward Voltage



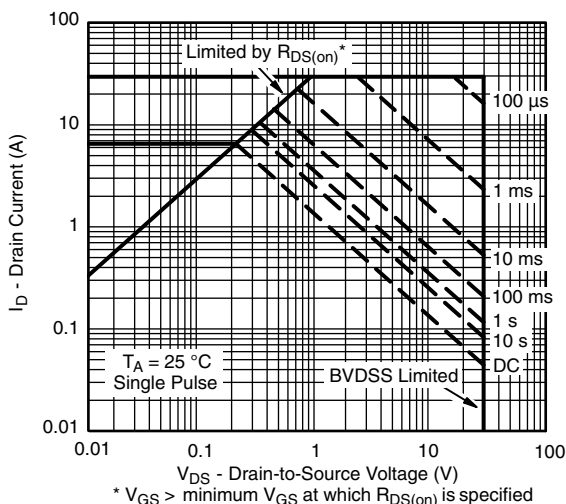
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



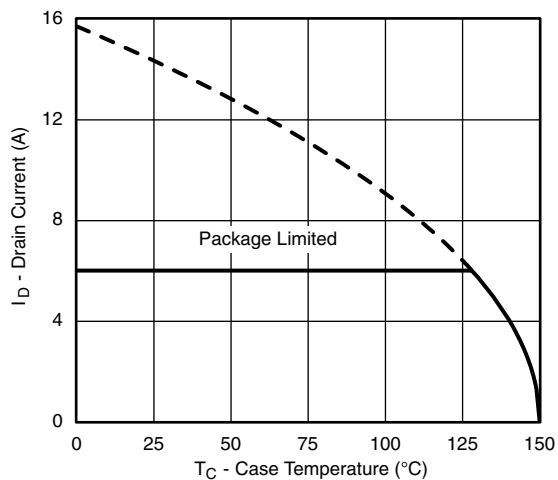
Single Pulse Power



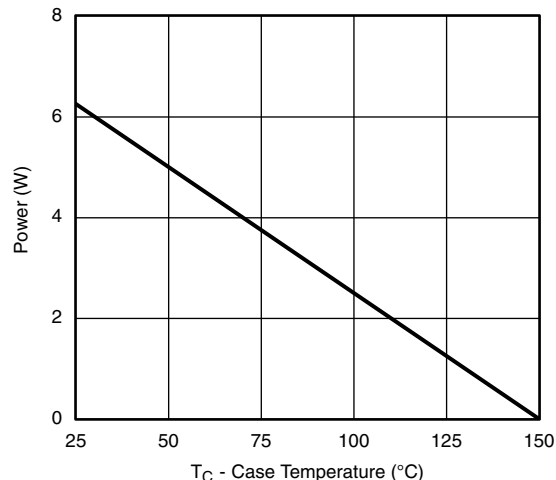
Safe Operating Area, Junction-to-Ambient



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Current Derating ^a



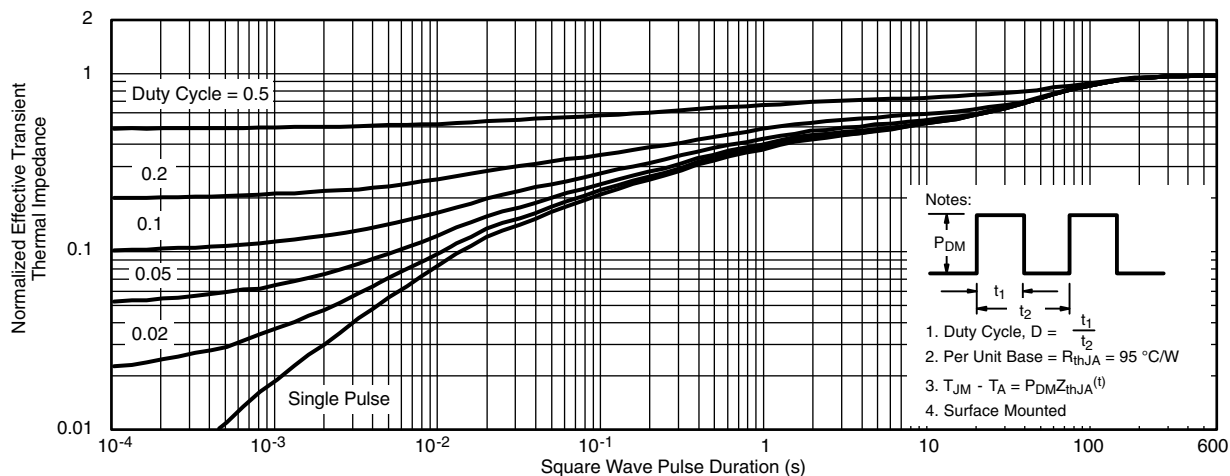
Power Derating

Note

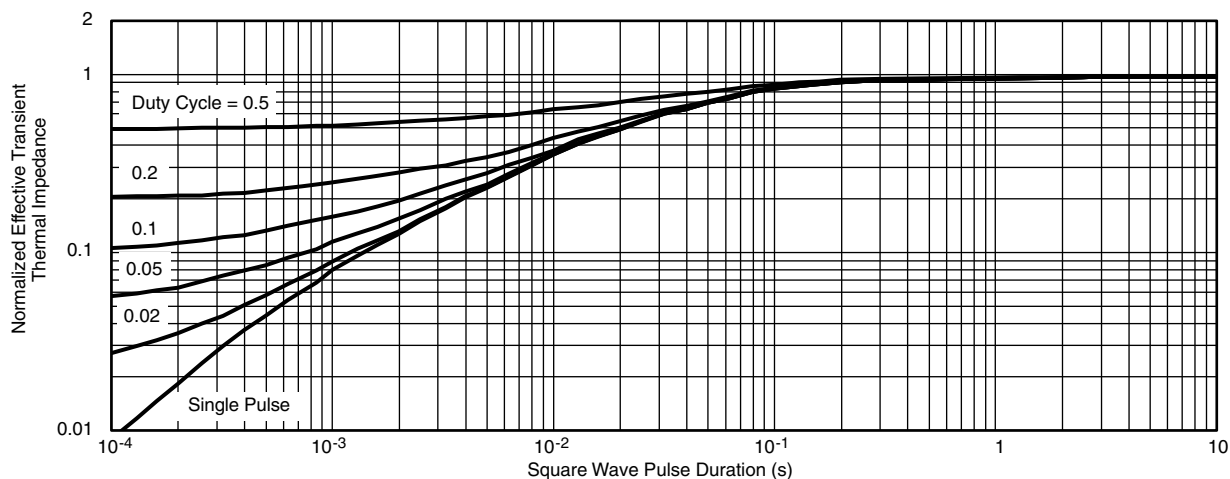
- a. The power dissipation P_D is based on T_J (max.) = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient

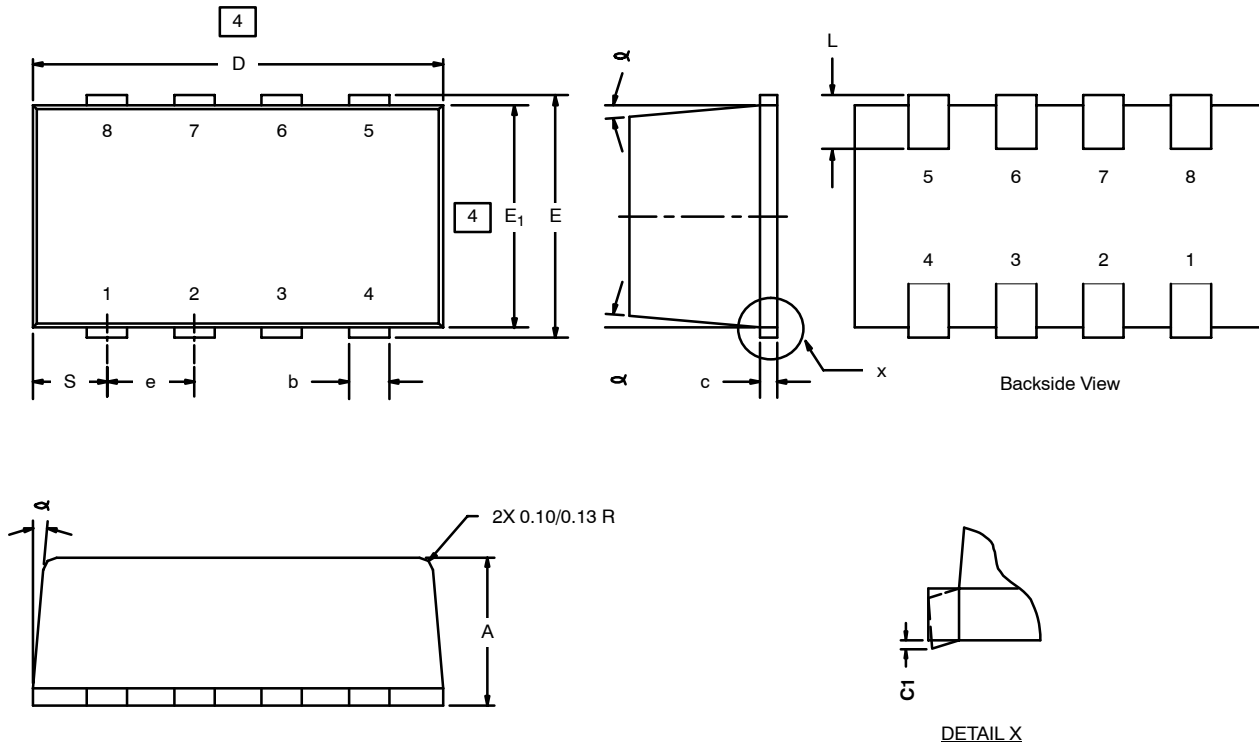


Normalized Thermal Transient Impedance, Junction-to-Foot

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?69056.



1206-8 ChipFET®



NOTES:

1. All dimensions are in millimeters.
2. Mold gate burrs shall not exceed 0.13 mm per side.
3. Leadframe to molded body offset is horizontal and vertical shall not exceed 0.08 mm.
4. Dimensions exclusive of mold gate burrs.
5. No mold flash allowed on the top and bottom lead surface.

Dim	MILLIMETERS			INCHES		
	Min	Nom	Max	Min	Nom	Max
A	1.00	–	1.10	0.039	–	0.043
b	0.25	0.30	0.35	0.010	0.012	0.014
c	0.1	0.15	0.20	0.004	0.006	0.008
c1	0	–	0.038	0	–	0.0015
D	2.95	3.05	3.10	0.116	0.120	0.122
E	1.825	1.90	1.975	0.072	0.075	0.078
E ₁	1.55	1.65	1.70	0.061	0.065	0.067
e	0.65 BSC			0.0256 BSC		
L	0.28	–	0.42	0.011	–	0.017
S	0.55 BSC			0.022 BSC		
α	5°Nom			5°Nom		
ECN: C-03528—Rev. F, 19-Jan-04						
DWG: 5547						

Single-Channel 1206-8 ChipFET® Power MOSFET Recommended Pad Pattern and Thermal Performance

INTRODUCTION

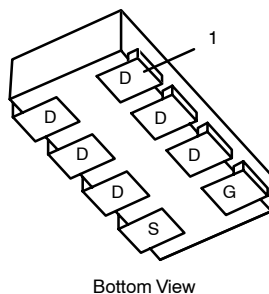
New Vishay Siliconix ChipFETs in the leadless 1206-8 package feature the same outline as popular 1206-8 resistors and capacitors but provide all the performance of true power semiconductor devices. The 1206-8 ChipFET has the same footprint as the body of the LITTLE FOOT® TSOP-6, and can be thought of as a leadless TSOP-6 for purposes of visualizing board area, but its thermal performance bears comparison with the much larger SO-8.

This technical note discusses the single-channel ChipFET 1206-8 pin-out, package outline, pad patterns, evaluation board layout, and thermal performance.

PIN-OUT

Figure 1 shows the pin-out description and Pin 1 identification for the single-channel 1206-8 ChipFET device. The pin-out is similar to the TSOP-6 configuration, with two additional drain pins to enhance power dissipation and thermal performance. The legs of the device are very short, again helping to reduce the thermal path to the external heatsink/pcb and allowing a larger die to be fitted in the device if necessary.

Single 1206-8 ChipFET



Bottom View

FIGURE 1.

For package dimensions see the 1206-8 ChipFET package outline drawing (<http://www.vishay.com/doc?71151>).

BASIC PAD PATTERNS

The basic pad layout with dimensions is shown in Application Note 826, *Recommended Minimum Pad Patterns With Outline Drawing Access for Vishay Siliconix MOSFETs*, (<http://www.vishay.com/doc?72286>). This is sufficient for low power dissipation MOSFET applications, but power semiconductor performance requires a greater copper pad area, particularly for the drain leads.

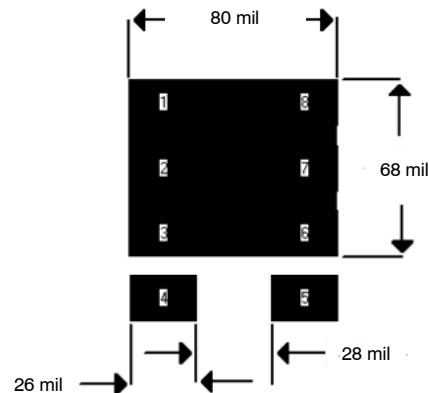


FIGURE 2. Footprint With Copper Spreading

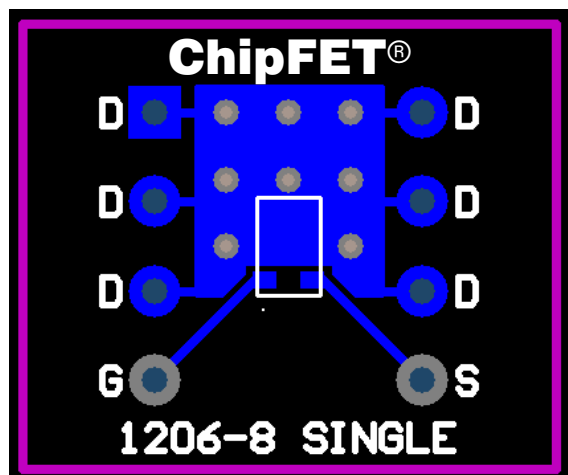
The pad pattern with copper spreading shown in Figure 2 improves the thermal area of the drain connections (pins 1,2,3,6,7,8) while remaining within the confines of the basic footprint. The drain copper area is 0.0054 sq. in. or 3.51 sq. mm). This will assist the power dissipation path away from the device (through the copper leadframe) and into the board and exterior chassis (if applicable) for the single device. The addition of a further copper area and/or the addition of vias to other board layers will enhance the performance still further. An example of this method is implemented on the Vishay Siliconix Evaluation Board described in the next section (Figure 3).

THE VISHAY SILICONIX EVALUATION BOARD FOR THE SINGLE 1206-8

The ChipFET 1206-08 evaluation board measures 0.6 in by 0.5 in. Its copper pad pattern consists of an increased pad area around the six drain leads on the top-side—approximately 0.0482 sq. in. 31.1 sq. mm—and vias added through to the underside of the board, again with a maximized copper pad area of approximately the board-size dimensions. The outer package outline is for the 8-pin DIP, which will allow test sockets to be used to assist in testing.

The thermal performance of the 1206-8 on this board has been measured with the results following on the next page. The testing included comparison with the minimum recommended footprint on the evaluation board-size pcb and the industry standard one-inch square FR4 pcb with copper on both sides of the board.

Front of Board



Back of Board

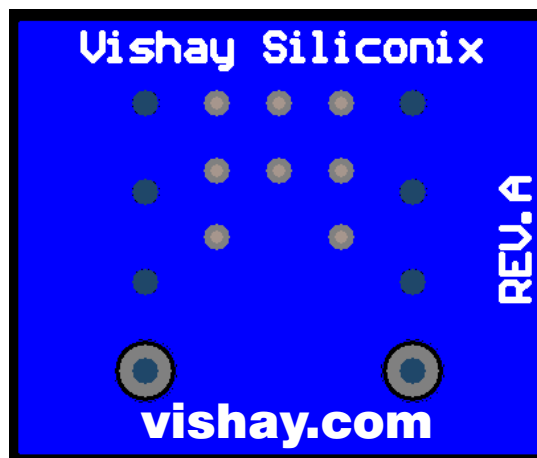


FIGURE 3.

THERMAL PERFORMANCE

Junction-to-Foot Thermal Resistance (the Package Performance)

Thermal performance for the 1206-8 ChipFET measured as junction-to-foot thermal resistance is 15°C/W typical, 20°C/W maximum for the single device. The “foot” is the drain lead of the device as it connects with the body. This is identical to the SO-8 package $R_{\theta jf}$ performance, a feat made possible by shortening the leads to the point where they become only a small part of the total footprint area.

Junction-to-Ambient Thermal Resistance (dependent on pcb size)

The typical $R_{\theta ja}$ for the single-channel 1206-8 ChipFET is 80°C/W steady state, compared with 68°C/W for the SO-8. Maximum ratings are 95°C/W for the 1206-8 versus 80°C/W for the SO-8.

Testing

To aid comparison further, Figure 4 illustrates ChipFET 1206-8 thermal performance on two different board sizes and three different pad patterns. The results display the thermal performance out to steady state and produce a graphic account of how an increased copper pad area for the drain connections can enhance thermal performance. The measured steady state values of $R_{\theta ja}$ for the single 1206-8 ChipFET are :

1) Minimum recommended pad pattern (see Figure 2) on the evaluation board size of 0.5 in x 0.6 in.	156°C/W
2) The evaluation board with the pad pattern described on Figure 3.	111°C/W
3) Industry standard 1" square pcb with maximum copper both sides.	78°C/W

The results show that a major reduction can be made in the thermal resistance by increasing the copper drain area. In this example, a 45°C/W reduction was achieved without having to increase the size of the board. If increasing board size is an option, a further 33°C/W reduction was obtained by maximizing the copper from the drain on the larger 1" square pcb.

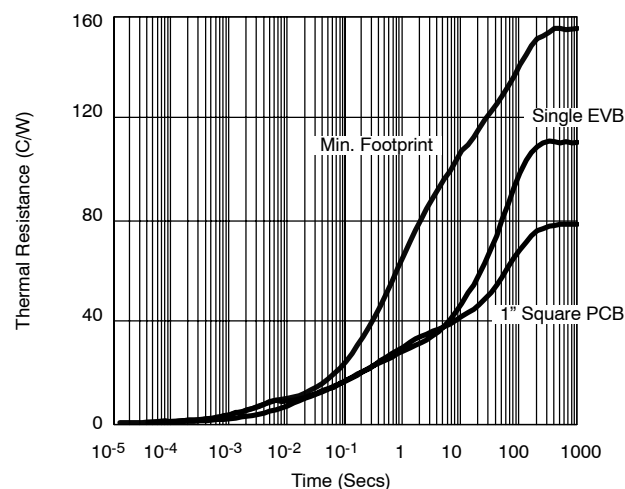


FIGURE 4. Single 1206-8 ChipFET

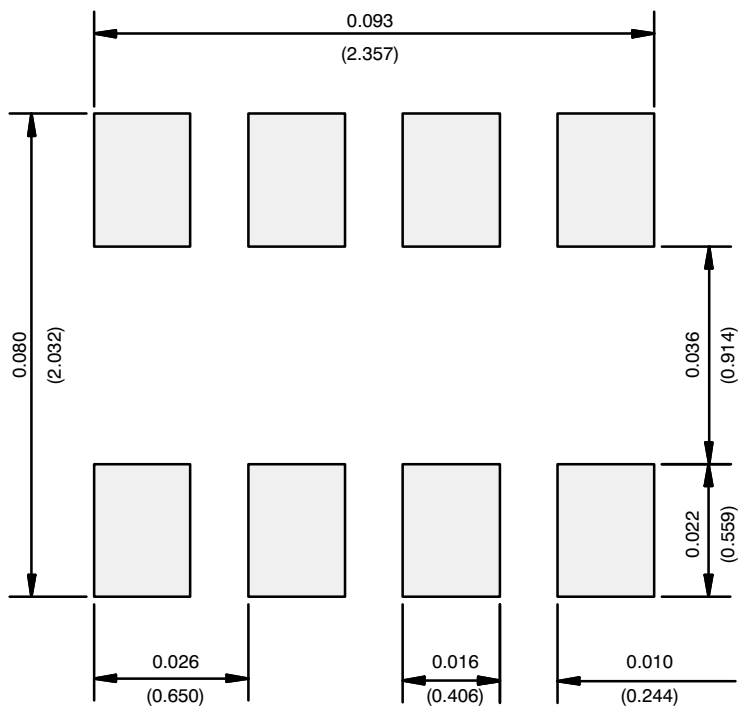
SUMMARY

The thermal results for the single-channel 1206-8 ChipFET package display similar power dissipation performance to the SO-8 with a footprint reduction of 80%. Careful design of the package has allowed for this performance to be achieved. The short leads allow the die size to be maximized and thermal resistance to be reduced within the confines of the TSOP-6 body size.

ASSOCIATED DOCUMENT

1206-8 ChipFET Dual Thermal performance, AN812 (<http://www.vishay.com/doc?71127>).

RECOMMENDED MINIMUM PADS FOR 1206-8 ChipFET®



Recommended Minimum Pads
Dimensions in Inches/(mm)

[Return to Index](#)



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