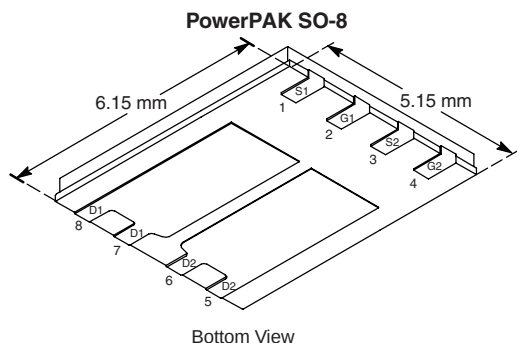


**Dual N-Channel 60-V (D-S) MOSFET****PRODUCT SUMMARY**

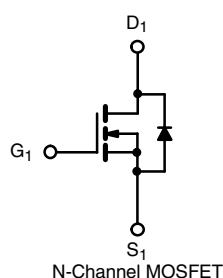
V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)
60	0.075 at $V_{GS} = 10$ V	4.6
	0.100 at $V_{GS} = 4.5$ V	4.0

FEATURES

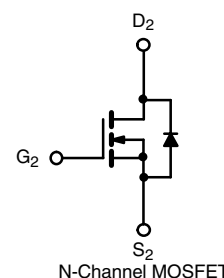
- Halogen-free According to IEC 61249-2-21 Available
- TrenchFET® Power MOSFET
- New Low Thermal Resistance PowerPAK® Package
- Dual MOSFET for Space Savings

**RoHS**
COMPLIANT
HALOGEN
FREE
Available

Ordering Information: Si7948DP-T1-E3 (Lead (Pb)-free)
Si7948DP-T1-GE3 (Lead (Pb)-free and Halogen-free)



N-Channel MOSFET



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS $T_A = 25$ °C, unless otherwise noted

ABSOLUTE MAXIMUM RATINGS $T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted					
Parameter		Symbol	10 s	Steady State	Unit
Drain-Source Voltage		V_{DS}	60		V
Gate-Source Voltage		V_{GS}	± 20		
Continuous Drain Current ($T_J = 150\text{ }^{\circ}\text{C}$) ^a	$T_A = 25\text{ }^{\circ}\text{C}$	I_D	4.6	3.0	A
	$T_A = 70\text{ }^{\circ}\text{C}$		3.6	2.4	
Pulsed Drain Current		I_{DM}	15		
Continuous Source Current (Diode Conduction) ^a		I_S	2.7	1.2	
Single Avalanche Current	L = 1.0 mH	I_{AS}	15		mJ
Single Avalanche Energy		E_{AS}	11		
Maximum Power Dissipation ^a	$T_A = 25\text{ }^{\circ}\text{C}$	P_D	3.3	1.4	W
	$T_A = 70\text{ }^{\circ}\text{C}$		2.1	0.9	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	- 55 to 150		$^{\circ}\text{C}$
Soldering Recommendations (Peak Temperature) ^{b, c}			260		

THERMAL RESISTANCE RATINGS

Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^a	$t \leq 10$ s	R_{thJA}	29	38	°C/W
	Steady State		60	85	
Maximum Junction-to-Case (Drain)	Steady State	R_{thJC}	4.0	5.2	

Notes

- Surface Mounted on 1" x 1" FR4 board.
- See Solder Profile (www.vishay.com/ppg273257). The PowerPAK SO-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

SPECIFICATIONS $T_J = 25^\circ\text{C}$, unless otherwise noted

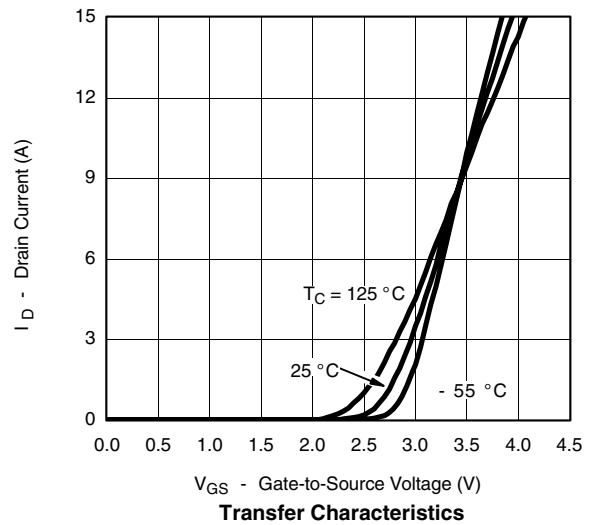
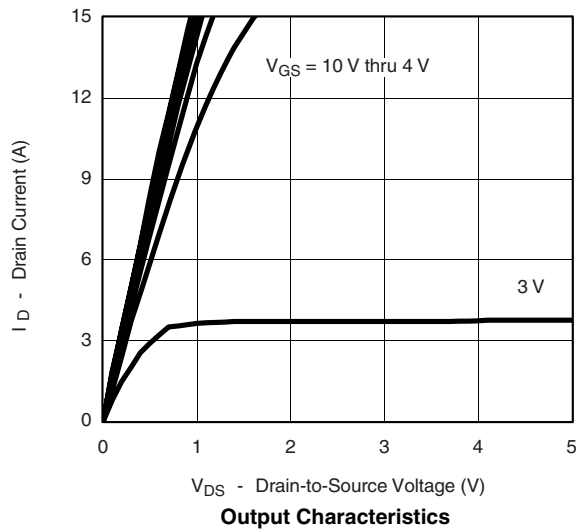
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250\ \mu\text{A}$	1		3	V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\ \text{V}$, $V_{GS} = \pm 20\ \text{V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 60\ \text{V}$, $V_{GS} = 0\ \text{V}$			1	μA
		$V_{DS} = 60\ \text{V}$, $V_{GS} = 0\ \text{V}$, $T_J = 55^\circ\text{C}$			5	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \geq 5\ \text{V}$, $V_{GS} = 10\ \text{V}$	15			A
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = 10\ \text{V}$, $I_D = 4.6\ \text{A}$		0.060	0.075	Ω
		$V_{GS} = 4.5\ \text{V}$, $I_D = 4.0\ \text{A}$		0.080	0.100	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 15\ \text{V}$, $I_D = 4.6\ \text{A}$		6		S
Diode Forward Voltage ^a	V_{SD}	$I_S = 2.7\ \text{A}$, $V_{GS} = 0\ \text{V}$		0.8	1.2	V
Dynamic^b						
Total Gate Charge	Q_g	$V_{DS} = 30\ \text{V}$, $V_{GS} = 10\ \text{V}$, $I_D = 15\ \text{A}$		12	20	nC
Gate-Source Charge	Q_{gs}			2		
Gate-Drain Charge	Q_{gd}			3.5		
Gate Resistance	R_g			1.5		Ω
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 30\ \text{V}$, $R_L = 2\ \Omega$ $I_D \cong 15\ \text{A}$, $V_{GEN} = 10\ \text{V}$, $R_g = 2.5\ \Omega$		7	20	ns
Rise Time	t_r			8	25	
Turn-Off Delay Time	$t_{d(off)}$			15	40	
Fall Time	t_f			7	20	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = 2.7\ \text{A}$, $dI/dt = 100\ \text{A}/\mu\text{s}$		30	60	

Notes:

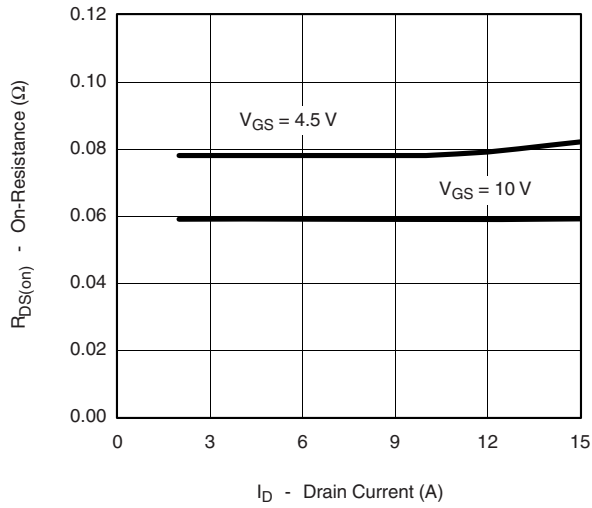
a. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.

b. Guaranteed by design, not subject to production testing.

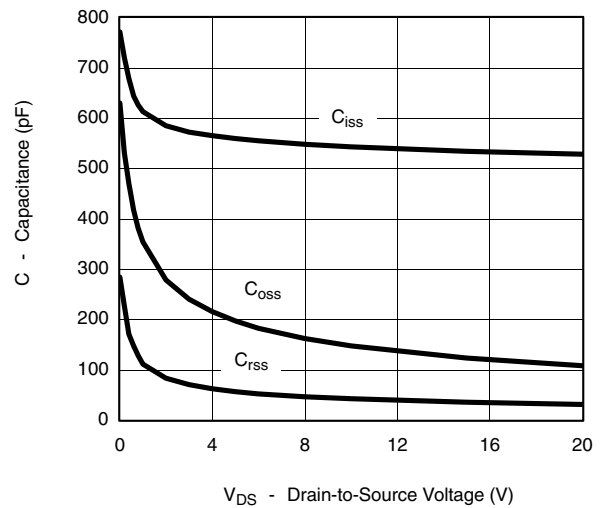
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS 25°C , unless otherwise noted

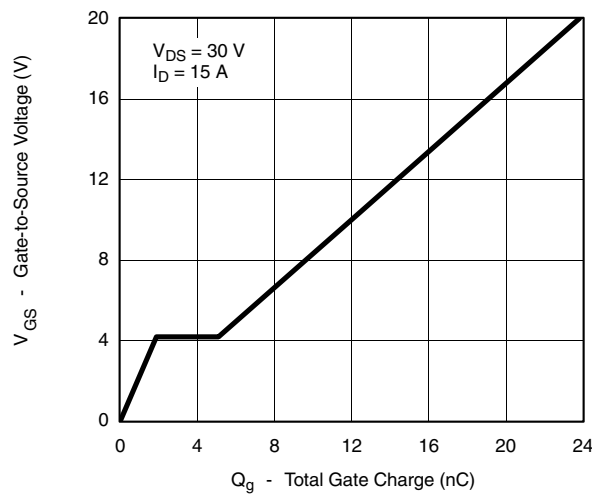
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



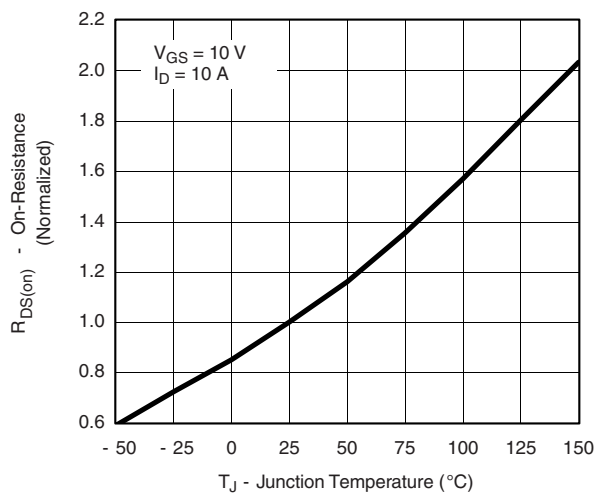
On-Resistance vs. Drain Current



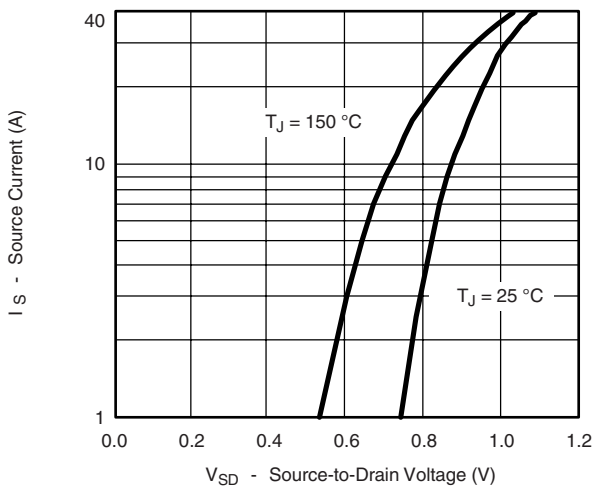
Capacitance



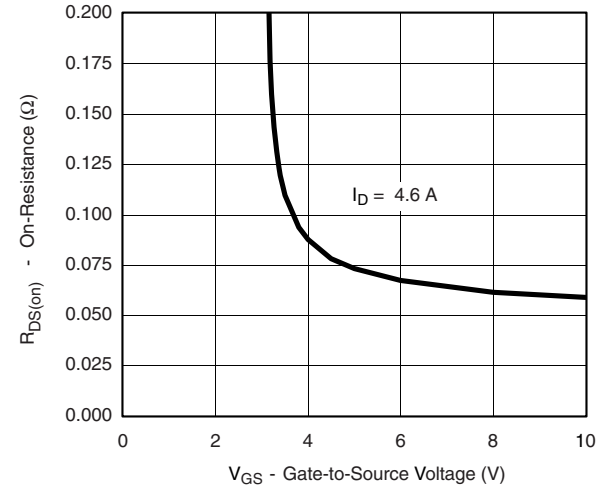
Gate Charge



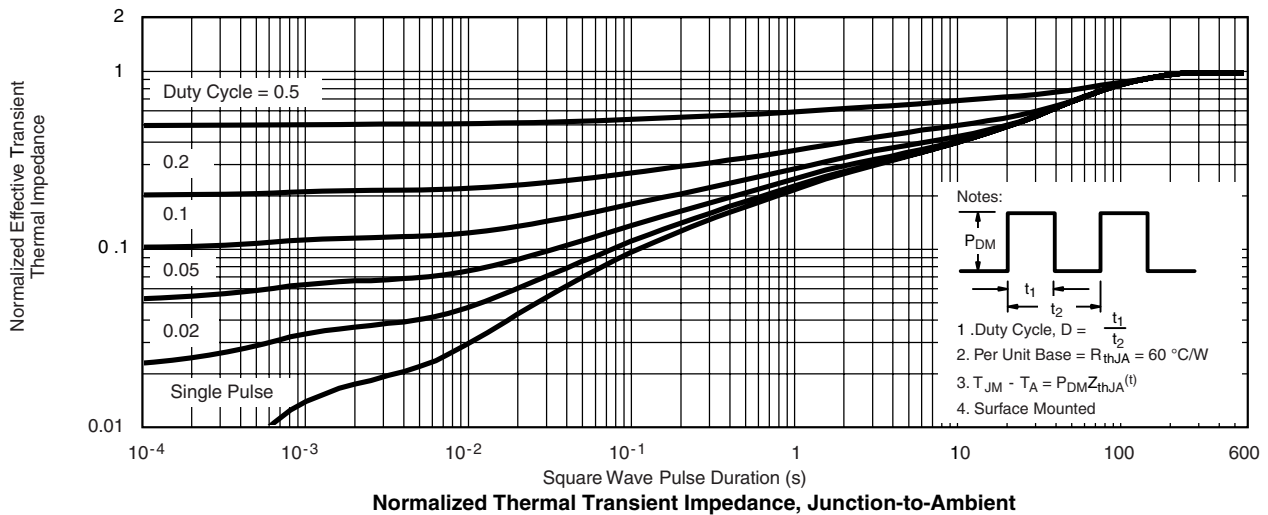
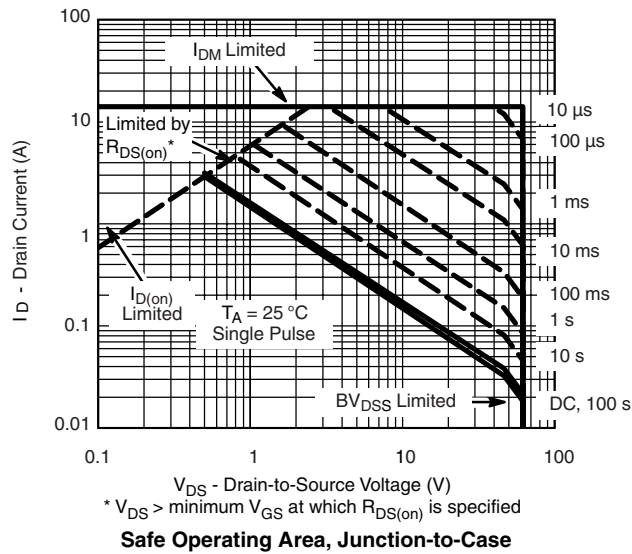
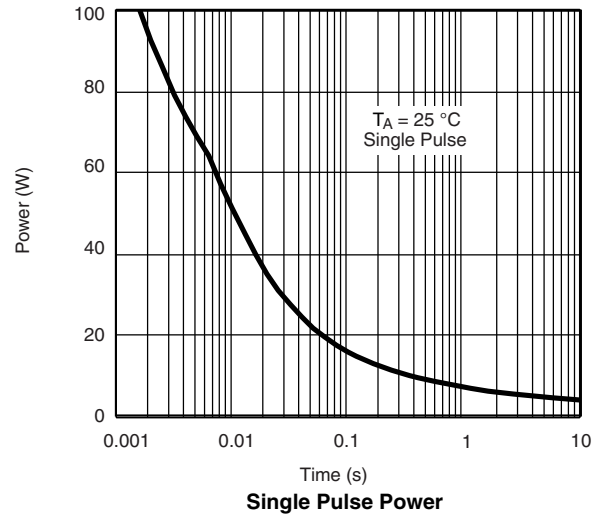
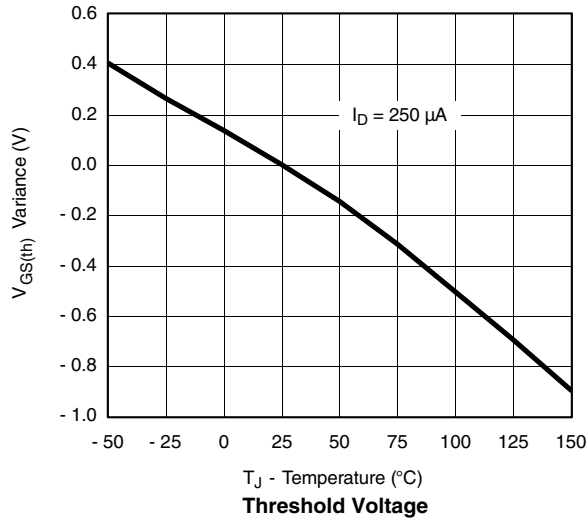
On-Resistance vs. Junction Temperature



Source-Drain Diode Forward Voltage

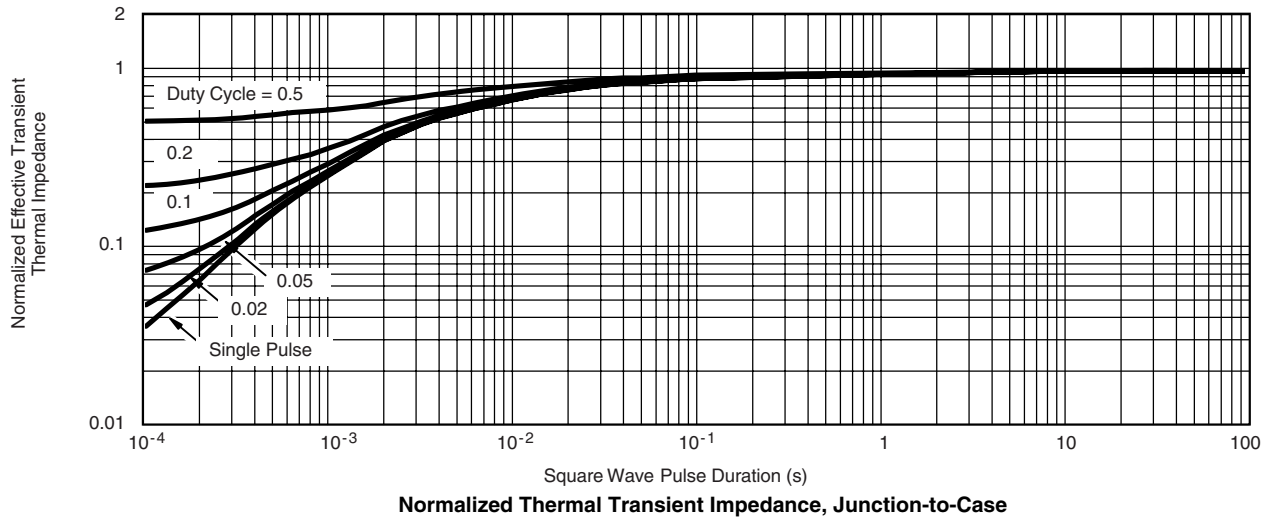


On-Resistance vs. Gate-to-Source Voltage

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



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