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FDI040N06

N-Channel PowerTrench® MOSFET

60V, 168A, 4.0mΩ

Features

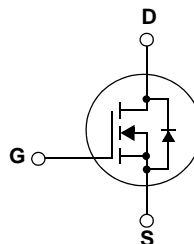
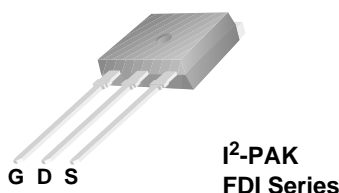
- $R_{DS(on)} = 3.2m\Omega$ (Typ.) @ $V_{GS} = 10V$, $I_D = 75A$
- Fast Switching Speed
- Low Gate Charge
- High Performance Trench Technology for Extremely Low $R_{DS(on)}$
- High Power and Current Handling Capability
- RoHS Compliant

General Description

This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench process that has been especially tailored to minimize the on-state resistance and yet maintain superior switching performance.

Application

- DC to DC converters / Synchronous Rectification



MOSFET Maximum Ratings $T_C = 25^\circ C$ unless otherwise noted

Symbol	Parameter	FDI040N06	Units
V_{DSS}	Drain to Source Voltage	60	V
V_{GSS}	Gate to Source Voltage	± 20	V
I_D	Drain Current	-Continuous ($T_C = 25^\circ C$, Silicion Limited)	A
		-Continuous ($T_C = 100^\circ C$, Silicion Limited)	
		-Continuous ($T_C = 25^\circ C$, Package Limited)	
I_{DM}	Drain Current	- Pulsed (Note 1)	A
E_{AS}	Single Pulsed Avalanche Energy	(Note 2)	mJ
dv/dt	Peak Diode Recovery dv/dt	(Note 3)	V/ns
P_D	Power Dissipation	($T_C = 25^\circ C$)	W
		- Derate above $25^\circ C$	W/ $^\circ C$
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +175	$^\circ C$
T_L	Maximum Lead Temperature for Soldering Purpose, 1/8" from Case for 5 Seconds	300	$^\circ C$

*Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 120A.

Thermal Characteristics

Symbol	Parameter	FDI040N06	Units
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max	0.65	$^\circ C/W$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max	62.5	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDI040N06	FDI040N06	TO-262	Tube	-	50

Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
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Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250\mu\text{A}$, $V_{GS} = 0\text{V}$, $T_C = 25^\circ\text{C}$	60	-	-	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\mu\text{A}$, Referenced to 25°C	-	0.04	-	$V/^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 60\text{V}$, $V_{GS} = 0\text{V}$	-	-	1	μA
		$V_{DS} = 60\text{V}$, $V_{GS} = 0\text{V}$, $T_C = 150^\circ\text{C}$	-	-	500	
I_{GSS}	Gate to Body Leakage Current	$V_{GS} = \pm 20\text{V}$, $V_{DS} = 0\text{V}$	-	-	± 100	nA

On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 250\mu\text{A}$	2.5	3.5	4.5	V
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{V}$, $I_D = 75\text{A}$	-	3.2	4.0	$\text{m}\Omega$
g_{FS}	Forward Transconductance	$V_{DS} = 10\text{V}$, $I_D = 75\text{A}$	-	169	-	S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 25\text{V}$, $V_{GS} = 0\text{V}$ $f = 1\text{MHz}$	-	6190	8235	pF
C_{oss}	Output Capacitance		-	900	1195	pF
C_{rss}	Reverse Transfer Capacitance		-	385	580	pF
$Q_{g(tot)}$	Total Gate Charge at 10V	$V_{DS} = 48\text{V}$, $I_D = 75\text{A}$ $V_{GS} = 10\text{V}$ (Note 4)	-	102	133	nC
Q_{gs}	Gate to Source Gate Charge		-	32	-	nC
Q_{gd}	Gate to Drain "Miller" Charge		-	32	-	nC

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 30\text{V}$, $I_D = 75\text{A}$ $V_{GS} = 10\text{V}$, $R_{GEN} = 4.7\Omega$ (Note 4)	-	30	70	ns
t_r	Turn-On Rise Time		-	40	90	ns
$t_{d(off)}$	Turn-Off Delay Time		-	55	120	ns
t_f	Turn-Off Fall Time		-	24	58	ns

Drain-Source Diode Characteristics

I _S	Maximum Continuous Drain to Source Diode Forward Current		-	-	168	A
I _{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	672	A
V _{SD}	Drain to Source Diode Forward Voltage	V _{GS} = 0V, I _{SD} = 75A	-	-	1.3	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0V, I _{SD} = 75A	-	41	-	ns
Q _{rr}	Reverse Recovery Charge	dI _F /dt = 100A/μs	-	47	-	nC

Notes:

- 1: Repetitive Rating: Pulse width limited by maximum junction temperature
- 2: $L = 0.31\text{mH}$, $I_{AS} = 75\text{A}$, $V_{DD} = 50\text{V}$, $R_G = 25\Omega$, Starting $T_J = 25^\circ\text{C}$
- 3: $I_{SD} \leq 75\text{A}$, $di/dt \leq 200\text{A}/\mu\text{s}$, $V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^\circ\text{C}$
- 4: Essentially Independent of Operating Temperature Typical Characteristics

Typical Performance Characteristics

Figure 1. On-Region Characteristics

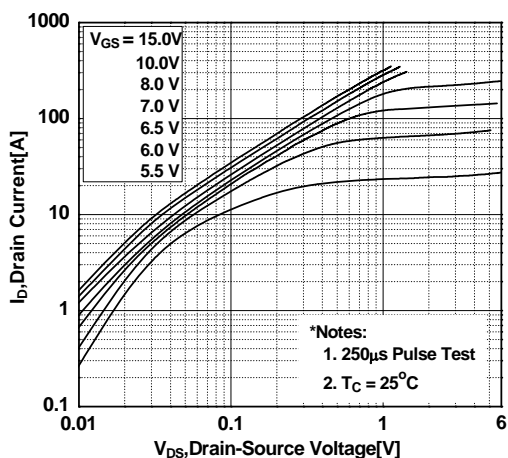


Figure 2. Transfer Characteristics

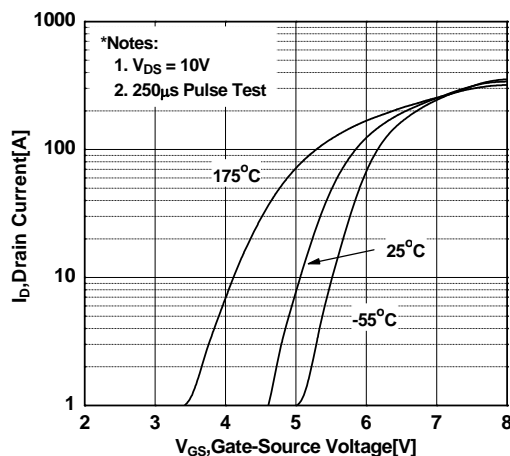


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

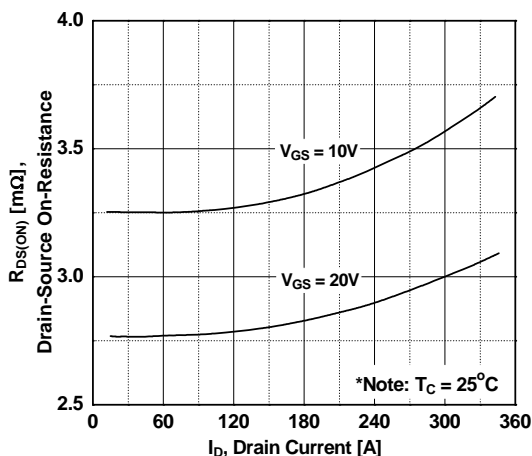


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

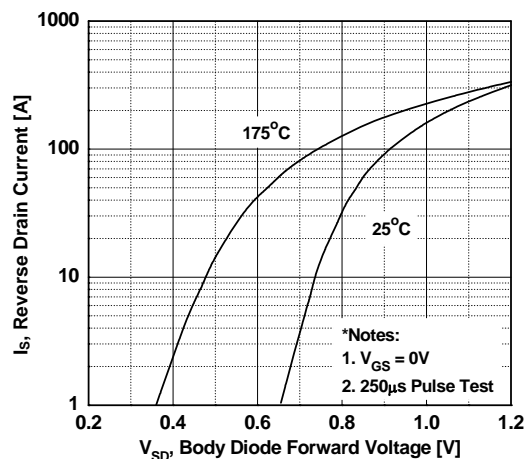


Figure 5. Capacitance Characteristics

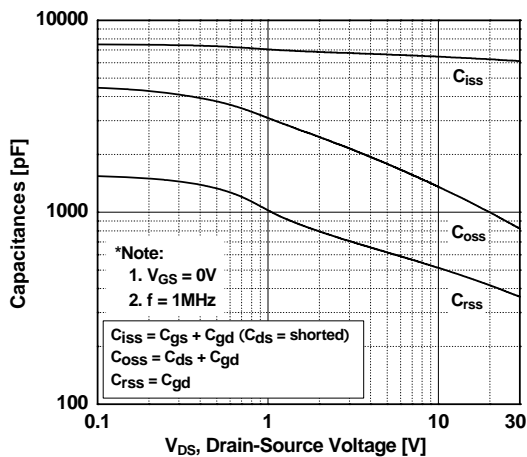
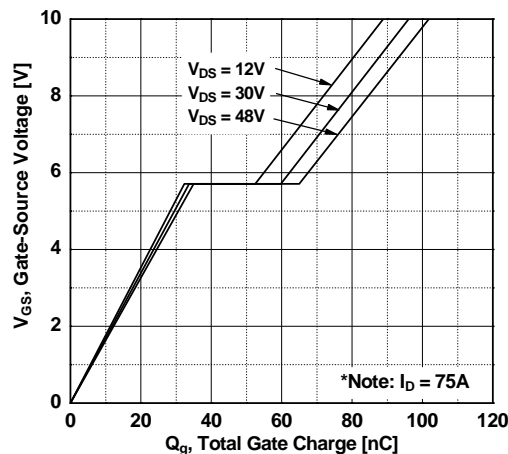


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

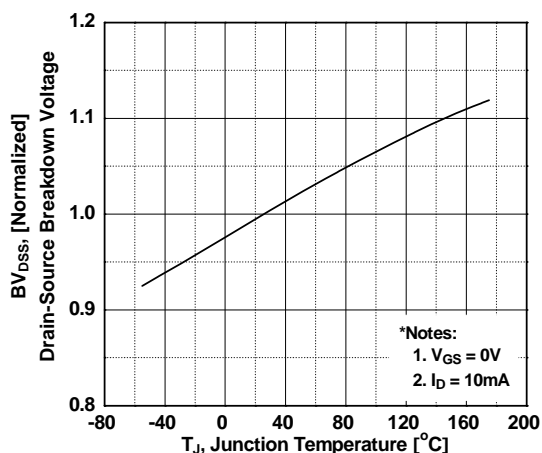


Figure 8. On-Resistance Variation vs. Temperature

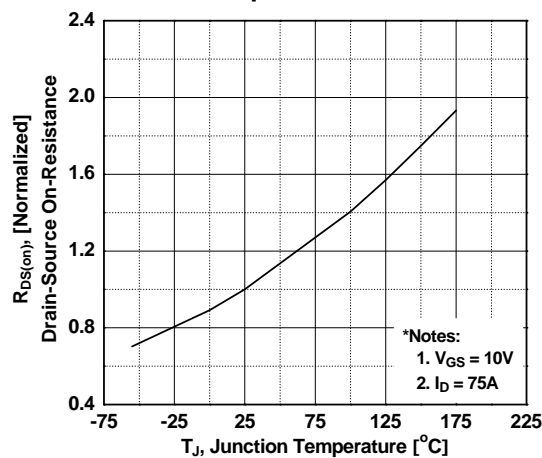


Figure 9. Maximum Safe Operating Area

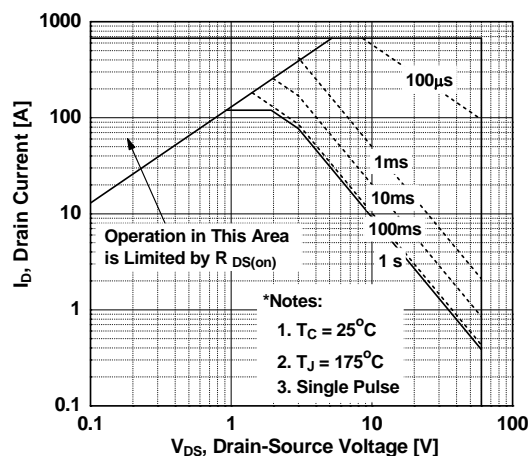


Figure 10. Maximum Drain Current vs. Case Temperature

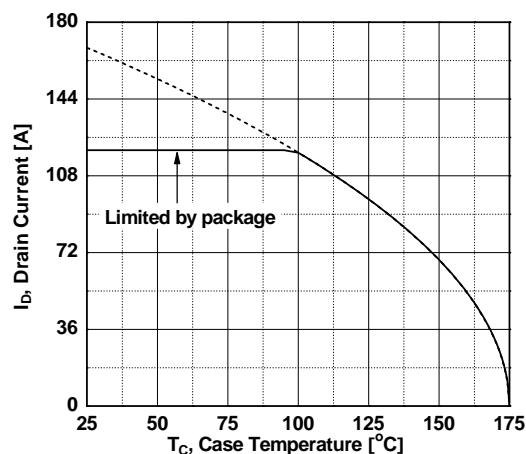
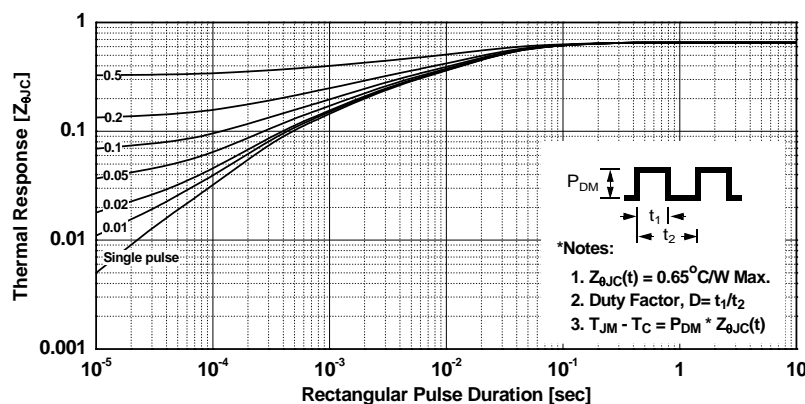


Figure 11. Transient Thermal Response Curve



Gate Charge Test Circuit & Waveform



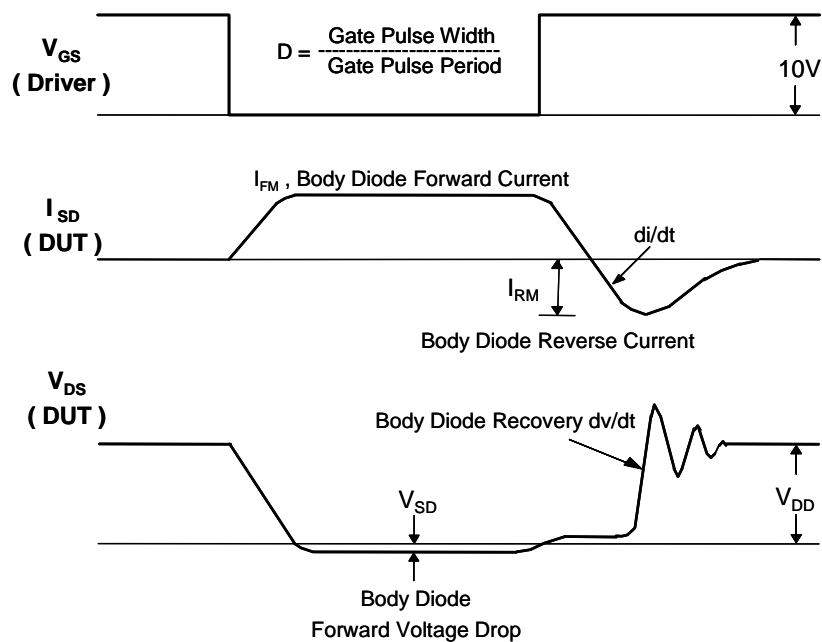
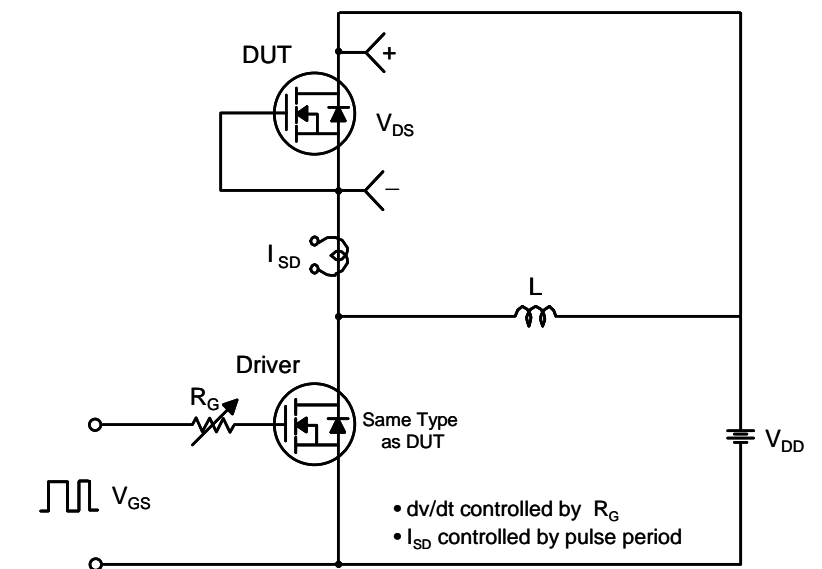
Resistive Switching Test Circuit & Waveforms



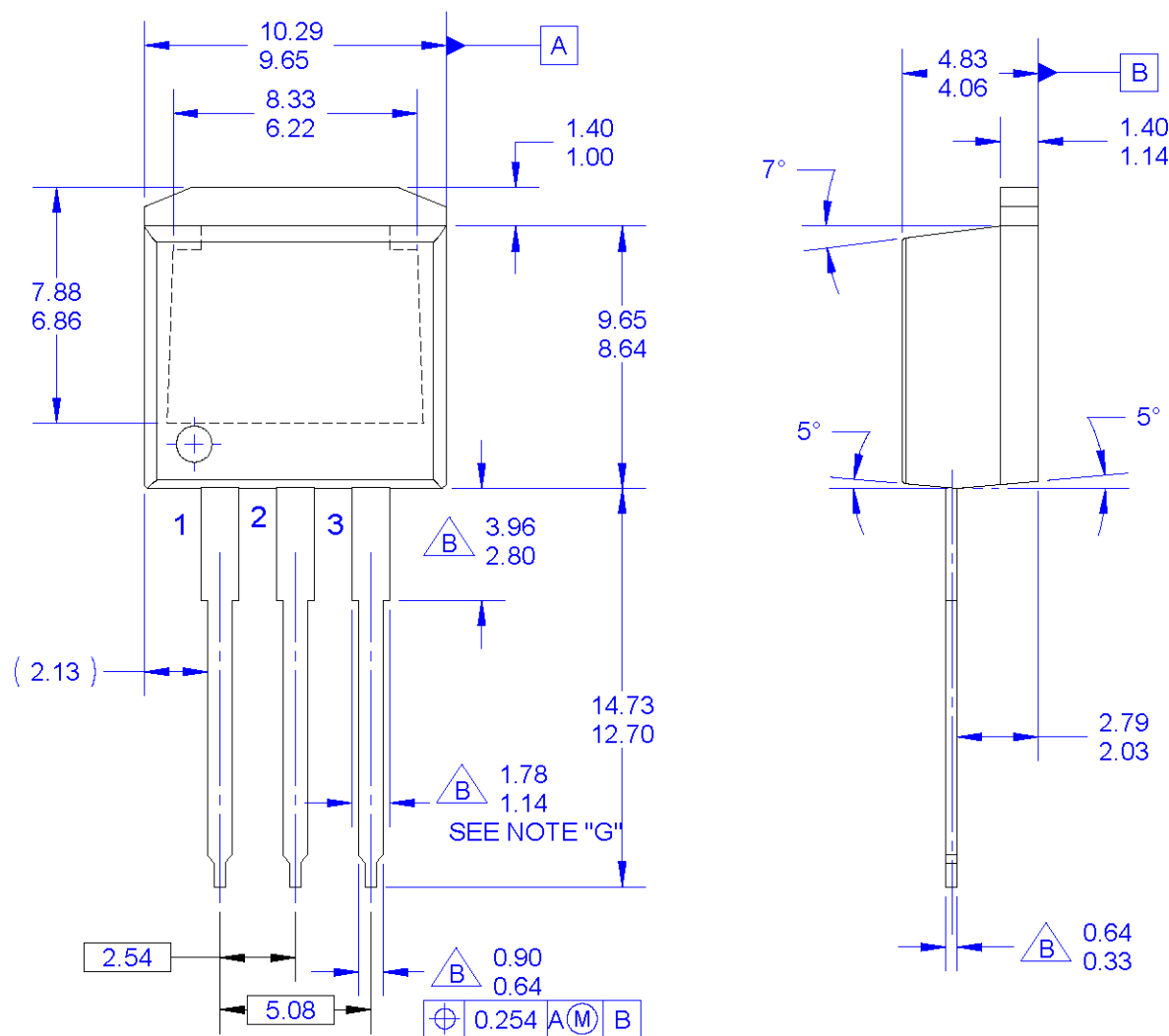
Unclamped Inductive Switching Test Circuit & Waveforms



Peak Diode Recovery dv/dt Test Circuit & Waveforms



Mechanical Dimensions

I²-PAK

NOTES:

- A. EXCEPT WHERE NOTED CONFORMS TO TO262 JEDEC VARIATION AA.
- B. DOES NOT COMPLY JEDEC STD. VALUE.
- C. ALL DIMENSIONS ARE IN MILLIMETERS.
- D. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR PROTRUSIONS.
- E. DIMENSION AND TOLERANCE AS PER ANSI Y14.5-1994.
- F. LOCATION OF PIN HOLE MAY VARY (LOWER LEFT CORNER, LOWER CENTER AND CENTER OF PACKAGE)
- G. MAXIMUM WIDTH FOR F102 DEVICE = 1.35 MAX.
- H. DRAWING FILE NAME: TO262A03REV5

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