

Features

- High Gain: 24 dB
- P1dB: 37.5 dBm
- P_{SAT}: 38.5 dBm
- IM3 Level: -24 dBc @ P_{OUT} = 33 dBm/tone
- Power Added Efficiency: 23% @ P_{SAT}
- Return Loss: 12 dB
- Bare Die Dimensions: 3.6 x 3.8 x 0.05 mm
- RoHS* Compliant

Description

The MAAP-011140-DIE is a 4-stage, 6 W power amplifier in bare die form. This power amplifier operates from 27.5 to 30.0 GHz and provides 24 dB of linear gain, 6 W saturated output power, and 23% efficiency while biased at 6 V.

The MAAP-011140-DIE is a power amplifier ideally suited for VSAT communications.

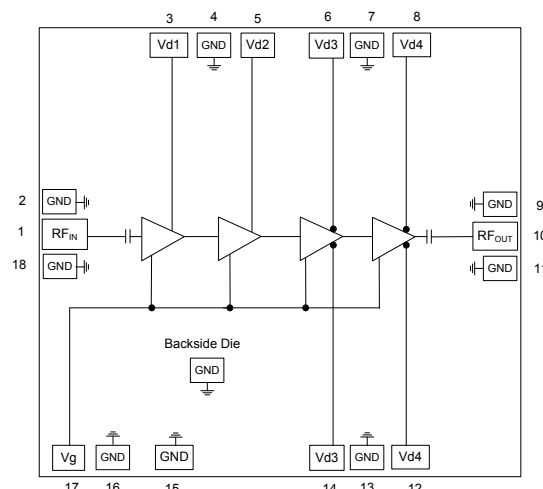
This product is fabricated using a GaAs pHEMT device process which features full passivation for enhanced reliability.

Ordering Information

Part Number	Package
MAAP-011140-DIE	Die in Gel Pack ¹

1. Die quantity varies

Functional Diagram



Pin Configuration²

Pad	Function	Description
1	RF _{IN}	RF Input
2, 4, 7, 9, 11, 13, 15, 16, 18 & backside	GND	Ground
3	V _{D1}	Drain Voltage Stage 1
5	V _{D2}	Drain Voltage Stage 2
6, 14	V _{D3}	Drain Voltage Stage 3
8, 12	V _{D4}	Drain Voltage Stage 4
10	RF _{OUT}	RF Output
17	V _G	Gate Voltage

2. Backside metal is RF, DC and thermal ground.

* Restrictions on Hazardous Substances, European Union Directive 2011/65/EU.

Electrical Specifications³: Freq. = 30 GHz, $T_C = +25^\circ\text{C}$, $V_D = +6\text{ V}$, $Z_0 = 50\ \Omega$

Parameter	Test Conditions	Units	Min.	Typ.	Max.
Gain	$P_{IN} = 0\text{ dBm}$	dB	22	24	—
P_{OUT}	$P_{IN} = 17\text{ dBm}$	dBm	36.0	37.5	—
IM3 Level	$P_{OUT} = 33\text{ dBm / tone}$	dBc	—	-24	—
Power Added Efficiency	$P_{SAT} (P_{IN} = 17\text{ dBm})$	%		23	
Input Return Loss	$P_{IN} = -20\text{ dBm}$	dB	—	12	—
Output Return Loss	$P_{IN} = -20\text{ dBm}$	dB	—	12	—
Quiescent Current	I_{DQ} (see bias conditions, page 5)	mA	—	3000	—
Current	$P_{SAT} (P_{IN} = 17\text{ dBm})$	mA	—	5250	—

3. Specifications apply to MMIC die with two RF input and two RF output bond wires, and tested with 50 Ω GSG probes. Further performance tuning to optimize the RF input and RF output impedance matching is shown on Recommended Bonding Diagram and PCB Layout Detail (pg. 4). Typical performance curves are achieved by using the recommended bonding diagram and PCB layout detail.

Maximum Operating Ratings

Parameter	Rating
Input Power	+19 dBm
Junction Temperature ^{4,5}	+160°C
Operating Temperature	-40°C to +85°C

4. Operating at nominal conditions with $T_C \leq +160^\circ\text{C}$ will ensure $MTTF > 1 \times 10^6$ hours.

5. Junction Temperature (T_J) = $T_C + \Theta_{JC} * ((V * I) - (P_{OUT} - P_{IN}))$

Typical thermal resistance (Θ_{JC}) = 3.4°C/W.

a) For $T_C = +25^\circ\text{C}$,

$T_J = 108^\circ\text{C}$ @ 6 V, 5.25 A, $P_{OUT} = 38.5$, $P_{IN} = 17\text{ dBm}$

b) For $T_C = +80^\circ\text{C}$,

$T_J = 159^\circ\text{C}$ @ 6 V, 4.96 A, $P_{OUT} = 38.1$, $P_{IN} = 17\text{ dBm}$

Absolute Maximum Ratings^{6,7}

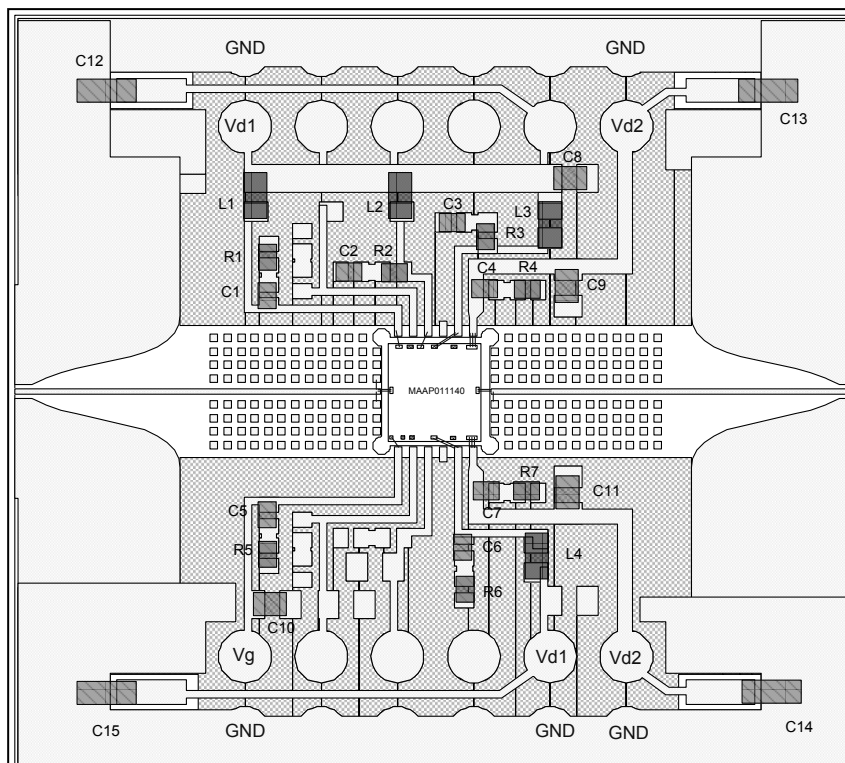
Parameter	Absolute Maximum
Input Power	+24 dBm
Drain Voltage	+6.5 V
Gate Voltage	-3 to 0 V
Junction Temperature ⁸	+175°C
Storage Temperature	-65°C to +150°C

6. Exceeding any one or combination of these limits may cause permanent damage to this device.

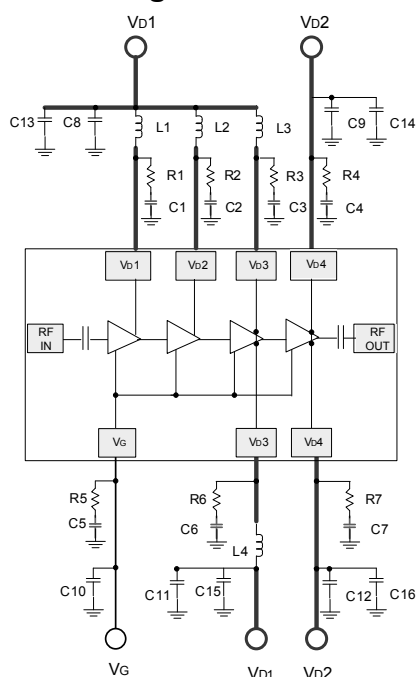
7. MACOM does not recommend sustained operation near these survivability limits.

8. Junction Temperature directly effects device MTTF. Junction temperature should be kept as low as possible to maximize lifetime.

Application PCB Layout



Application Diagram



Application Parts List

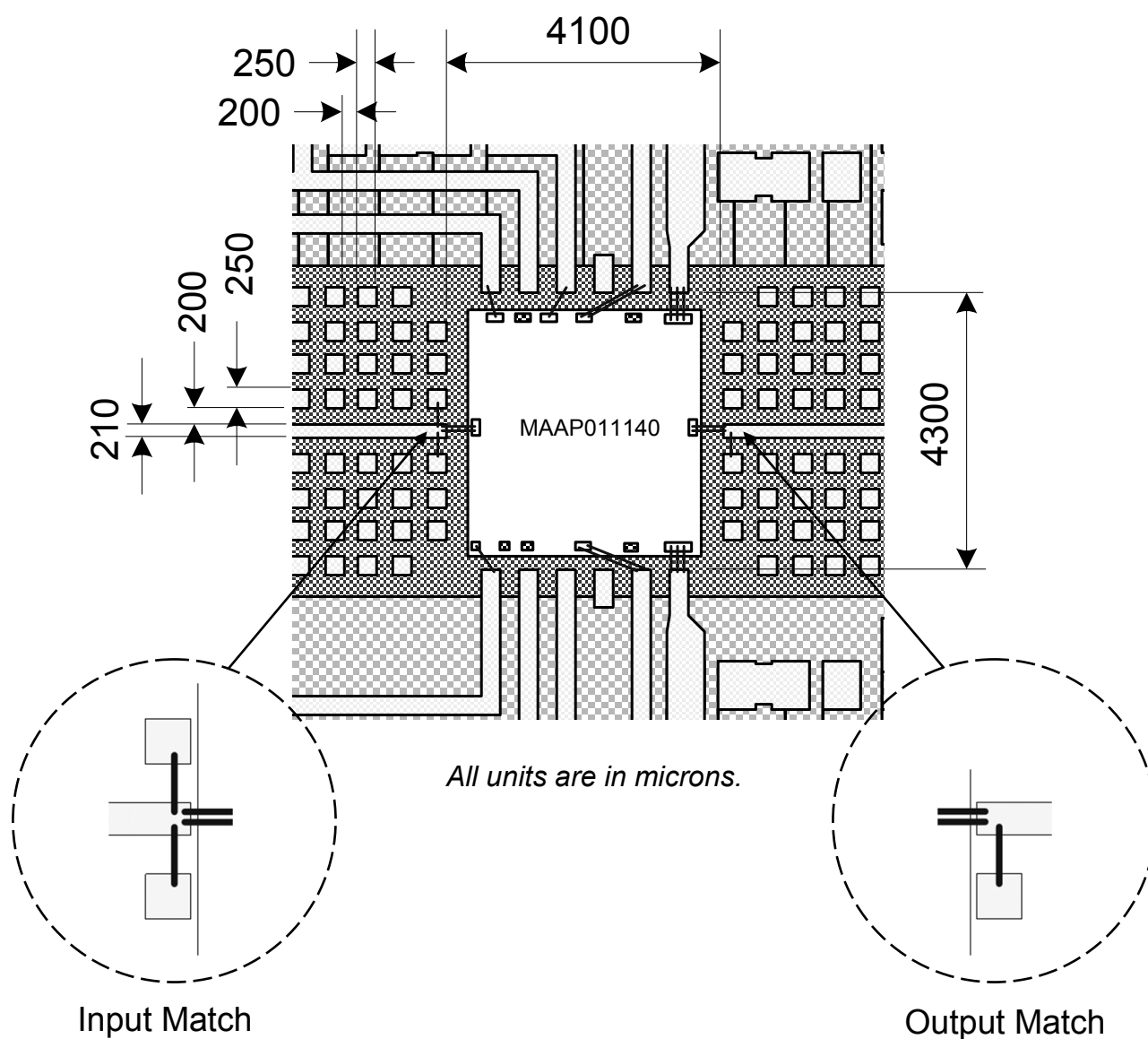
Part	Value	Case Style
C1 - C7	0.01 μ F	0402
C8 - C12	1 μ F	0603
C13 - C16	10 μ F	0805
R1 - R7	10 Ω	0402
L1 - L4 (Chip Ferrite Bead)	BLM18HE601SN1D	0603

PCB Material Specifications

Top Layer: 1/2 oz Copper Cladding, 0.017 mm thickness
Dielectric Layer: Rogers RO4350B, 0.101 mm thickness
Bottom Layer: 1/2 oz Copper Cladding, 0.017 mm thickness
Finished overall thickness: 0.135 mm

Recommended Bonding Diagram and PCB Layout Detail:

For optimum power match, RF input and output microstrip lines require open stubs on the application board for bonding wire inductance compensation. Optimum bonding wire inductance for the RF I/O connection is 0.2 nH, and physical length for the gold bond wire (.001" dia.) is approximately 350 μm each for the two wire connection.



Application Information

The MAAP-011140 is designed to be easy to use yet high performance. The ultra small size and simple bias allows easy placement on system board. RF input and output ports are DC de-coupled internally.

Biasing conditions

Recommended biasing conditions are $V_D = 6$ V, $I_{DQ} = 3000$ mA (controlled with V_G). The drain bias voltage range, V_D , is 3 to 6.5 V, and the quiescent drain current biasing range, I_{DQ} , is 2000 to 4000 mA.

V_D bias must be applied to V_{D1} , V_{D2} , V_{D3} , and V_{D4} pads.

Both V_{D3} pads (6 and 14) are required for current symmetry.

Both V_{D4} pads (8 and 12), are required for current symmetry.

A single DC voltage (V_G) will bias all amplifier stages. Muting can be accomplished by setting the V_G to the pinched off voltage ($V_G = -2$ V).

Die Attachment

This product is manufactured from 0.050 mm (0.002") thick GaAs substrate and has vias through to the backside to enable grounding to the circuit.

Recommended conductive epoxy is Namics Unimec XH9890-6. Epoxy should be applied and cured in accordance with the manufacturer's specifications and should avoid contact with the top of the die.

Operating the MAAP-011140-DIE

Turn-on

1. Apply V_G (-1.5 V).
2. Apply V_D (6.0 V typical).
3. Set I_{DQ} by adjusting V_G more positive (typically $V_G \sim -0.9$ V for $I_{DQ} = 3000$ mA).
4. Apply RF_{IN} signal.

Turn-off

1. Remove RF_{IN} signal.
2. Decrease V_G to -1.5 V.
3. Decrease V_D to 0 V.

Handling Procedures

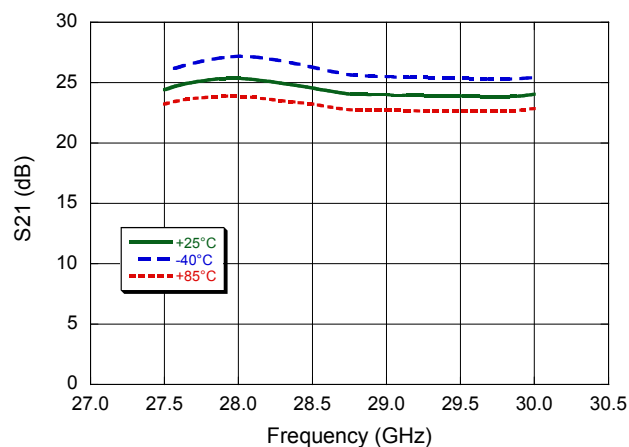
Please observe the following precautions to avoid damage:

Static Sensitivity

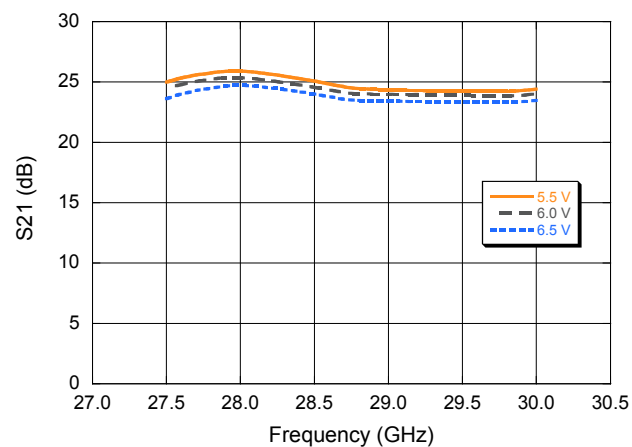
These electronic devices are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these devices.

Typical Performance Curves⁹

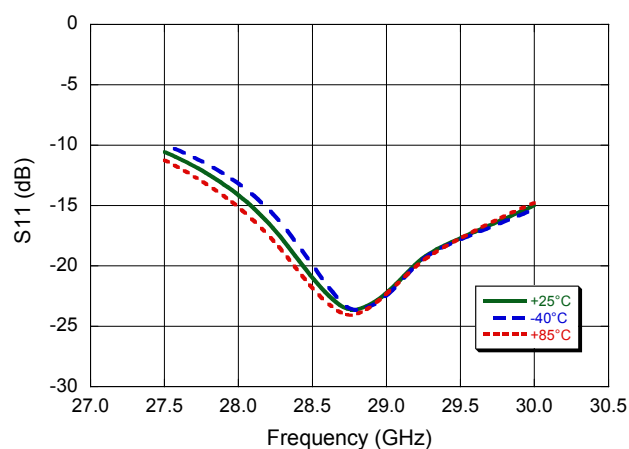
Small Signal Gain vs. Frequency over Temperature



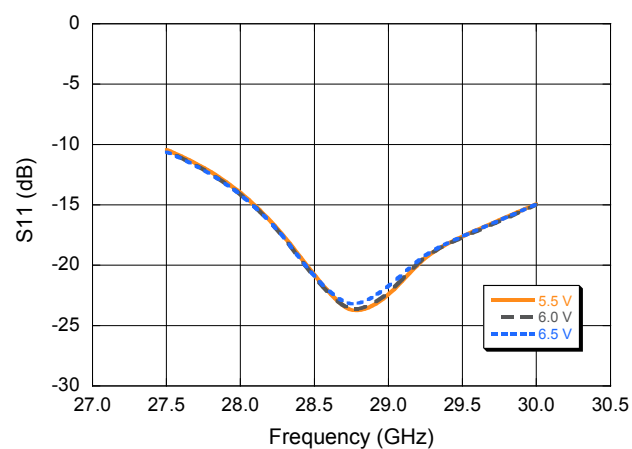
Small Signal Gain vs. Frequency over Bias Voltage



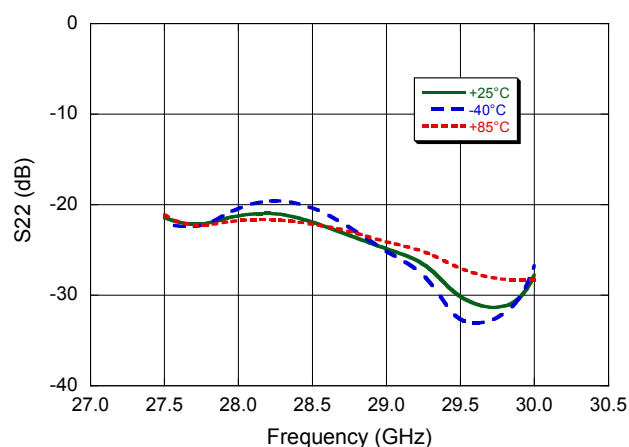
Input Return Loss vs. Frequency over Temperature



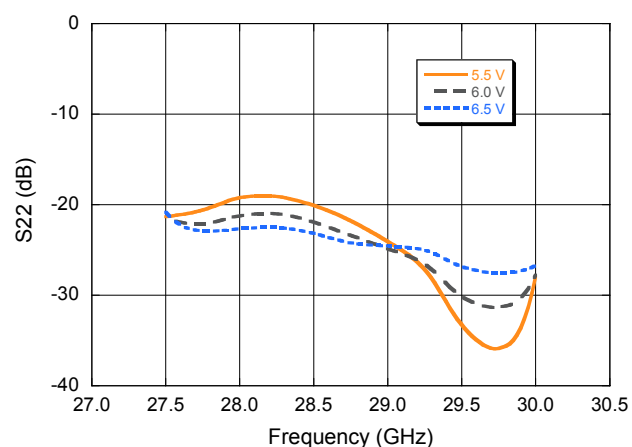
Input Return Loss vs. Frequency over Bias Voltage



Output Return Loss vs. Frequency over Temperature

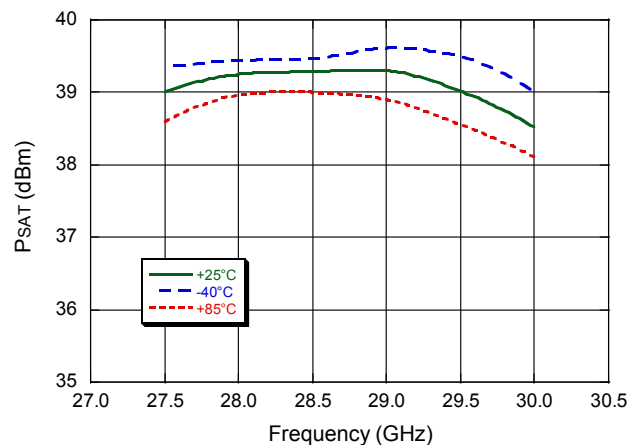


Output Return Loss vs. Frequency over Bias Voltage

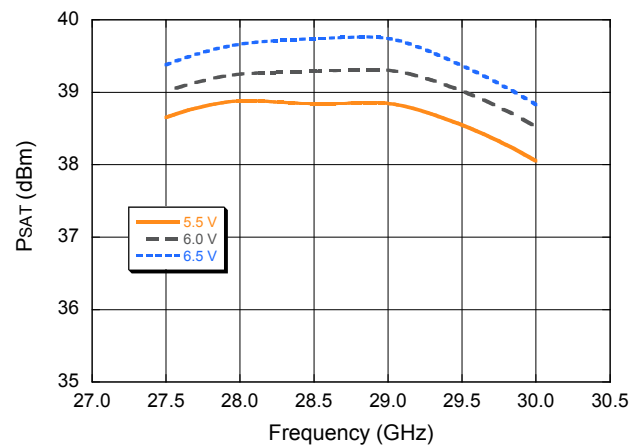


Typical Performance Curves⁹

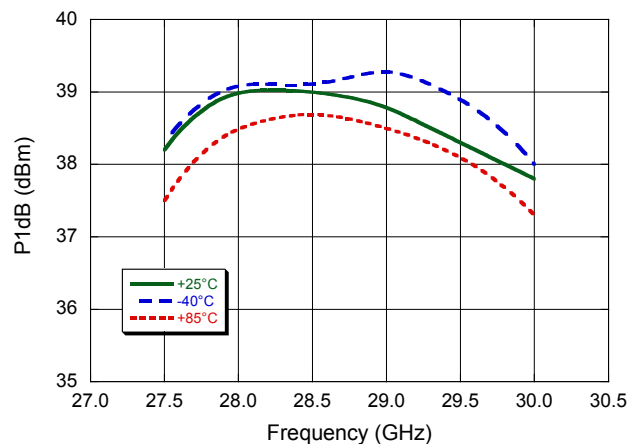
P_{SAT} vs. Frequency over Temperature



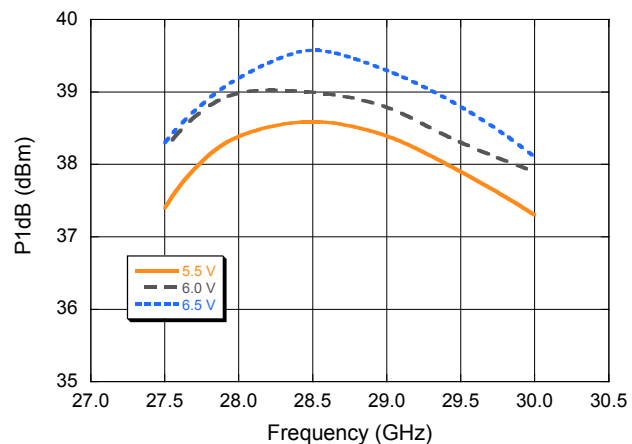
P_{SAT} vs. Frequency over Bias Voltage



$P1dB$ vs. Frequency over Temperature

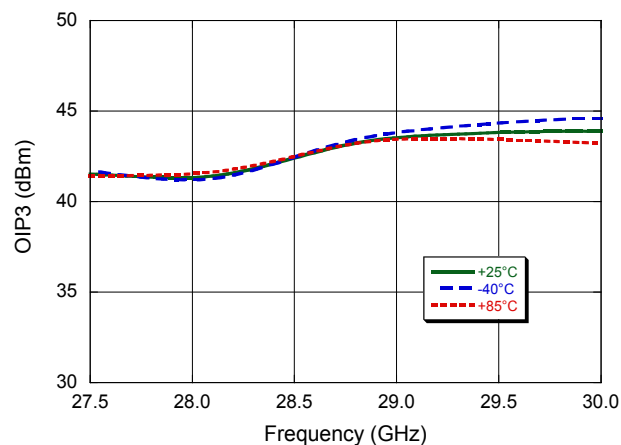


$P1dB$ vs. Frequency over Bias Voltage

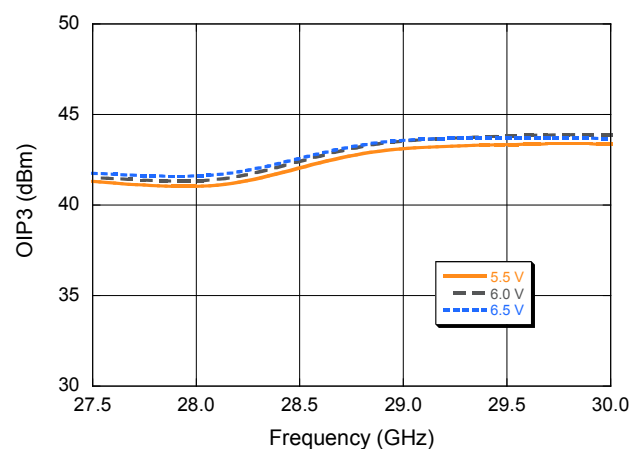


Typical Performance Curves⁹

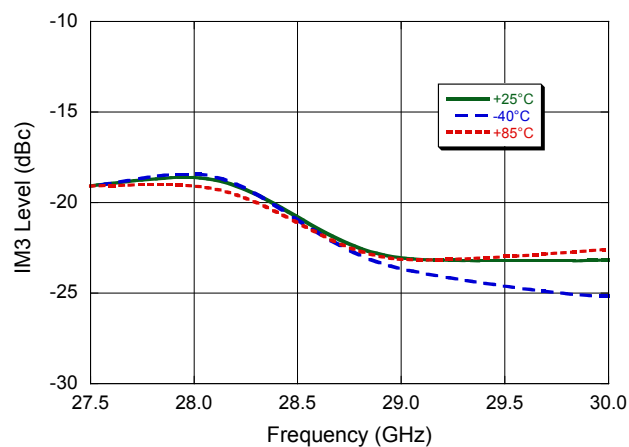
Output IP3 vs. Frequency over Temperature



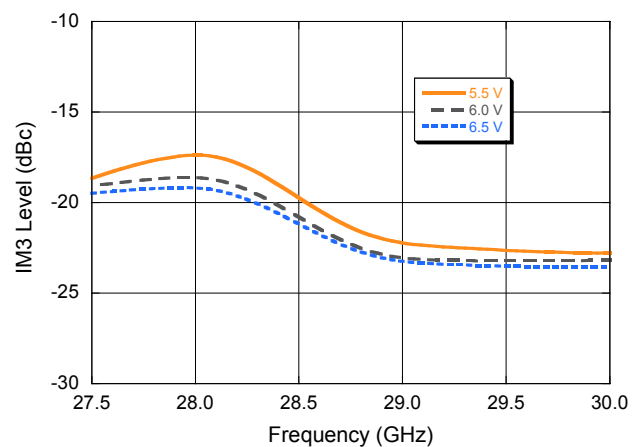
Output IP3 vs. Frequency over Bias Voltage



IM3 vs. Frequency over Temperature
($P_{OUT} = +33$ dBm/Tone)

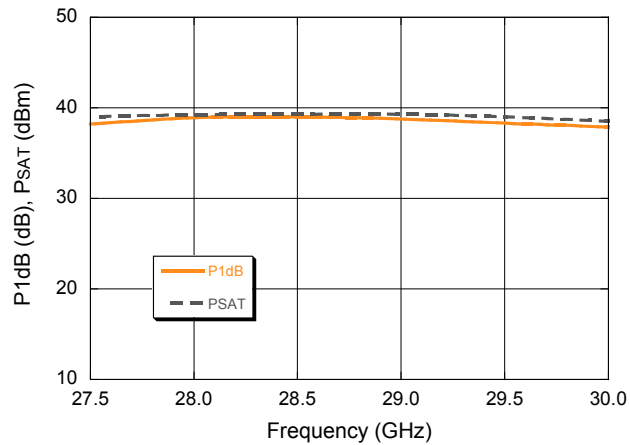


IM3 vs. Frequency over Bias Voltage
($P_{OUT} = +33$ dBm/Tone)

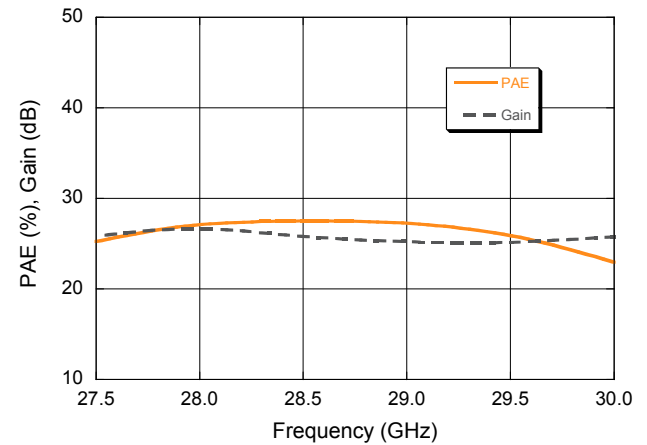


Typical Performance Curves⁹

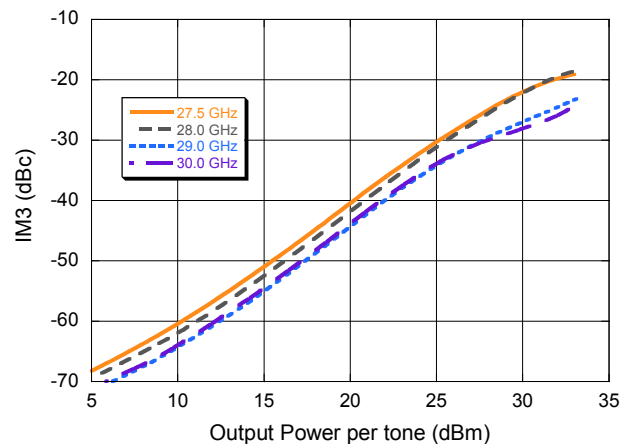
P_{1dB}, P_{SAT} vs. Frequency



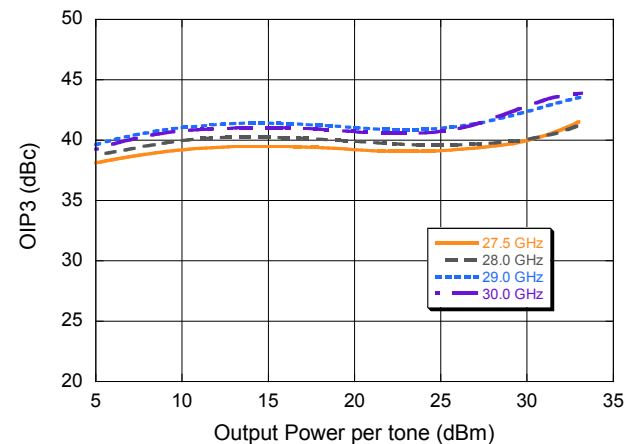
PAE, Gain vs. Frequency



IM3 vs. Output Power per Tone

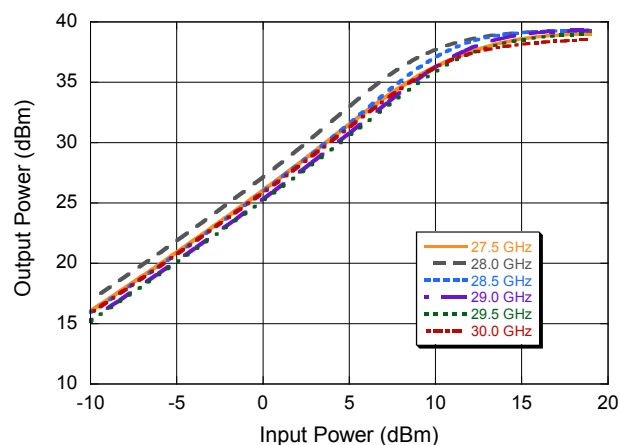


Output IP3 vs. Output Power per Tone

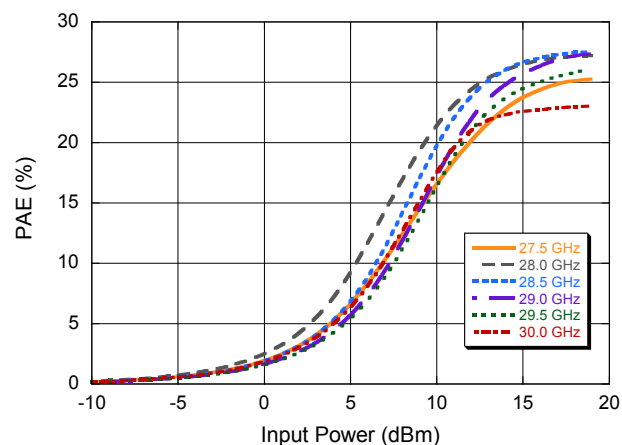


Typical Performance Curves⁹

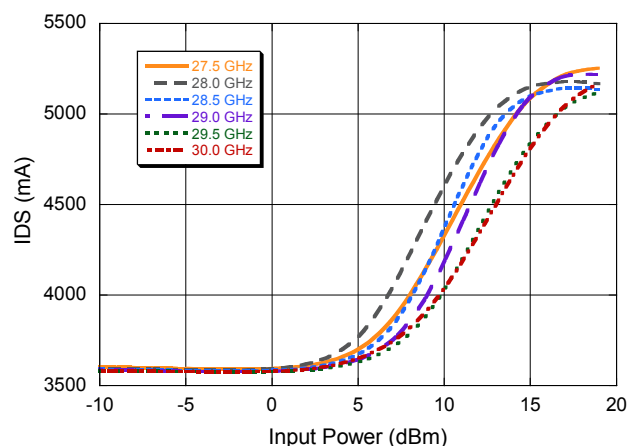
Output Power vs. Input Power



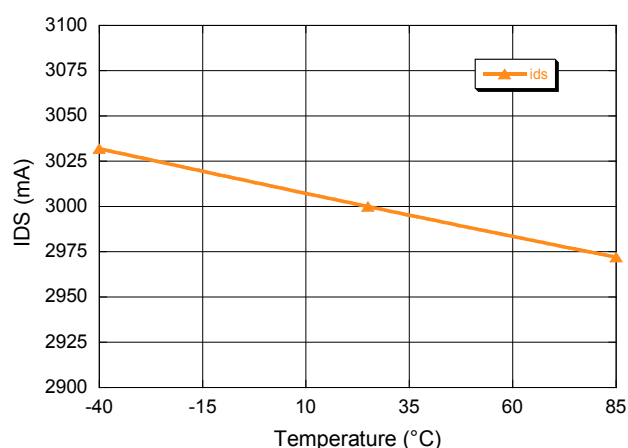
PAE vs. Input Power



Drain Current vs. Input Power

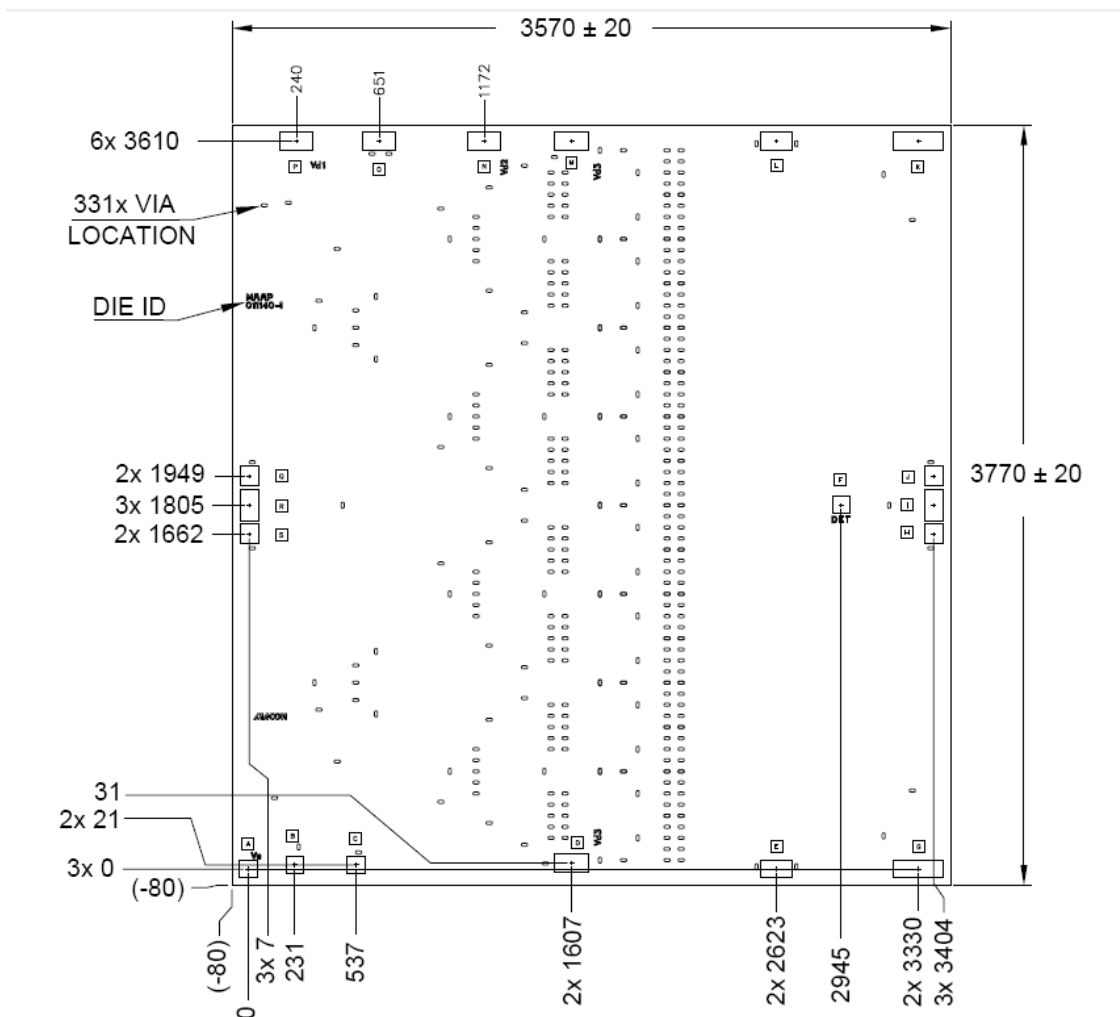


Quiescent Drain Current over Temperature



9. Typical performance curves are achieved by using the recommended bonding diagram and PCB layout detail.

MMIC Die Outline



Bond Pad Detail

Pad	Size (x)	Size (y)
A, B, C	88	88
D, M	169	88
E, L, O	161	88
F	84	84
G, K	249	88
H, J, Q, S	89	99
I, R	89	159
N, P	158	88

Notes:

1. All units are in μm , unless otherwise noted, with a tolerance of $\pm 5 \mu\text{m}$.
2. Die thickness is $50 \pm 10 \mu\text{m}$.

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