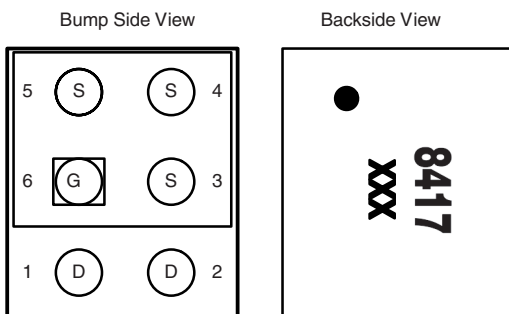


P-Channel 1.8 V (G-S) MOSFET

PRODUCT SUMMARY

V _{DS} (V)	R _{DS(on)} (Ω)	I _D (A) ^a	Q _g (Typ.)
- 12	0.021 at V _{GS} = - 4.5 V	- 14.5	35 nC
	0.026 at V _{GS} = - 2.5 V	- 13.0	
	0.033 at V _{GS} = - 1.8 V	- 11.5	

MICRO FOOT



Device Marking: 8417
xxx = Date/Lot Traceability Code

Ordering Information: Si8417DB-T2-E1 (Lead (Pb)-free)

FEATURES

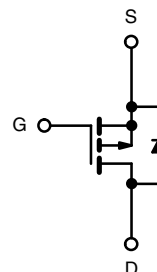
- Halogen-free according to IEC 61249-2-21 Definition
- TrenchFET[®] Power MOSFET
- Ultra Small MICRO FOOT[®] ChipScale Packaging Reduces Footprint Area, Profile (0.62 mm) and On-Resistance Per Footprint Area
- Compliant to RoHS Directive 2002/95/EC



RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- PA Switch
- Battery Switch
- Load Switch



P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V _{DS}	- 12	V
Gate-Source Voltage	V _{GS}	± 8	
Continuous Drain Current (T _J = 150 °C)	I _D	T _C = 25 °C - 14.5	A
		T _C = 70 °C - 11.7	
		T _A = 25 °C - 9.7 ^{b, c}	
		T _A = 70 °C - 7.7 ^{b, c}	
Pulsed Drain Current	I _{DM}	- 20	A
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C - 5.7	
		T _A = 25 °C - 2.5 ^{b, c}	
Maximum Power Dissipation	P _D	T _C = 25 °C 6.57	W
		T _C = 70 °C 4.2	
		T _A = 25 °C 2.9 ^{b, c}	
		T _A = 70 °C 1.86 ^{b, c}	
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to 150	°C
Package Reflow Conditions ^d	IR/Convection	260	

Notes:

a. Based on T_C = 25 °C.

b. Surface mounted on 1" x 1" FR4 board.

c. t = 10 s.

d. Refer to IPC/JEDEC (J-STD-020), no manual or hand soldering.

e. In this document, any reference to the Case represents the body of the MICRO FOOT device and Foot is the bump.

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{a, b}	R_{thJA}	35	45	°C/W
Maximum Junction-to-Foot (Drain)	Steady State R_{thJF}	16	20	

Notes:

a. Surface mounted on 1" x 1" FR4 board.

b. Maximum under steady state conditions is 72 °C/W.

SPECIFICATIONS ($T_J = 25\text{ °C}$, unless otherwise noted)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}$, $I_D = -250\text{ }\mu\text{A}$	- 12			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = -250\text{ }\mu\text{A}$		- 13.3		mV/°C
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			2.4		
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = -250\text{ }\mu\text{A}$	- 0.35		- 0.9	V
Gate-Source Leakage	I_{GSS}	$V_{DS} = 0\text{ V}$, $V_{GS} = 5\text{ V}$			- 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -12\text{ V}$, $V_{GS} = 0\text{ V}$			- 1	μA
		$V_{DS} = -12\text{ V}$, $V_{GS} = 0\text{ V}$, $T_J = 70\text{ °C}$			- 10	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \leq 5\text{ V}$, $V_{GS} = -4.5\text{ V}$	- 20			A
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = -4.5\text{ V}$, $I_D = -1\text{ A}$		0.0174	0.021	Ω
		$V_{GS} = -2.5\text{ V}$, $I_D = -1\text{ A}$		0.0214	0.026	
		$V_{GS} = -1.8\text{ V}$, $I_D = -1\text{ A}$		0.0270	0.033	
Forward Transconductance ^a	g_{fs}	$V_{DS} = -4\text{ V}$, $I_D = -1\text{ A}$		8.3		S
Dynamic^b						
Input Capacitance	C_{iss}	$V_{DS} = -6\text{ V}$, $V_{GS} = 0\text{ V}$, $f = 1\text{ MHz}$		2220		pF
Output Capacitance	C_{oss}			865		
Reverse Transfer Capacitance	C_{rss}			555		
Total Gate Charge	Q_g	$V_{DS} = -6\text{ V}$, $V_{GS} = -5\text{ V}$, $I_D = -1\text{ A}$		38	57	nC
Gate-Source Charge	Q_{gs}			35	53	
Gate-Drain Charge	Q_{gd}			7.3		
Gate Resistance	R_g			5.9		
Gate Resistance	R_g	$V_{GS} = -0.1\text{ V}$, $f = 1\text{ MHz}$		28		Ω
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -6\text{ V}$, $R_L = 4\text{ }\Omega$ $I_D \cong -1\text{ A}$, $V_{GEN} = -4.5\text{ V}$, $R_g = 6\text{ }\Omega$		14	21	ns
Rise Time	t_r			25	40	
Turn-Off Delay Time	$t_{d(off)}$			380	570	
Fall Time	t_f			240	360	

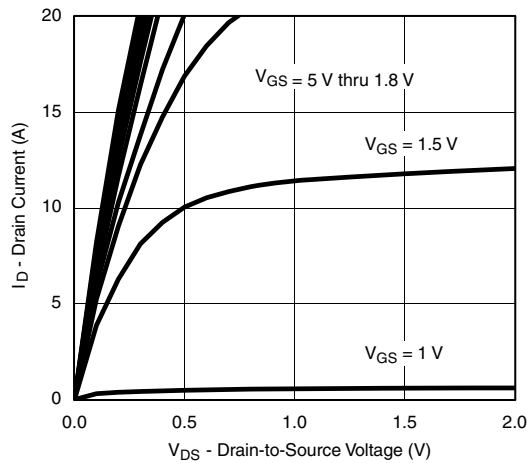
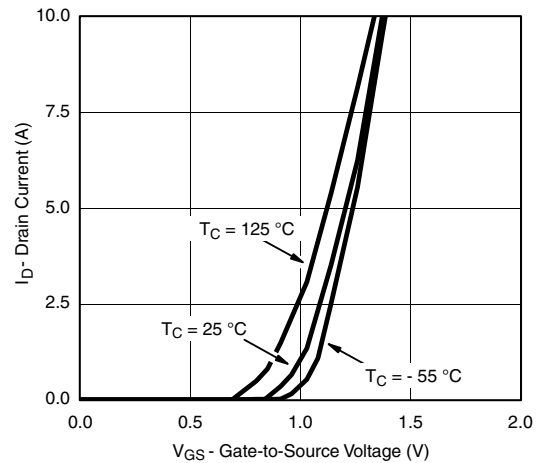
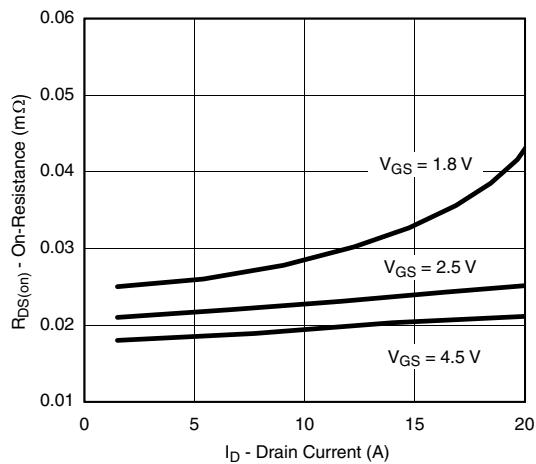
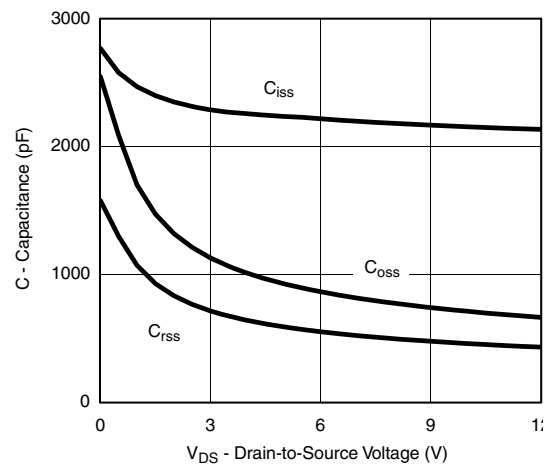
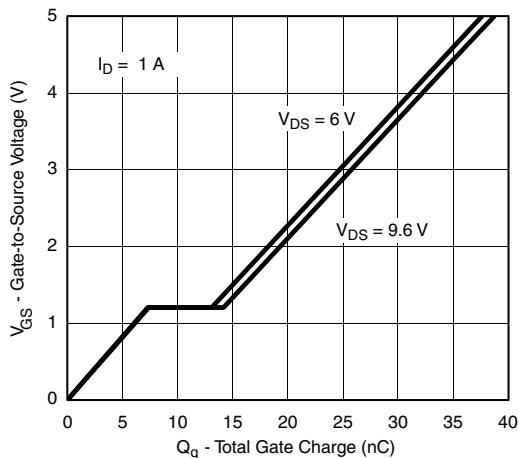
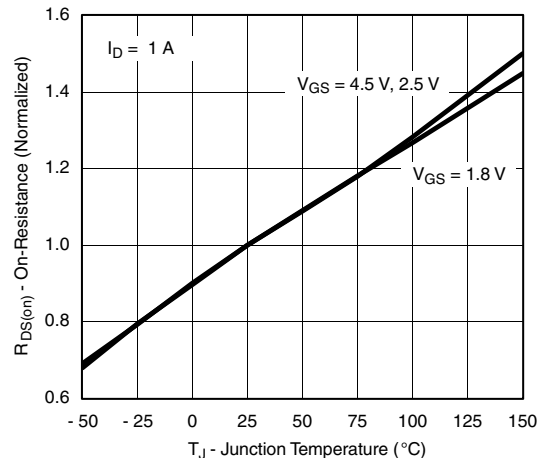


SPECIFICATIONS $T_J = 25\text{ }^{\circ}\text{C}$, unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	$T_C = 25\text{ }^{\circ}\text{C}$			- 5.5	A
Pulse Diode Forward Current	I_{SM}				- 20	
Body Diode Voltage	V_{SD}	$I_S = -1\text{ A}$, $V_{GS} = 0\text{ V}$		- 0.65	- 1.2	V
Body Diode Reverse Recovery Time	t_{rr}	$I_F = -1\text{ A}$, $dI/dt = 100\text{ A}/\mu\text{s}$, $T_J = 25\text{ }^{\circ}\text{C}$		311	467	ns
Body Diode Reverse Recovery Charge	Q_{rr}			1.136	1.705	μC
Reverse Recovery Fall Time	t_a			116		ns
Reverse Recovery Rise Time	t_b			195		

Notes:

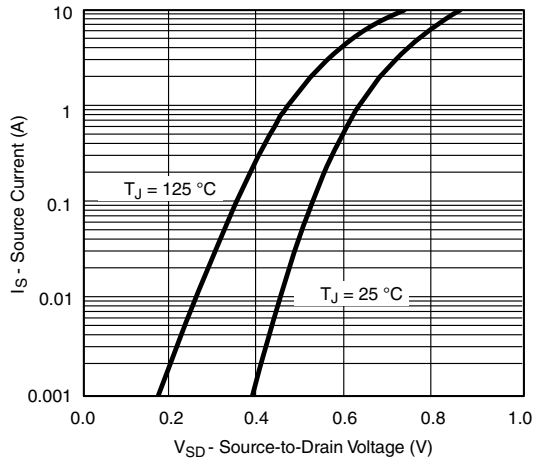
- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

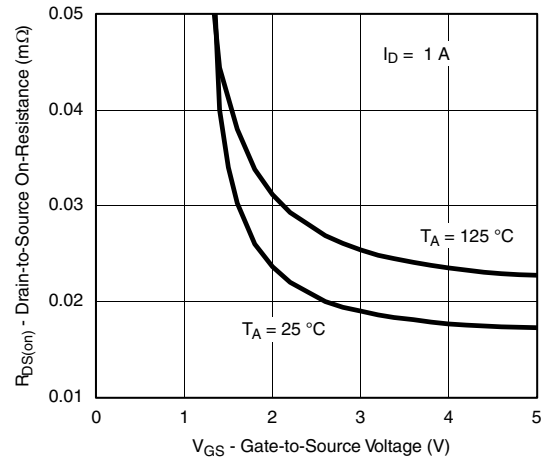
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)**Output Characteristics****Transfer Characteristics****On-Resistance vs. Drain Current and Gate Voltage****Capacitance****Gate Charge****On-Resistance vs. Junction Temperature**



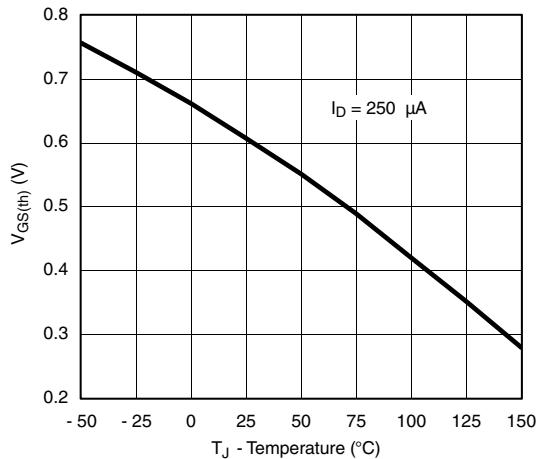
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



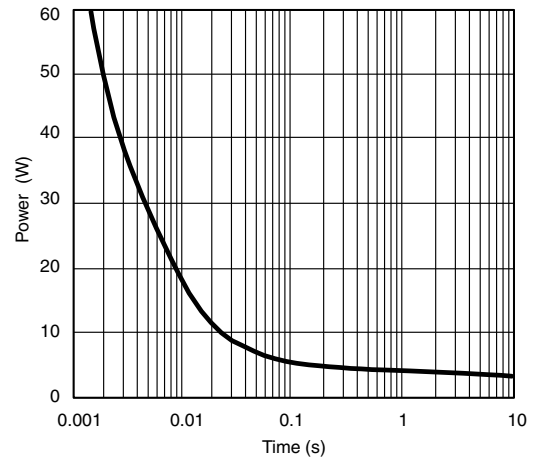
Source-Drain Diode Forward Voltage



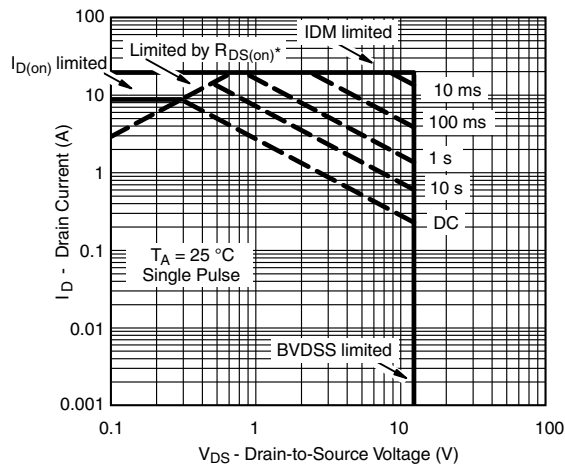
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage

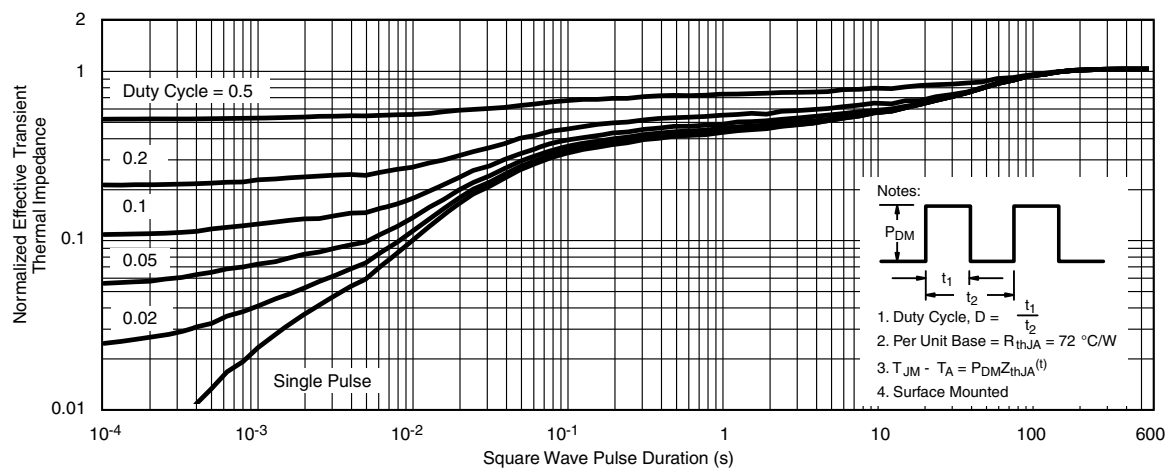
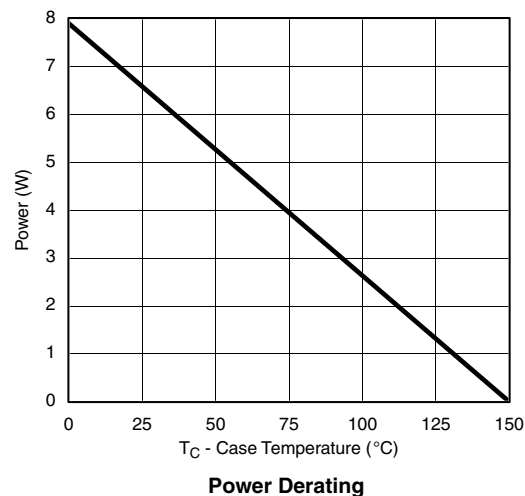
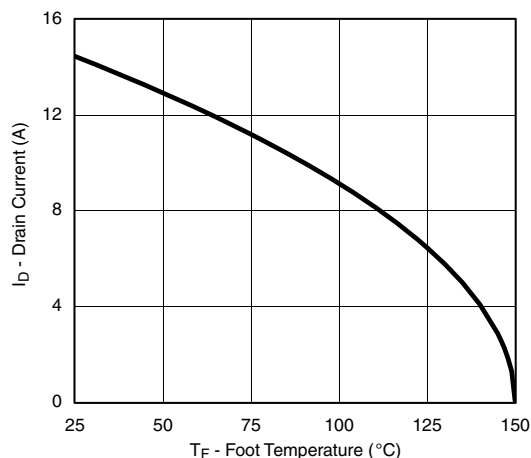
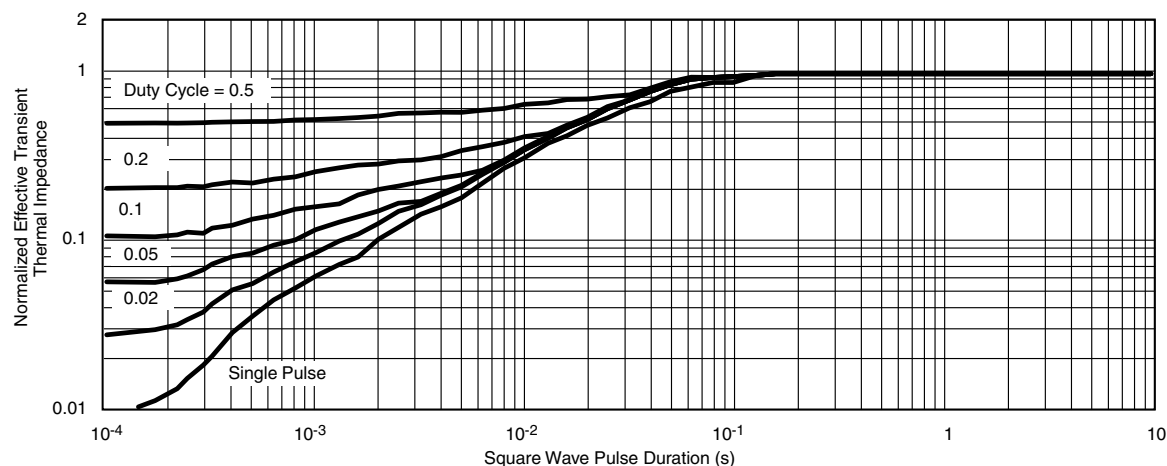


Single Pulse Power, Junction-to-Ambient



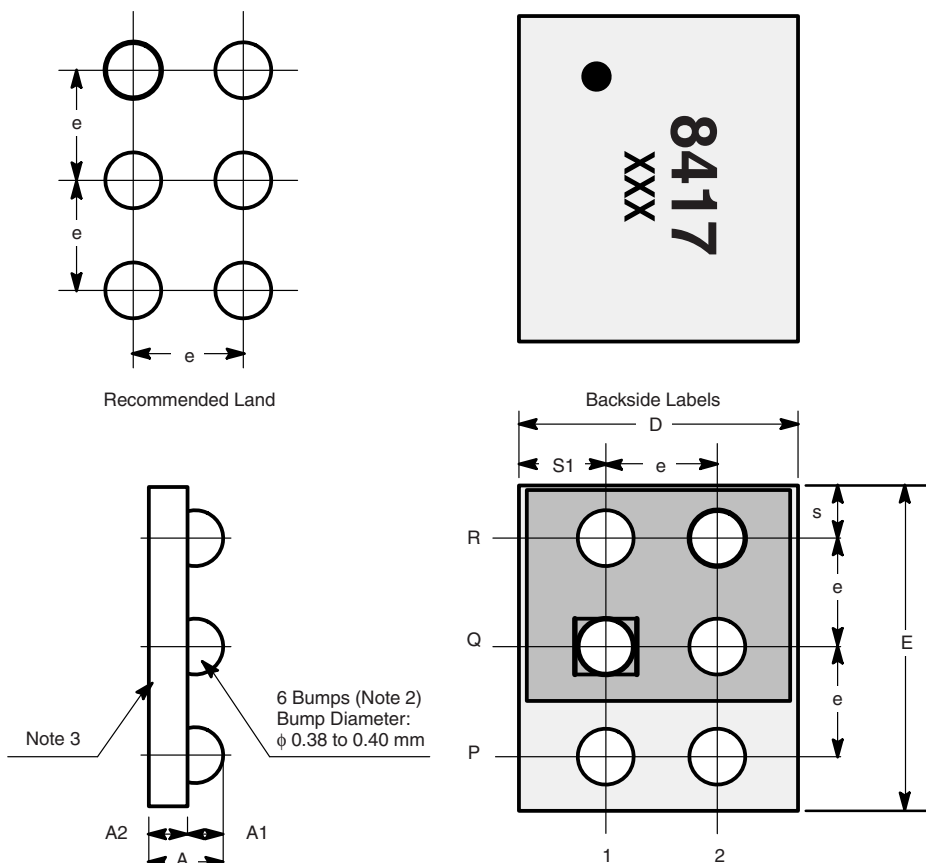
* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area, Junction-to-Ambient

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)**Normalized Thermal Transient Impedance, Junction-to-Ambient****Normalized Thermal Transient Impedance, Junction-to-Foot**

PACKAGE OUTLINE

MICRO FOOT: 6-BUMP (2.4 mm x 2 mm, 0.8 mm PITCH)



Notes (Unless Otherwise Specified):

1. All dimensions are in millimeters.
2. Six (6) solder bumps are 95.5Sn/3.8Ag/0.7Cu with diameter ϕ 0.38 mm to 0.40 mm.
3. Backside surface is coated with a Ti/Ni/Ag layer.
4. Non-solder mask defined copper landing pad.
5. The flat side of wafers is oriented at the bottom.
6. • is location of Pin 1P.

Dim.	Millimeters ^a		Inches	
	Min.	Max.	Min.	Max.
A	0.600	0.650	0.0236	0.0256
A ₁	0.260	0.290	0.0102	0.0114
A ₂	0.340	0.360	0.0134	0.0142
b	0.370	0.410	0.0146	0.0161
D	1.920	2.000	0.0756	0.0787
E	2.320	2.400	0.0913	0.0945
e	0.750	0.850	0.0295	0.0335
S	0.370	0.400	0.0150	0.0157
S1	0.580	0.600	0.0228	0.0236

Notes:

a. Use millimeters as the primary measurement.

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?73531.

PAD DISTRIBUTION TABLE			
	P	Q	R
1	Drain	Gate	Source
2	Drain	Source	Source



Disclaimer

ALL PRODUCT, PRODUCT SPECIFICATIONS AND DATA ARE SUBJECT TO CHANGE WITHOUT NOTICE TO IMPROVE RELIABILITY, FUNCTION OR DESIGN OR OTHERWISE.

Vishay Intertechnology, Inc., its affiliates, agents, and employees, and all persons acting on its or their behalf (collectively, "Vishay"), disclaim any and all liability for any errors, inaccuracies or incompleteness contained in any datasheet or in any other disclosure relating to any product.

Vishay makes no warranty, representation or guarantee regarding the suitability of the products for any particular purpose or the continuing production of any product. To the maximum extent permitted by applicable law, Vishay disclaims (i) any and all liability arising out of the application or use of any product, (ii) any and all liability, including without limitation special, consequential or incidental damages, and (iii) any and all implied warranties, including warranties of fitness for particular purpose, non-infringement and merchantability.

Statements regarding the suitability of products for certain types of applications are based on Vishay's knowledge of typical requirements that are often placed on Vishay products in generic applications. Such statements are not binding statements about the suitability of products for a particular application. It is the customer's responsibility to validate that a particular product with the properties described in the product specification is suitable for use in a particular application. Parameters provided in datasheets and / or specifications may vary in different applications and performance may vary over time. All operating parameters, including typical parameters, must be validated for each customer application by the customer's technical experts. Product specifications do not expand or otherwise modify Vishay's terms and conditions of purchase, including but not limited to the warranty expressed therein.

Except as expressly indicated in writing, Vishay products are not designed for use in medical, life-saving, or life-sustaining applications or for any other application in which the failure of the Vishay product could result in personal injury or death. Customers using or selling Vishay products not expressly indicated for use in such applications do so at their own risk. Please contact authorized Vishay personnel to obtain written terms and conditions regarding products designed for such applications.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted by this document or by any conduct of Vishay. Product names and markings noted herein may be trademarks of their respective owners.