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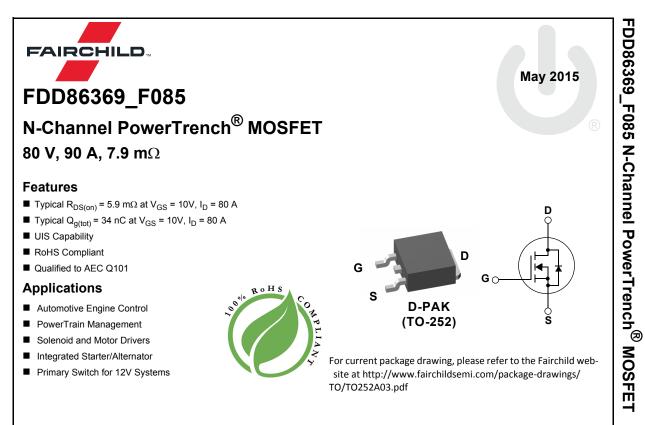


ON Semiconductor®

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Please note: As part of the Fairchild Semiconductor integration, some of the Fairchild orderable part numbers will need to change in order to meet ON Semiconductor's system requirements. Since the ON Semiconductor product management systems do not have the ability to manage part nomenclature that utilizes an underscore (_), the underscore (_) in the Fairchild part numbers will be changed to a dash (-). This document may contain device numbers with an underscore (_). Please check the ON Semiconductor website to verify the updated device numbers. The most current and up-to-date ordering information can be found at www.onsemi.com. Please email any questions regarding the system integration to Fairchild_questions@onsemi.com.

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MOSFET Maximum Ratings T_J = 25°C unless otherwise noted.

Symbol	Parameter		Ratings	Units
V _{DSS}	Drain-to-Source Voltage		80	V
V _{GS}	Gate-to-Source Voltage		±20	V
	Drain Current - Continuous (V _{GS} =10) (Note 1)	T _C =25°C	90	•
D	Pulsed Drain Current	T _C = 25°C	See Figure 4	— A
E _{AS}	Single Pulse Avalanche Energy	(Note 2)	29	mJ
D	Power Dissipation		150	W
P _D	Derate Above 25°C		1.0	W/ ^o C
T _J , T _{STG}	Operating and Storage Temperature		-55 to + 175	°C
R _{0JC}	Thermal Resistance, Junction to Case		1.0	°C/W
R _{0JA}	Maximum Thermal Resistance, Junction to Ambient	(Note 3)	52	°C/W

Notes:

1: Current is limited by bondwire configuration.

2: Starting $T_J = 25^{\circ}$ C, $L = 14\mu$ H, $I_{AS} = 64A$, $V_{DD} = 80V$ during inductor charging and $V_{DD} = 0V$ during time in avalanche.

3: R_{0JA} is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. R_{0JC} is guaranteed by design, while R_{0JA} is determined by the board design. The maximum rating presented here is based on mounting on a 1 in² pad of 2oz copper.

Package Marking and Ordering Information

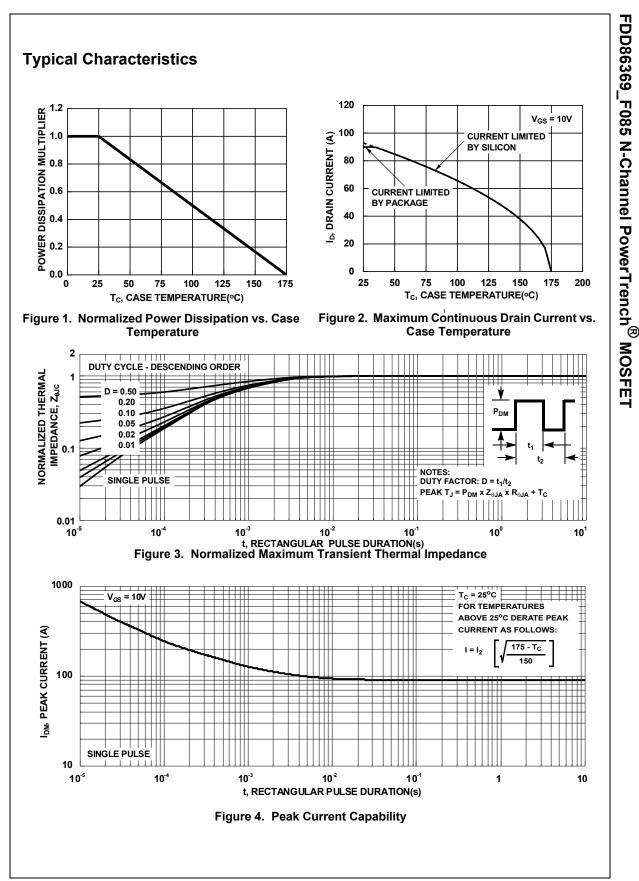
Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDD86369	FDD86369_F085	D-PAK(TO-252)	13"	16mm	2500units

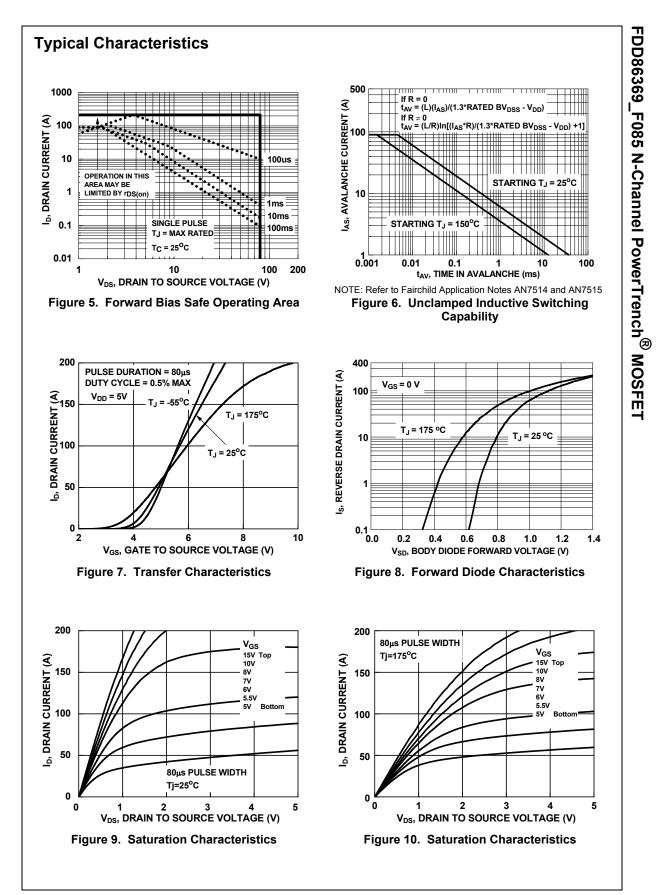
Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Units
Off Cha	racteristics				1	
B _{VDSS}	Drain-to-Source Breakdown Voltage	I _D = 250μA, V _{GS} = 0V	80	-	-	V
I _{DSS}	Drain-to-Source Leakage Current	$V_{DS}=80V, T_{J}=25^{\circ}C$ $V_{GS}=0V T_{J}=175^{\circ}C$ (Note 4)	-	-	1	μA mA
I _{GSS}	Gate-to-Source Leakage Current	$V_{GS} = \pm 20V$	-	-	±100	nA
On Cha	racteristics					
V _{GS(th)}	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_{D} = 250 \mu A$		2.7	4.0	V
_	Drain to Source On Resistance	$I_D = 80A,$ $T_J = 25^{\circ}C$ $V_{GS} = 10V$ $T_J = 175^{\circ}C$ (Note 4	-	5.9	7.9	mΩ
R _{DS(on)}		V_{GS} = 10V T_{J} = 175°C (Note 4) -	13.0	17.4	mΩ
Dynami C _{iss}	c Characteristics		_	2530	-	pF
C _{oss}	Output Capacitance	$-V_{DS} = 40V, V_{GS} = 0V,$	-	430	-	pF
C _{rss}	Reverse Transfer Capacitance	f = 1MHz		16	-	pF
R _q	Gate Resistance	V _{GS} = 0.5V, f = 1MHz	-	2.2	-	Ω
Q _{g(ToT)}	Total Gate Charge	$V_{GS} = 0$ to 10V $V_{DD} = 64V$	-	36	54	nC
Q _{g(th)}	Threshold Gate Charge	$V_{GS} = 0 \text{ to } 2V$ $I_D = 80A$	-	4.6	-	nC
Q _{gs}	Gate-to-Source Gate Charge	, ,	-	13	-	nC
Q _{gd}	Gate-to-Drain "Miller" Charge	_	-	8.5	-	nC
Switchi	ng Characteristics					
t _{on}	Turn-On Time		-	-	70	ns
t _{d(on)}	Turn-On Delay		-	13	-	ns
t _r	Rise Time	$V_{DD} = 40V, I_D = 80A,$	-	34	-	ns
t _{d(off)}	Turn-Off Delay	V_{GS} = 10V, R_{GEN} = 6 Ω	-	22	-	ns
t _f	Fall Time	_	-	9	-	ns
t _{off}	Turn-Off Time		-	-	46	ns
Drain-S	ource Diode Characteristics					
V	Source to Drain Diada Visitara	I _{SD} =80A, V _{GS} = 0V	-	-	1.25	V
V _{SD}	Source-to-Drain Diode Voltage	$I_{SD} = 40A, V_{GS} = 0V$	-	-	1.2	V
t _{rr}	Reverse-Recovery Time		-	49	64	ns
Q _{rr}	Reverse-Recovery Charge	— I _F = 80A, dI _{SD} /dt = 100A/μs		40	53	nC

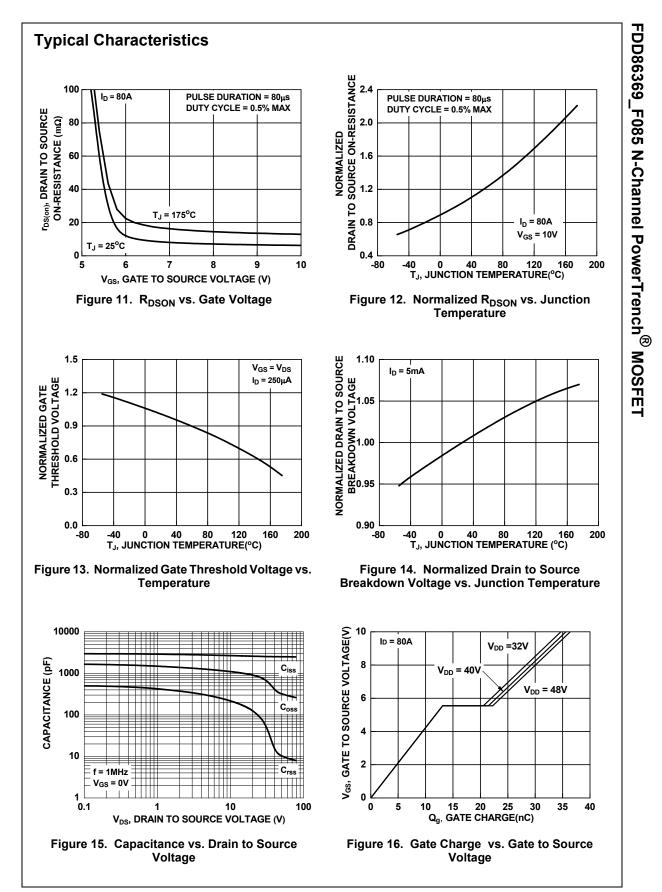
FDD86369_F085 N-Channel PowerTrench[®] MOSFET

Note:

4: The maximum value is specified by design at T_J = 175°C. Product is not tested to this condition in production.









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