Timing Solutions

PRODUCT SELECTOR GUIDE

Timing
The industry's broadest portfolio of oscillators, clock buffers, clock generators, PCI Express (PCIe) clocks, jitter attenuators and SyncE/IEEE 1588 clocks.

Timing Solutions

Silicon Labs offers a broad portfolio of timing products that enable hardware designers to simplify clock generation, clock distribution, jitter attenuation and network synchronization. These products combine best-in-class jitter performance and frequency flexibility, enabling customers to easily architect optimized clock tree solutions. Custom samples are available in 1-2 weeks, easing design and reducing time-to-market.

Products:

Oscillators

- Any frequency up to 3.0 GHz
- Ultra-low jitter: 80 fs RMS
- Short lead times: 1-2 weeks (samples)

Clock Buffers

- Integrated format/level translation
- Ultra-low additive jitter: 50 fs RMS
- PCI Express Gen 1/2/3/4 compliant

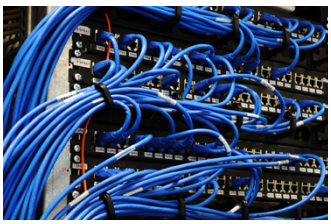
Clock Generators

- Any-frequency, any-output
- Ultra-low jitter: 70 fs RMS
- Clock tree on a chip replaces clocks and XOs

Jitter Attenuating Clocks/ Network Synchronizers

- Any frequency, any output
- Ultra-low jitter: 70 fs RMS
- Clock tree on a chip replaces clocks, XOs, VCXOs

Applications:



- Enterprise routers
- Cable/DSL
- PON

- Base stations
- Small cells/DAS
- Backhaul/Fronthaul

- Switches/servers
- Storage/security
- Search acceleration
- Machine learning

- Audio/video
- Test/measurement
- Mil/aero

- Optical Transport (OTN)
- WDM
- Carrier Ethernet

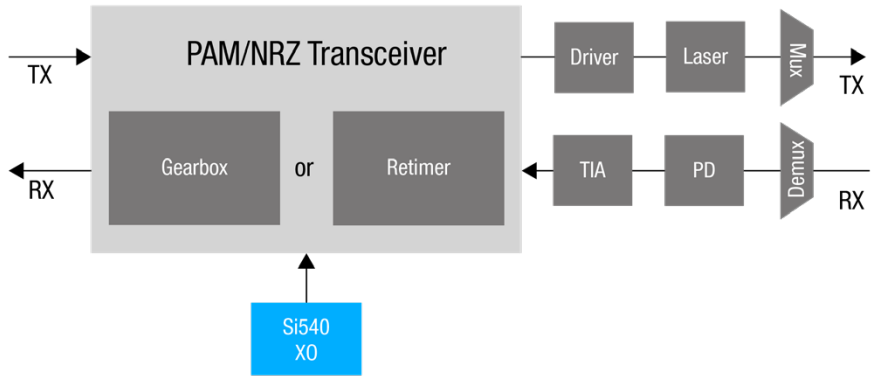
Crystal Oscillators (XO)

Silicon Labs offers the industry's broadest portfolio of high performance, low jitter XOs and VCXOs. Silicon Labs' new Si54x and Si56x Ultra Series™ family of high performance XOs delivers best-in-class jitter performance and frequency flexibility. All devices are highly customizable, with samples of any XO available with 1-2 week lead times.

PORTFOLIO KEY FEATURES

- Industry's lowest jitter any frequency XOs
- Jitter as low as 80 fs RMS typ
- Any frequency up to 3.0 GHz
- Single, dual, quad and I2C prog. options
- LVPECL, LVDS, HCSL, CML, LVCMOS
- Superior stability vs. SAW oscillators
- Best-in-class power supply noise rejection
- Single device supports 1.8 – 3.3 V operation
- -40° to +85° C operation
- Samples in 1-2 weeks

EXAMPLE APPLICATION: 100G/200G OPTICAL MODULE



FEATURED PRODUCTS

PERFORMANCE OPTION	PART NUMBER	NUMBER OF FREQUENCIES	FREQUENCY RANGE	TYP JITTER (fs RMS)	TOTAL STABILITY (±PPM)	LVPECL	LVDS	HCSL	CML	LVCMOS	DUAL LVCMOS	VOLTAGE (V)	PACKAGE SIZE (MM)
ULTRA LOW JITTER	Si545	SINGLE	200 kHz to 1.5 GHz	80	25, 50	✓	✓	✓	✓	✓	✓	1.8 - 3.3	5 x 7
	Si546	DUAL											3.2 x 5
	Si547	QUAD											
	Si549	ANY (I2C)											
	Si540	SINGLE	200 kHz to 1.5 GHz	125	25, 50	✓	✓	✓	✓	✓	✓	1.8 - 3.3	5 x 7
	Si541	DUAL											3.2 x 5
	Si542	QUAD											
	Si544	ANY (I2C)											
	Si560	SINGLE	200 kHz to 3.0 GHz	90	50	✓	✓	✓	✓	✓	✓	1.8 - 3.3	5 x 7
	Si561	DUAL											3.2 x 5
	Si562	QUAD											
	Si564	ANY (I2C)											
LOW JITTER	Si530/1	SINGLE	10 MHz to 1.4 GHz	300	31.5, 61.5	✓	✓		✓	✓		1.8, 2.5, 3.3	5 x 7
	Si532/3	DUAL											
	Si534	QUAD											
	Si570	ANY (I2C)											
GENERAL PURPOSE	Si590/1	SINGLE	10 MHz to 810 MHz	500	30, 50, 100	✓	✓			✓		1.8, 2.5, 3.3	5 x 7
	Si598	ANY (I2C)											3.2 x 5
	Si510/1	SINGLE	100 kHz to 250 MHz	800	30, 50, 100	✓	✓	✓		✓	✓	1.8, 2.5, 3.3	5 x 7
	Si512/3	DUAL											3.2 x 5
	Si514	ANY (I2C)											2.5 x 3.2

XO | XO Software Tools | XO Development Tools | Reference Designs

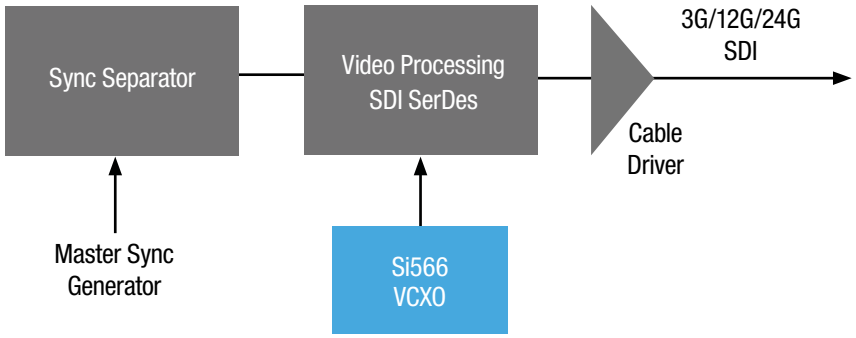
Voltage-Controlled Crystal Oscillators (VCXO)

Silicon Labs offers the industry's broadest portfolio of high performance, low jitter XOs and VCXOs. Silicon Labs' new Si56x Ultra Series™ family of high performance VCXOs deliver exceptional jitter performance and best-in-class control voltage linearity and power supply noise rejection. All devices are highly customizable, with samples of any VCXO available with 1-2 week lead times.

PORTFOLIO KEY FEATURES

- Jitter: 100 fs RMS typ (12 kHz – 20 MHz)
- Any frequency up to 3.0 GHz
- Single, dual, quad and I2C prog. options
- LVPECL, LVDS, HCSL, CML, LVCMOS
- Superior linearity vs. traditional VCSO/VCXOs
- Best-in-class power supply noise rejection
- 1.8, 2.5 or 3.3 V
- 5x7 mm, 3.2x5 mm
- -40° to +85° C operation
- Samples in 1–2 weeks

EXAMPLE APPLICATION: VIDEO FORMAT CONVERTER



FEATURED VOLTAGE-CONTROLLED CRYSTAL OSCILLATORS (VCXO)

PERFORMANCE OPTION	PART NUMBER	NUMBER OF FREQUENCIES	FREQUENCY RANGE	TYP JITTER (fs RMS)	MIN APR (±PPM)	LVPECL	LVDS	HCSL	CML	LVCMOS	DUAL LVCMOS	VOLTAGE (V)	PACKAGE (MM)
ULTRA-LOW JITTER	Si565	SINGLE	200 kHz to 3.0 GHz	100	20 - 190	✓	✓	✓	✓	✓	✓	1.8 - 3.3	5 x 7
	Si566	DUAL											3.2 x 5
	Si567	QUAD											
	Si569	ANY (I2C)											
LOW JITTER	Si550	SINGLE	10 MHz to 1.4 GHz	500	12 - 375	✓	✓		✓	✓		1.8, 2.5, 3.3	5 x 7
	Si552	DUAL											
	Si554	QUAD											
	Si571	ANY (I2C)											
GENERAL PURPOSE	Si595	SINGLE	10 MHz to 810 MHz	700	10 - 370	✓	✓		✓	✓		1.8, 2.5, 3.3	5 x 7
	Si596	DUAL											3.2 x 5
	Si597	QUAD											
	Si598	ANY (I2C)											
	Si515	SINGLE	100 kHz to 250 MHz	1000	30, 50, 100	✓	✓	✓		✓	✓	1.8, 2.5, 3.3	5 x 7
	Si516	DUAL											3.2 x5
													2.5 x 3.2

VCXO | VCXO Software Tools | VCXO Development Tools | Reference Designs

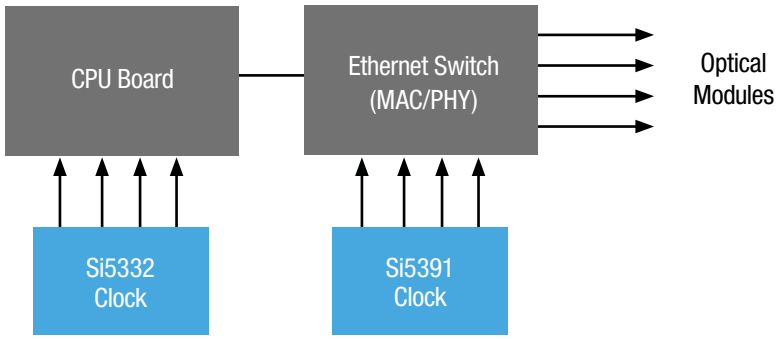
Clock Generators

Silicon Labs offers the industry's lowest jitter, most frequency flexible, most highly integrated clock generators. Leveraging Silicon Labs' proven MultiSynth technology, a single clock generator can replace an entire clock tree of multiple oscillators, buffers, clock generators, and muxes, simplifying design and accelerating time to market. Silicon Labs' comprehensive clock generator portfolio offers optimized solutions for communications, data center, industrial and consumer applications.

PORTFOLIO KEY FEATURES

- Ultra-low jitter as low as 69 fs RMS
- Generate any combination of frequencies
- Lowest jitter fractional clock synthesis
- Programmable format per output
- LVPECL, LVDS, HCSL, CML, LVCMOS
- Programmable VDDO per output
- Best-in-class power supply noise rejection
- PCIe Gen 1/2/3/4 compliant
- Custom samples in 2 weeks
- ClockBuilder Pro support

APPLICATION EXAMPLE: DATA CENTER ETHERNET SWITCH



FEATURED CLOCK GENERATORS

PERFORMANCE OPTION	PART NUMBER	CLOCK INPUTS	CLOCK OUTPUTS	MAX OUTPUT FREQUENCY	TYP JITTER (fs RMS)	LVPECL	LVDS	HCSL	CML	LVCMOS	VOLTAGE (V)	PACKAGE
ULTRA-LOW JITTER	Si5391	4	12	1028 MHz	69	✓	✓	✓	✓	✓	1.8, 3.3	QFN64
	Si5341	4	10	1028 MHz	100	✓	✓	✓	✓	✓	1.8, 3.3	QFN64
	Si5340	4	4	1028 MHz	100	✓	✓	✓	✓	✓	1.8, 3.3	QFN64
LOW JITTER	Si5332	3	6, 8, 12	333.33 MHz	190	✓	✓	✓	✓	✓	1.8, 2.5, 3.3	QFN48 QFN40 QFN32
GENERAL PURPOSE	Si5338/35/34	2	4	710 MHz	700	✓	✓	✓		✓	1.8, 2.5, 3.3	QFN24
PCIE CLOCK GENERATORS	Si52202/04/08/12	1	2, 4, 8, 12	133 MHz	240			✓			1.5, 1.8	QFN48 QFN32 QFN24 QFN20
	Si52142/3/4/6/7	1	2, 4, 5, 6, 9	100 MHz	600			✓			3.3	QFN24 QFN24 QFN24 QFN32 QFN48
	Si52111/2	1	1, 2	100 MHz	600			✓		✓	3.3	TDFN10
CMOS CLOCK GENERATORS	Si5350/1	1	3, 8	200 MHz	-					✓	1.8, 2.5, 3.3	MSOP10 QFN20
	Si51210/1/4/8	1	1, 2, 3	170 MHz	-					✓	1.8, 2.5, 3.3	TDFN6 TDFN8

Clk Gens | Clk Gen Software Tools | Clk Gen Development Tools | Reference Designs

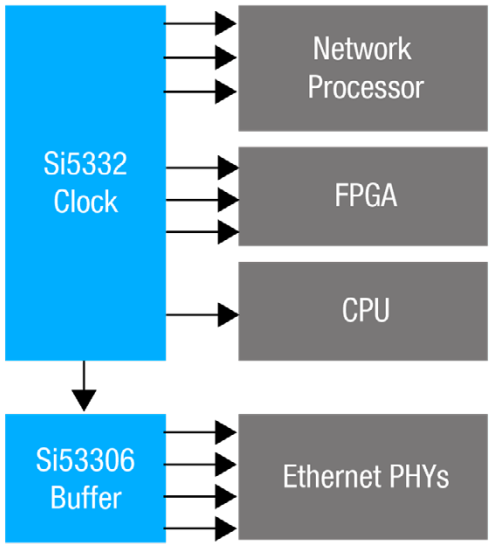
Clock Buffers

Silicon Labs offers a comprehensive portfolio of clock buffers. In addition to universal buffers that support any in/out signal format translation, we offer a wide range of differential and single-ended buffers that provide ultra-low additive jitter and low skew clock distribution. Silicon Labs also offers a broad range of low-power PCIe buffers that integrate all termination components while providing compliance with PCIe Gen 1/2/3/4 standards.

PORTFOLIO KEY FEATURES

- Ultra-low additive jitter as low as 50 fs RMS
- Clock distribution up to 1.25 GHz
- LVPECL, LVDS, HCSL, CML, LVCMOS
- Pin-selectable signal format
- Individual clock output OE control
- Synchronous, glitchless OE control
- Best-in-class power supply noise rejection
- PCIe: push-pull HCSL drivers
- PCIe: integrated termination resistors
- PCIe: Gen 1/2/3/4 compliant
- PCIe: Intel-qualified solutions

APPLICATION EXAMPLE: SWITCH/ROUTER



FEATURED CLOCK BUFFERS

PRODUCT FAMILY	PART NUMBER	CLOCK INPUTS	CLOCK OUTPUTS	MAX OUTPUT FREQUENCY	TYP JITTER (fs RMS)	LVPECL	LVDS	HCSL	CML	LVCMOS	VOLTAGE (V)	PACKAGE
ANY FORMAT	Si5331x	2	6, 10	1250 MHz	50	✓	✓	✓	✓	✓	1.8, 2.5, 3.3	32QFN
	Si5330x	1, 2	2, 4, 6, 10	725 MHz	50	✓	✓	✓	✓	✓	1.8, 2.5, 3.3	16QFN 32QFN 44QFN
LVPECL	Si5332x	1, 2	2, 4, 5, 6, 10	1250 MHz	50	✓					2.5, 3.3	QFN16 QFN24 QFN32
LVDS	Si5334x	2	4, 6, 8, 10	1250 MHz	50		✓				1.8, 2.5, 3.3	QFN16 QFN24 QFN32
LVCMOS	Si5336x	1, 2	8, 12	200 MHz	100					✓	1.8, 2.5, 3.3	16QFN 24QFN 16TSSOP
PCI EXPRESS	Si53204/8/12	1	4, 8, 12	200 MHz	50			✓			1.5, 1.8	QFN64 QFN48 QFN32
	Si5315x	1	2, 4, 6, 9	210 MHz	100			✓			3.3	24QFN 32QFN 48QFN
	Si53102-Ax	1	2	175 MHz	200			✓			2.5, 3.3	8TDFN
PCI EXPRESS ZERO DELAY BUFFERS	Si5311x	1	6, 8, 12, 15, 19	133 MHz	80			✓			3.3	40QFN 48QFN 64QFN 72QFN
TCXO BUFFERS	SL18860/1	1	3	52 MHz	-					✓	1.8	TDFN10

Buffers | PCIe Clock Jitter Tool | Buffer Development Tools | Reference Designs

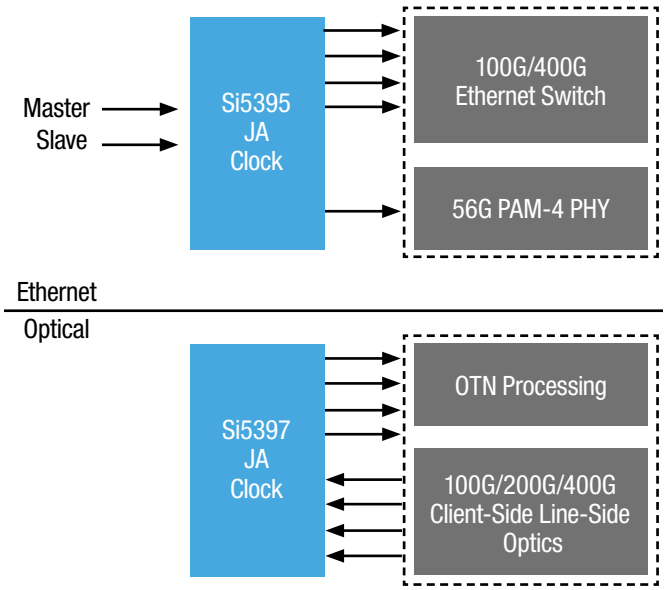
Jitter Attenuating Clocks

Silicon Labs offers the industry's lowest jitter, most frequency flexible, most highly integrated jitter attenuating clock generators. Leveraging Silicon Labs' proven DSPLL and MultiSynth technology, a single jitter attenuating clock can synchronize to a wide range of different clocks, filter jitter, and provide any combination of output frequencies. Silicon Labs offers an extensive range of jitter attenuating clocks to solve the most complex timing challenges in 100G+ packet optical transport and Ethernet designs.

PORTFOLIO KEY FEATURES

- Generate any combination of output frequencies
- Ultra-low jitter as low as 69 fs RMS
- Enhanced hitless switching
- Programmable loop bandwidth down to 0.1 Hz
- Programmable format per output (LVPECL, LVDS, HCSL, CML, LVCMOS)
- Programmable VDDO per output
- Best-in-class power supply noise rejection
- Custom samples in 2 weeks
- ClockBuilder Pro support

APPLICATION EXAMPLE:



FEATURED JITTER ATTENUATING CLOCKS

APPLICATION	PART NUMBER	# DSPLL	# MULTISYNTH	CLOCK INPUTS	CLOCK OUTPUTS	MAX OUTPUT FREQUENCY	TYP JITTER (fs RMS)	LVPECL	LVDS	HCSL	CML	LVCMOS	VOLTAGE (V)	PACKAGE
OPTICAL NETWORKING BROADBAND	Si5395/4/2	1	5/4/2	4	12/4/2	1028 MHz	69	✓	✓	✓	✓	✓	1.8, 3.3	QFN64 / QFN44
	Si5345/4/2	1	5/4/2	4	10/4/2	1028 MHz	90	✓	✓	✓	✓	✓	1.8, 3.3	QFN44 / QFN44
	Si5347	4		4	8/4	720 MHz	90	✓	✓	✓	✓	✓	1.8, 3.3	QFN64
	Si5346	2		4	4	720 MHz	90	✓	✓	✓	✓	✓	1.8, 3.3	QFN44
COHERENT OPTICS	Si5344H/42H	1	2/1	2	4/2	2.75 GHz	50	✓	✓	✓	✓	✓	1.8, 2.5, 3.3	QFN44

Jitter Attenuators | JA Software Tools | JA Development Tools | Reference Designs

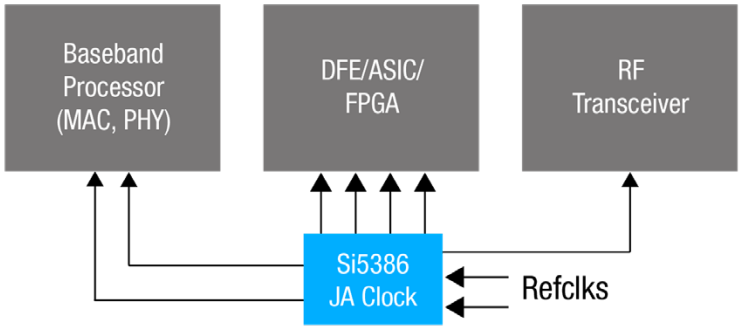
Wireless Clocks

Silicon Labs offers the industry's most highly integrated clocking solutions for radio access networks. Leveraging Silicon Labs' proven DSPLL and MultiSynth technology, a single jitter attenuating clock can synchronize to a wide range of different clocks, filter jitter, and generate LTE, Ethernet and general-purpose clocks from a single device. All PLL components are integrated on-chip, eliminating the need for discrete VCXOs, XOs and loop filters in the design.

PORTFOLIO KEY FEATURES

- Ultra-low phase noise
- Replaces multiple clock IC's and VCXO's
- Generates LTE & Ethernet clocks from single IC
- No external loop filter
- Integrated crystal option
- Noise floor: -165 dBc/Hz
- Best-in-class power supply noise rejection
- Custom samples in 2 weeks
- ClockBuilder Pro support

APPLICATION EXAMPLE: SMALL CELL / DAS



FEATURED WIRELESS CLOCK

APPLICATION	PART NUMBER	# DSPLL	# MULTISYNTH	CLOCK INPUTS	CLOCK OUTPUTS	MAX OUTPUT FREQUENCY	TYP JITTER (fs RMS)	LVPECL	LVDS	HCSL	CML	LVCMOS	VOLTAGE (V)	PACKAGE
C-RAN SMALL CELLS DAS	Si5386	1	5	4	12	2.94912 GHz	80	✓	✓	✓	✓	✓	1.8, 3.3	LGA64 **QFN64**
MACRO RRH	Si5380	1	0	4	12	1.475 GHz	65	✓	✓	✓	✓	✓	1.8, 3.3	QFN64
BACKHAUL FRONTHAUL BBU	Si5381	4	0	4	12	2.94912 GHz	80	✓	✓	✓	✓	✓	1.8, 3.3	LGA64 **QFN64**
	Si5382	2	0	4	12	2.94912 GHz	80	✓	✓	✓	✓	✓	1.8, 3.3	LGA64 **QFN64**

Wireless Clks | Wireless Clk Software Tools | Wireless Clk Dev Tools | Ref Designs

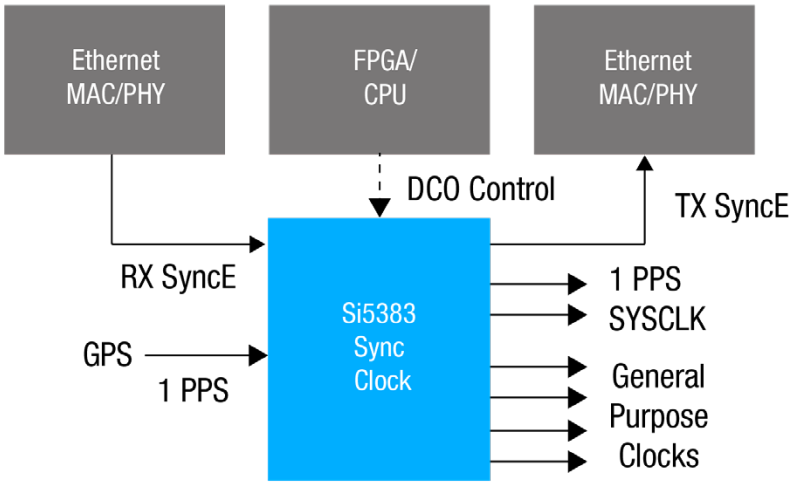
Network Synchronizers (Synchronous Ethernet / IEEE 1588)

Silicon Labs offers standards-compliant synchronization clocks that lead the industry in terms of jitter performance and power consumption. These products combine network synchronization and jitter attenuation functions in a single device, enabling single-IC designs for pizza box Carrier Ethernet switches/routers and BBU control card applications.

PORTFOLIO KEY FEATURES

- Ultra-low jitter as low as 100 fs RMS
- Programmable loop bandwidth down to 1mHz
- Each DSPLL generates any output frequency
- Support for 1PPS/1Hz input and output
- Synchronous, free-run, holdover modes
- Automatic/manual hitless switching
- Pin or SW-controlled 1588 DCO (1 ppt/step)
- Meets G.8262 (SyncE), G.812, G.813
- Suitable for ITU-T G.8273.1 T-GM, G.8273.2 T-BC, T-TSC
- ClockBuilder Pro support

APPLICATION EXAMPLE: TELECOM BOUNDARY CLOCK



FEATURED NETWORK SYNCHRONIZERS

APPLICATION	PART NUMBER	# DSPLL	GPS SYNC (1 PPS INPUT)	MIN LOOP BANDWIDTH	CLOCK INPUTS	CLOCK OUTPUTS	MAX OUTPUT FREQUENCY	TYP JITTER (fs RMS)	LVPECL	LVDS	HCSL	CML	LVCMOS	VOLTAGE (V)	PACKAGE
OPTICAL NETWORKING BROADBAND WIRELESS	Si5383	3	✓	1 mHz	5	7	718.5 MHz	150	✓	✓	✓	✓	✓	1.8, 3.3	LGA56
	Si5384	1	✓	1 mHz	5	7			✓	✓	✓	✓	✓		LGA56
	Si5348	3		1 mHz	5	7			✓	✓	✓	✓	✓		QFN64

Net Sync | Net Sync Software Tools | Net Sync Dev Tools | Reference Designs

Smart. Connected. Energy-Friendly.