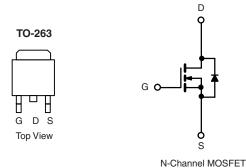


Vishay Siliconix

Automotive N-Channel 150 V (D-S) 175 °C MOSFET

PRODUCT SUMMARY				
V _{DS} (V)	150			
$R_{DS(on)}(\Omega)$ at $V_{GS} = 10 \text{ V}$	0.038			
$R_{DS(on)}(\Omega)$ at $V_{GS} = 6 \text{ V}$	0.040			
I _D (A)	40			
Configuration	Single			



FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET® Power MOSFET
- Package with Low Thermal Resistance
- AEC-Q101 Qualifiedd
- 100 % R_a and UIS Tested
- Compliant to RoHS Directive 2002/95/EC



FREE

ORDERING INFORMATION	
Package	TO-263
Lead (Pb)-free and Halogen-free	SQM40N15-38-GE3

ABSOLUTE MAXIMUM RATINGS (T _C = 25 °C, unless otherwise noted)					
PARAMETER	SYMBOL	LIMIT	UNIT		
Drain-Source Voltage		V_{DS}	150	.,,	
Gate-Source Voltage	V _{GS}	± 20	V		
Continuous Drain Current	T _C = 25 °C	I _D	40		
Continuous Drain Current	T _C = 125 °C		23	1	
Continuous Source Current (Diode Conduction)a	I _S	100	Α		
Pulsed Drain Current ^b	I _{DM}	80			
Single Pulse Avalanche Current	ingle Pulse Avalanche Current		40		
Single Pulse Avalanche Energy	Single Pulse Avalanche Energy L = 0.1 mH		80	mJ	
Maximum Power Dissipation ^b	T _C = 25 °C	Б	166	W	
Maximum Fower Dissipation	T _C = 125 °C	P_{D}	55	VV	
Operating Junction and Storage Temperature Range		T _J , T _{stg}	- 55 to + 175	°C	

THERMAL RESISTANCE RATINGS					
PARAMETER		SYMBOL	LIMIT	UNIT	
Junction-to-Ambient	PCB Mount ^c	R_{thJA}	40	90 AM	
Junction-to-Case (Drain)	·		0.9	°C/W	

Notes

- a. Package limited.
- b. Pulse test; pulse width \leq 300 μ s, duty cycle \leq 2 %.
- c. When mounted on 1" square PCB (FR-4 material).
- d. Parametric verification ongoing.



www.vishay.com Vishay Siliconix

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static	•	•					
Drain-Source Breakdown Voltage	V _{DS}	$V_{GS} = 0$, $I_D = 250 \mu A$		150		=.	V
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} =	= V _{GS} , I _D = 250 μA	2.5	3.0	3.5	V
Gate-Source Leakage	I _{GSS}	V _{DS} =	$0 \text{ V}, \text{ V}_{GS} = \pm 20 \text{ V}$	-	-	± 100	nA
		$V_{GS} = 0 V$	V _{DS} = 150 V	1.0		1.0	
Zero Gate Voltage Drain Current	I _{DSS}	$V_{GS} = 0 V$	V _{DS} = 150 V, T _J = 125 °C	-	-	50	μΑ
		$V_{GS} = 0 V$	V _{DS} = 150 V, T _J = 175 °C			250	
On-State Drain Current ^a	I _{D(on)}	V _{GS} = 10 V	$V_{DS} \ge 5 V$	50	-		Α
		V _{GS} = 10 V	I _D = 15 A	-	0.027	0.038	
Drain-Source On-State Resistance ^a	В	V _{GS} = 10 V	I _D = 15 A, T _J = 125 °C	-	-	0.078	Ω
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} = 10 V	I _D = 15 A, T _J = 175 °C	-	-	0.105	•
		V _{GS} = 6 V	I _D = 10 A	-	0.030	0.040	
Forward Transconductanceb	9 _{fs}	V _{DS} = 15 V, I _D = 15 A		-	40	-	S
Dynamic ^b							
Input Capacitance	C _{iss}				2710	3390	
Output Capacitance	C _{oss}	$V_{GS} = 0 V$	$V_{DS} = 25 \text{ V}, f = 1 \text{ MHz}$	-	310	390	pF
Reverse Transfer Capacitance	C _{rss}]		-	130	165	
Total Gate Charge ^c	Qg			-	46	70	
Gate-Source Charge ^c	Q _{gs}	V _{GS} = 10 V	$V_{DS} = 75 \text{ V}, I_{D} = 85 \text{ A}$	-	20		nC
Gate-Drain Charge ^c	Q _{gd}]		-	11		
Gate Resistance	R _g		f = 1 MHz		2	3	Ω
Turn-On Delay Time ^c	t _{d(on)}			-	14	21	
Rise Time ^c	t _r	$V_{DD} = 75 \text{ V}, \text{ R}_{L} = 0.88 \Omega$ $I_{D} \cong 85 \text{ A}, \text{ V}_{GEN} = 10 \text{ V}, \text{ R}_{g} = 1 \Omega$		-	17	26	ns ns
Turn-Off Delay Time ^c	t _{d(off)}			-	24	36	
Fall Time ^c	t _f			-	9	14	
Source-Drain Diode Ratings and Char-	acteristics ^b						
Pulsed Current ^a	I _{SM}			-	-	80	Α
Forward Voltage	V_{SD}	$I_F = 85 \text{ A}, V_{GS} = 0$		-	0.95	1.5	V

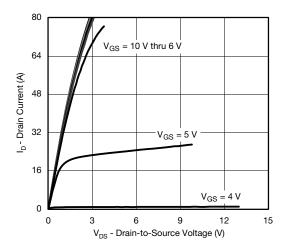
Notes

- a. Pulse test; pulse width $\leq 300~\mu s,$ duty cycle $\leq 2~\%.$
- b. Guaranteed by design, not subject to production testing.
- c. Independent of operating temperature.

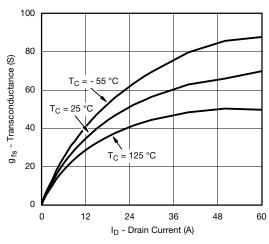
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



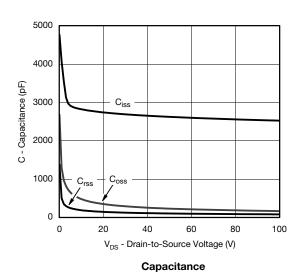
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)

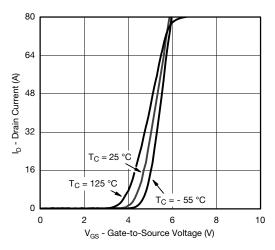


Output Characteristics

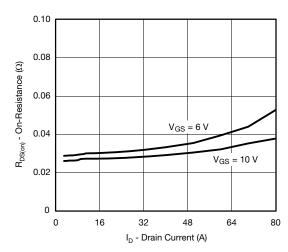


Transconductance

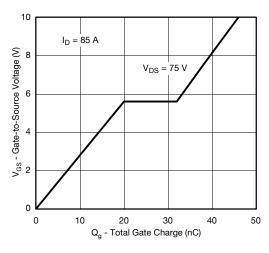




Transfer Characteristics

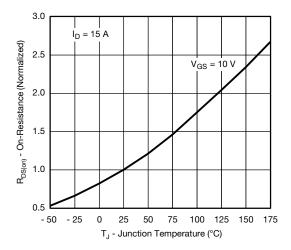


On-Resistance vs. Drain Current

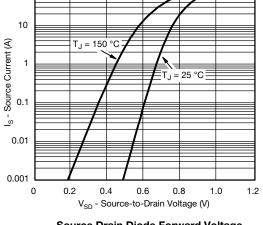




TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)

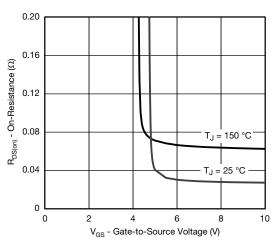


On-Resistance vs. Junction Temperature

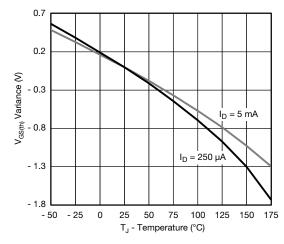


100

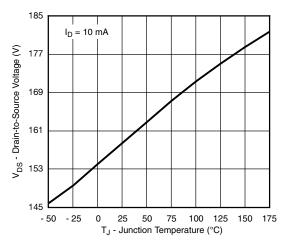
Source Drain Diode Forward Voltage



On-Resistance vs. Gate-to-Source Voltage



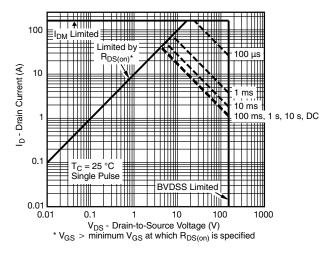
Threshold Voltage



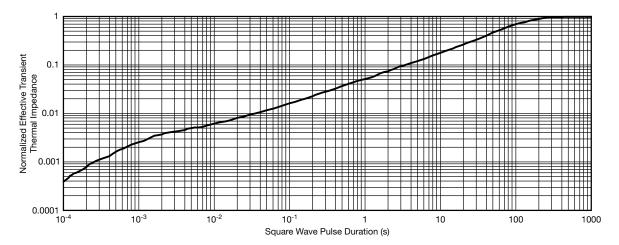
Drain Source Breakdown vs. Junction Temperature



THERMAL RATINGS ($T_A = 25$ °C, unless otherwise noted)



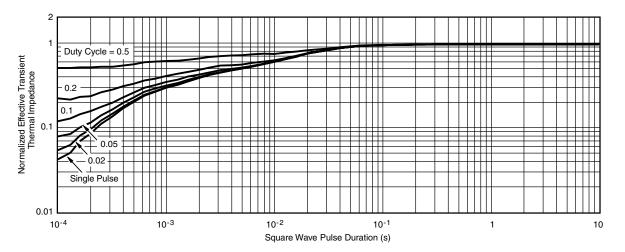
Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Ambient



THERMAL RATINGS (T_A = 25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Case

Note

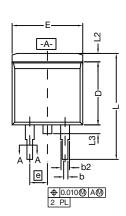
- The characteristics shown in the two graphs
- Normalized Transient Thermal Impedance Junction-to-Ambient (25 °C)
- Normalized Transient Thermal Impedance Junction-to-Case (25 °C)

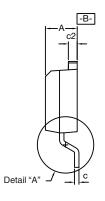
are given for general guidelines only to enable the user to get a "ball park" indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions.

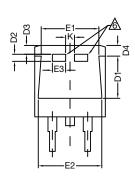
Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg265269.



TO-263 (D²PAK): 3-LEAD

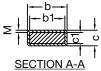








DETAIL A (ROTATED 90°)



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	 . !	1

- 1. Plane B includes maximum features of heat sink tab and plastic.
- 2. No more than 25 % of L1 can fall above seating plane by max. 8 mils.
- 3. Pin-to-pin coplanarity max. 4 mils.
- 4. *: Thin lead is for SUB, SYB. Thick lead is for SUM, SYM, SQM.
- 5. Use inches as the primary measurement.

6. This feature is for thick lead.

		INCHES		MILLIN	METERS
DIM.		MIN.	MAX.	MIN.	MAX.
Α		0.160	0.190	4.064	4.826
	b	0.020	0.039	0.508	0.990
	b1	0.020	0.035	0.508	0.889
	b2	0.045	0.055	1.143	1.397
c*	Thin lead	0.013	0.018	0.330	0.457
C	Thick lead	0.023	0.028	0.584	0.711
c1	Thin lead	0.013	0.017	0.330	0.431
CI	Thick lead	0.023	0.027	0.584	0.685
	c2	0.045	0.055	1.143	1.397
	D	0.340	0.380	8.636	9.652
	D1	0.220	0.240	5.588	6.096
	D2	0.038	0.042	0.965	1.067
	D3	0.045	0.055	1.143	1.397
	D4	0.044	0.052	1.118	1.321
	Е	0.380	0.410	9.652	10.414
	E1	0.245	-	6.223	=
	E2	0.355	0.375	9.017	9.525
	E3	0.072	0.078	1.829	1.981
	е	0.100) BSC	2.54	BSC
	K	0.045	0.055	1.143	1.397
	L	0.575	0.625	14.605	15.875
L1		0.090	0.110	2.286	2.794
	L2	0.040	0.055	1.016	1.397
L3		0.050	0.070	1.270	1.778
	L4	0.010 BSC		0.254 BSC	
	М	-	0.002	-	0.050
ECN: T13-0707-Rev. K, 30-Sep-13					

DWG: 5843





RECOMMENDED MINIMUM PADS FOR D²PAK: 3-Lead



Recommended Minimum Pads Dimensions in Inches/(mm)

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