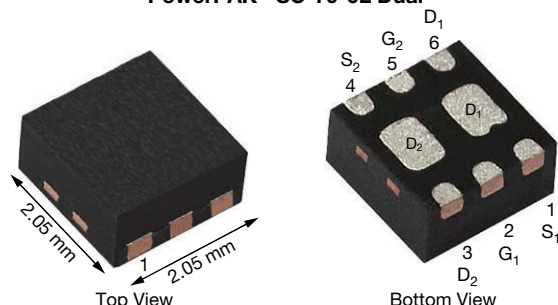


Dual P-Channel 20 V (D-S) MOSFET

PRODUCT SUMMARY

V _{DS} (V)	R _{DS(on)} (Ω)	I _D (A)	Q _g (TYP.)
-20	0.057 at V _{GS} = -4.5 V	-4.5 ^a	4.9 nC
	0.095 at V _{GS} = -2.5 V	-4.5 ^a	

PowerPAK® SC-70-6L Dual

Marking Code: DM

Ordering Information:
[SiA907EDJT-T1-GE3](#) (Lead (Pb)-free and Halogen-free)

[SiA907EDJT-T4-GE3](#) (Lead (Pb)-free and Halogen-free)

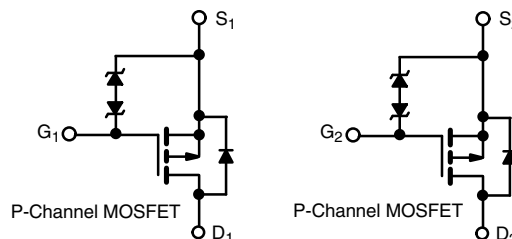
FEATURES

- TrenchFET® power MOSFET
- Thermally enhanced Thin PowerPAK® SC-70 package
 - Small footprint area
 - Low on-resistance
- Typical ESD protection: 1500 V HBM
- High speed switching
- Material categorization: For definitions of compliance please see www.vishay.com/doc?99912


RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- Charger Switch, Load Switch for Portable Devices
- Battery Management



ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V _{DS}	-20	V
Gate-Source Voltage	V _{GS}	± 12	
Continuous Drain Current (T _J = 150 °C)	I _D	T _C = 25 °C	A
		T _C = 70 °C	
		T _A = 25 °C	
		T _A = 70 °C	
Pulsed Drain Current (t = 300 μs)	I _{DM}	-15	A
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C	
		T _A = 25 °C	-1.6 ^{b, c}
Maximum Power Dissipation	P _D	T _C = 25 °C	W
		T _C = 70 °C	
		T _A = 25 °C	
		T _A = 70 °C	
Operating Junction and Storage Temperature Range	T _J , T _{stg}	-55 to 150	°C
Soldering Recommendations (Peak Temperature) ^{d, e}		260	

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	TYPICAL	MAXIMUM	UNIT
Maximum Junction-to-Ambient ^{b, f}	R _{thJA}	52	65	°C/W
Maximum Junction-to-Case (Drain)	R _{thJC}	12.5	16	

Notes

- Package limited.
- Surface mounted on 1" x 1" FR4 board.
- t = 5 s.
- See solder profile (www.vishay.com/doc?73257). The Thin PowerPAK SC-70 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework conditions: Manual soldering with a soldering iron is not recommended for leadless components.
- Maximum under steady state conditions is 110 °C/W.

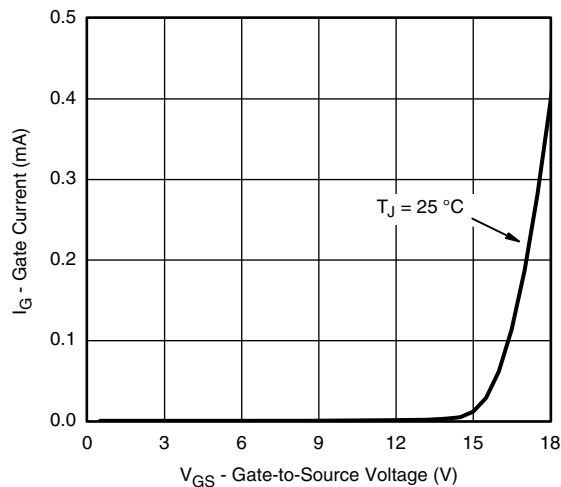
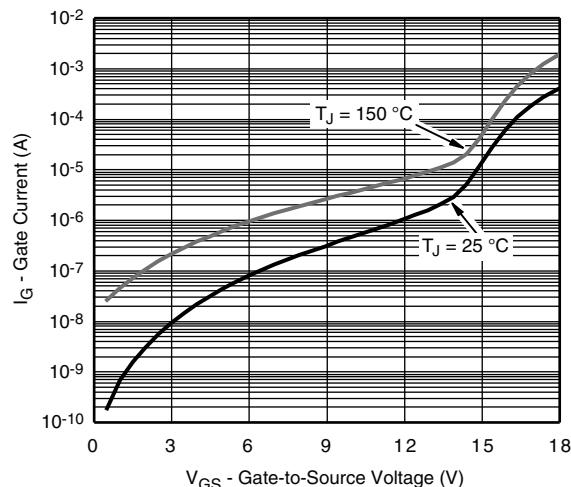
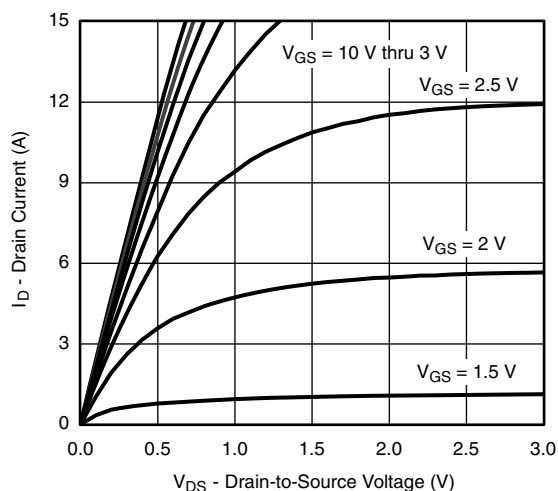
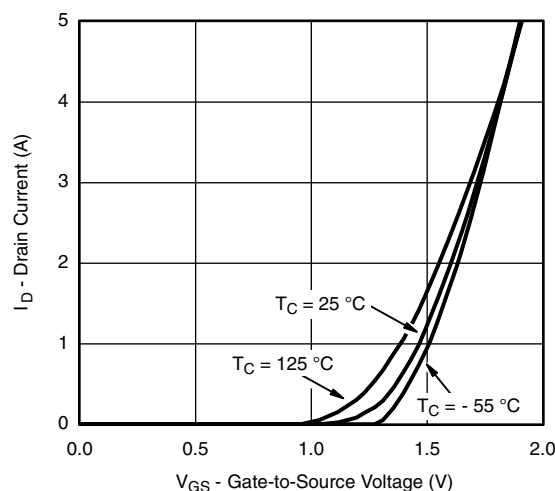
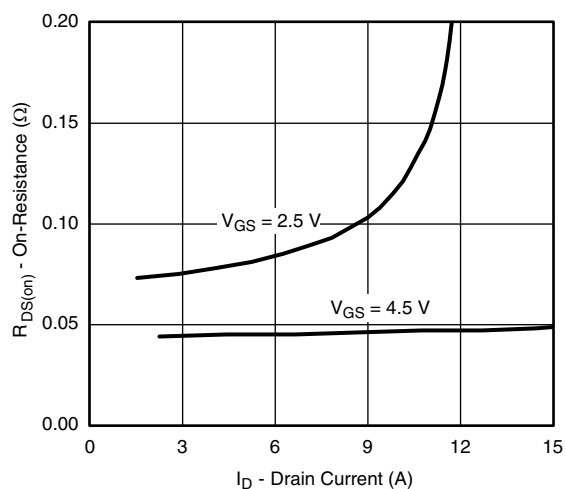
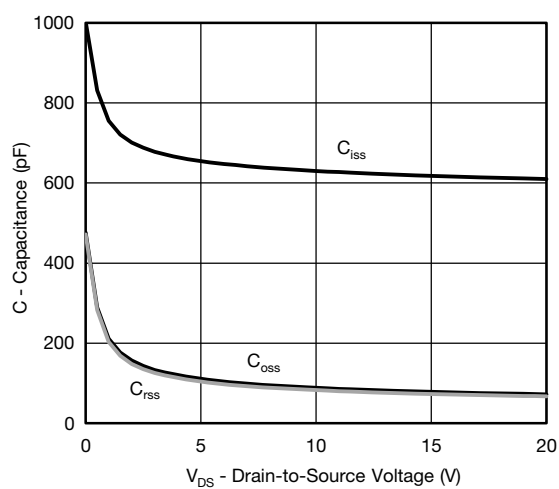


SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
Static							
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = -250 μA	-20	-	-	V	
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	I _D = -250 μA	-	-14	-	mV/°C	
V _{GS(th)} Temperature Coefficient	ΔV _{GS(th)} /T _J		-	2.5	-		
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = -250 μA	-0.5	-	-1.4	V	
Gate-Source Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 4.5 V	-	-	± 0.5	μA	
		V _{DS} = 0 V, V _{GS} = ± 12 V	-	-	± 10		
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = -20 V, V _{GS} = 0 V	-	-	-1		
		V _{DS} = -20 V, V _{GS} = 0 V, T _J = 55 °C	-	-	-10		
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≤ -5 V, V _{GS} = -4.5 V	-15	-	-	A	
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = -4.5 V, I _D = -3.6 A	-	0.047	0.057	Ω	
		V _{GS} = -2.5 V, I _D = -1.5 A	-	0.075	0.095		
Forward Transconductance ^a	g _{fs}	V _{DS} = -10 V, I _D = -3.6 A	-	11	-	S	
Dynamic ^b							
Total Gate Charge	Q _g	V _{DS} = -10 V, V _{GS} = -10 V, I _D = -4.7 A	-	15	23	nC	
		V _{DS} = -10 V, V _{GS} = -4.5 V, I _D = -4.7 A	-	7.1	11		
			-	1.3	-		
Gate-Source Charge	Q _{gs}		-	2.1	-		
Gate-Drain Charge	Q _{gd}		-				
Gate Resistance	R _g	f = 1 MHz	1.4	7	14	Ω	
Turn-On Delay Time	t _{d(on)}	V _{DD} = -10 V, R _L = 2.7 Ω I _D ≅ -3.7 A, V _{GEN} = -4.5 V, R _g = 1 Ω	-	13	25	ns	
Rise Time	t _r		-	15	30		
Turn-Off Delay Time	t _{d(off)}		-	30	60		
Fall Time	t _f		-	10	15		
Turn-On Delay Time	t _{d(on)}	V _{DD} = -10 V, R _L = 2.7 Ω I _D ≅ -3.7 A, V _{GEN} = -10 V, R _g = 1 Ω	-	5	10		
Rise Time	t _r		-	10	20		
Turn-Off Delay Time	t _{d(off)}		-	30	60		
Fall Time	t _f		-	10	20		
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C	-	-	-4.5	A	
Pulse Diode Forward Current	I _{SM}		-	-	-15		
Body Diode Voltage	V _{SD}	I _S = -3.7 A, V _{GS} = 0 V	-	-0.9	-1.2	V	
Body Diode Reverse Recovery Time	t _{rr}	I _F = -3.7 A, di/dt = 100 A/μs, T _J = 25 °C	-	15	30	ns	
Body Diode Reverse Recovery Charge	Q _{rr}		-	6	12	nC	
Reverse Recovery Fall Time	t _a		-	8.5	-	ns	
Reverse Recovery Rise Time	t _b		-	6.5	-		

Notes

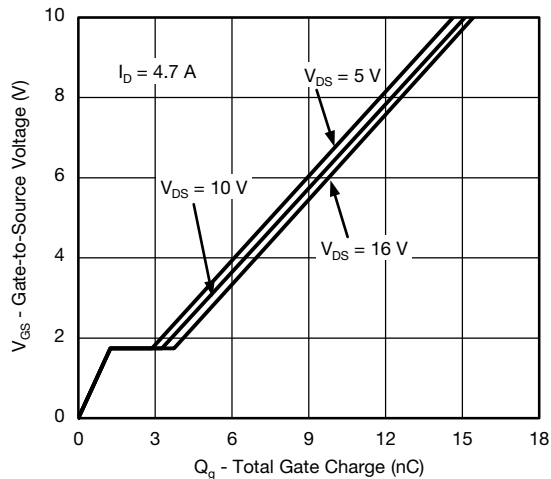
- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

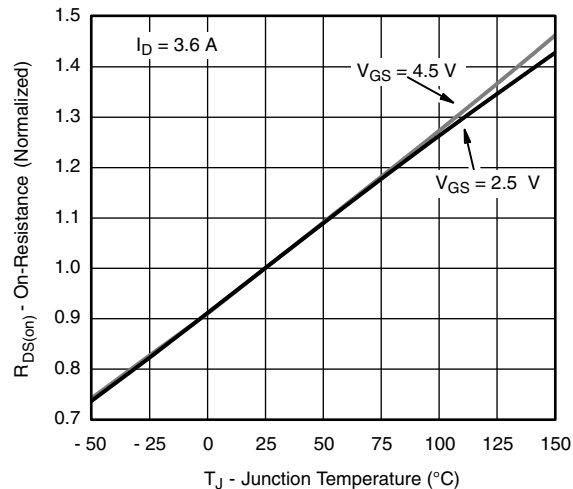
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Gate Current vs. Gate-to-Source Voltage

Gate Current vs. Gate-to-Source Voltage

Output Characteristics

Transfer Characteristics

On-Resistance vs. Drain Current and Gate Voltage

Capacitance



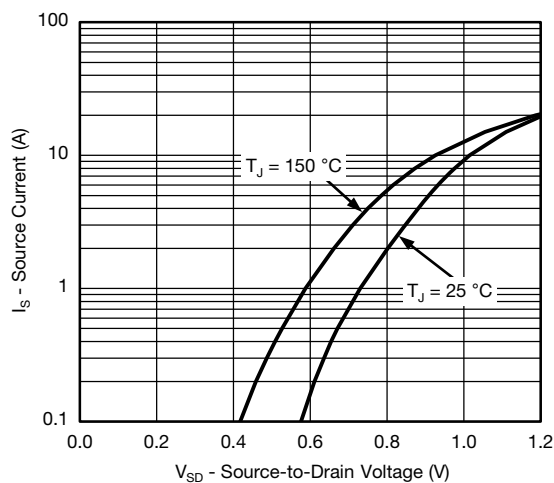
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



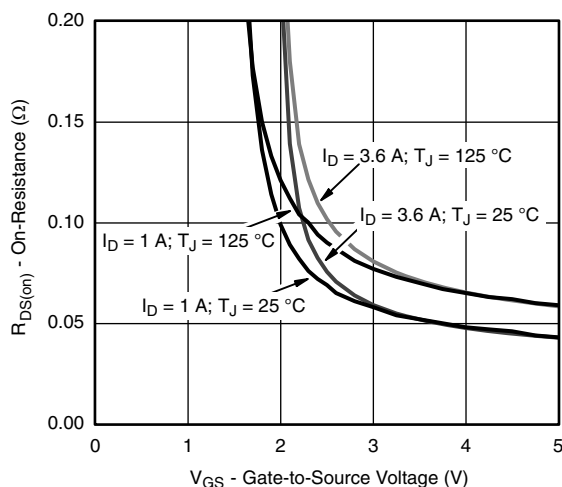
Gate Charge



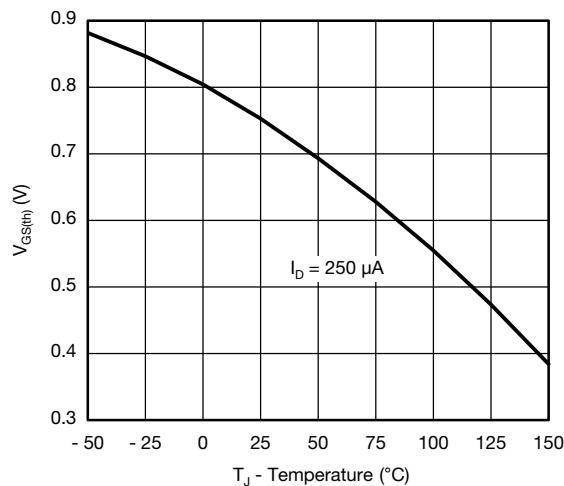
On-Resistance vs. Junction Temperature



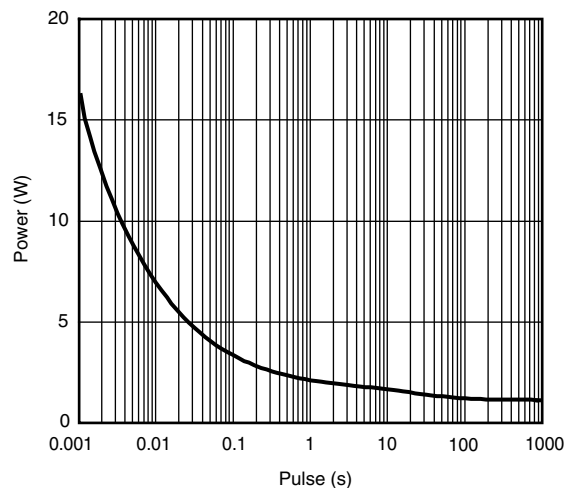
Source-Drain Diode Forward Voltage



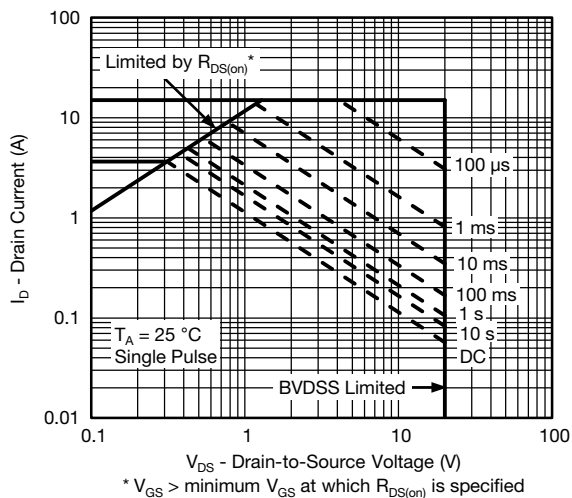
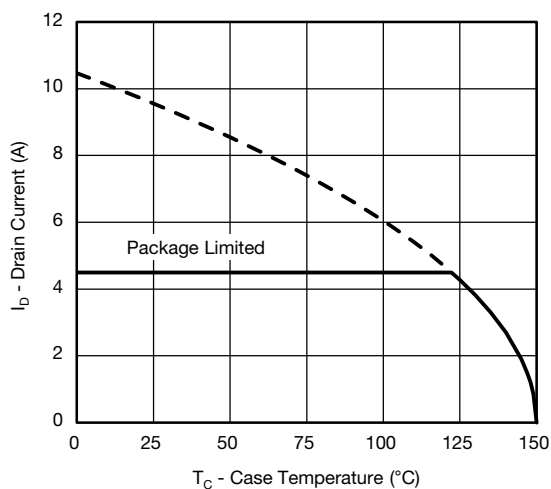
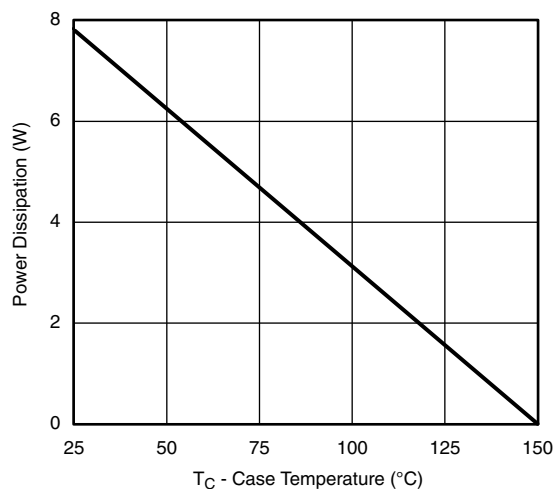
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



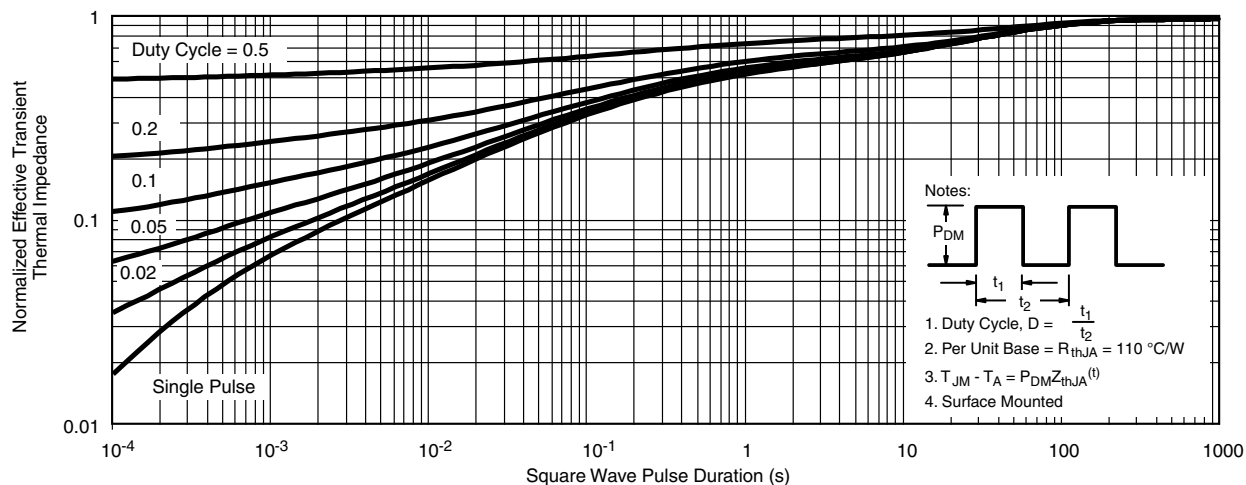
Single Pulse Power, Junction-to-Ambient

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Safe Operating Area, Junction-to-Ambient

Current Derating*

Power Derating

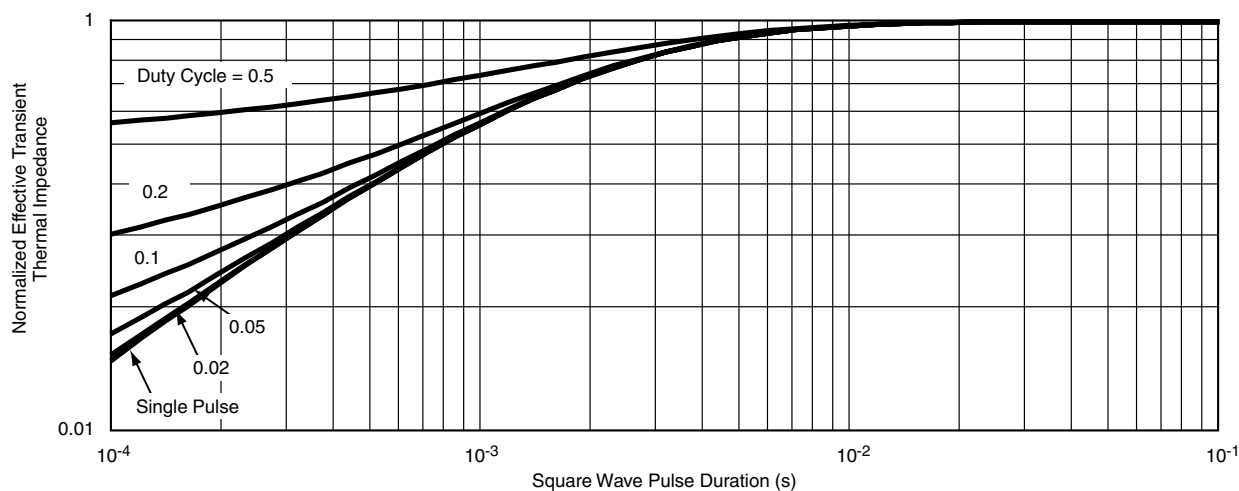
* The power dissipation P_D is based on $T_J (\text{max.}) = 150^\circ\text{C}$, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



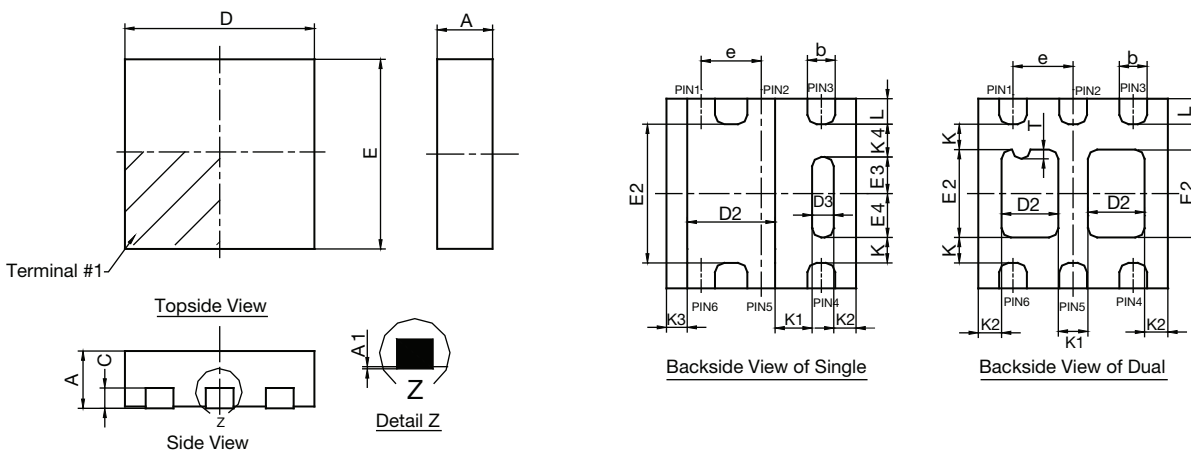
Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?67874.

Case Outline for PowerPAK® SC70T



DIM.	SINGLE PAD						DUAL PAD					
	MILLIMETERS			INCHES			MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.525	0.60	0.65	0.0206	0.024	0.026	0.525	0.60	0.65	0.0206	0.024	0.026
A1	0	-	0.05	0	-	0.002	0	-	0.05	0	-	0.002
b	0.23	0.30	0.38	0.009	0.012	0.015	0.23	0.30	0.38	0.009	0.012	0.015
C	0.15	0.20	0.25	0.006	0.008	0.010	0.15	0.20	0.25	0.006	0.008	0.010
D	1.98	2.05	2.15	0.078	0.081	0.085	1.98	2.05	2.15	0.078	0.081	0.085
D2	0.85	0.95	1.05	0.033	0.037	0.041	0.513	0.613	0.713	0.020	0.024	0.028
D3	0.135	0.235	0.335	0.005	0.009	0.013						
E	1.98	2.05	2.15	0.078	0.081	0.085	1.98	2.05	2.15	0.078	0.081	0.085
E2	1.40	1.50	1.60	0.055	0.059	0.063	0.85	0.95	1.05	0.033	0.037	0.041
E3	0.345	0.395	0.445	0.014	0.016	0.018						
E4	0.425	0.475	0.525	0.017	0.019	0.021						
e	0.65 BSC			0.026 BSC			0.65 BSC			0.026 BSC		
K	0.275 TYP.			0.011 TYP.			0.275 TYP.			0.011 TYP.		
K1	0.400 TYP.			0.016 TYP.			0.320 TYP.			0.013 TYP.		
K2	0.240 TYP.			0.009 TYP.			0.252 TYP.			0.010 TYP.		
K3	0.225 TYP.			0.009 TYP.								
K4	0.355 TYP.			0.014 TYP.								
L	0.175	0.275	0.375	0.007	0.011	0.015	0.175	0.275	0.375	0.007	0.011	0.015
T							0.05	0.10	0.15	0.002	0.004	0.006
ECN: C12-0160-Rev. B, 05-Mar-12 DWG: 5994												

Notes

1. All dimensions are in millimeter. Millimeters will govern.
2. Package outline exclusive of mold flash and metal burr.
3. Package outline inclusive of plating



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