

2.7V to 5.5V

1.3mA(Typ)

3.0µA(Max)

0V to VccV

Motor Drivers for Digital Still Cameras

5-Channel System Lens Driver for Digital Still Cameras

BD6370GUL

General Description

The BD6370GUL is a motor driver that integrates 3 Full-ON or Constant-Voltage type H-bridges, 1 Constant-Voltage or Linear Constant-Current or Full-ON type H-bridge and 1 Linear Constant-Current type H-bridge. The device can drive one stepping motor for auto focus, and DC motors for zoom and iris. It is therefore possible to drive another stepping motor for either zoom or iris, because it has the system to drive 6-channel H-bridges exclusively.

Features

- Low ON-Resistance Power CMOS Output
- Drive Mode Switch Function
- Serial Interface 3-line Bus Control
- Exclusive 6-Channel Drive Function
- 6-Bits D/A Converters for Constant-Voltage and Constant-Current Control
- High-Precision (±5%) Constant-Voltage Driver
- High-Precision (±3%) Linear Constant-Current Driver
- Both Constant-Voltage Drive Block and Constant-Current Drive Block feature Compensation Capacitor-Free Design
- Under Voltage Locked Out Protection & Thermal Shut Down Circuit

Applications

- Mobile system
- Home appliance
- Amusement system, etc

Key Specifications

- Power Supply Voltage Range:
 - 2.7V to 5.5V Motor Power Supply Voltage Range:
 - Circuit Current:
 - Stand-By Current:
- Control Input Voltage Range:
- H-Bridge Output Current:
- -0.4A/ch to +0.4A/ch Output ON-Resistance(Each Channel): 1.4Ω(Typ)
- -25°C to +85°C Operating Temperature Range:

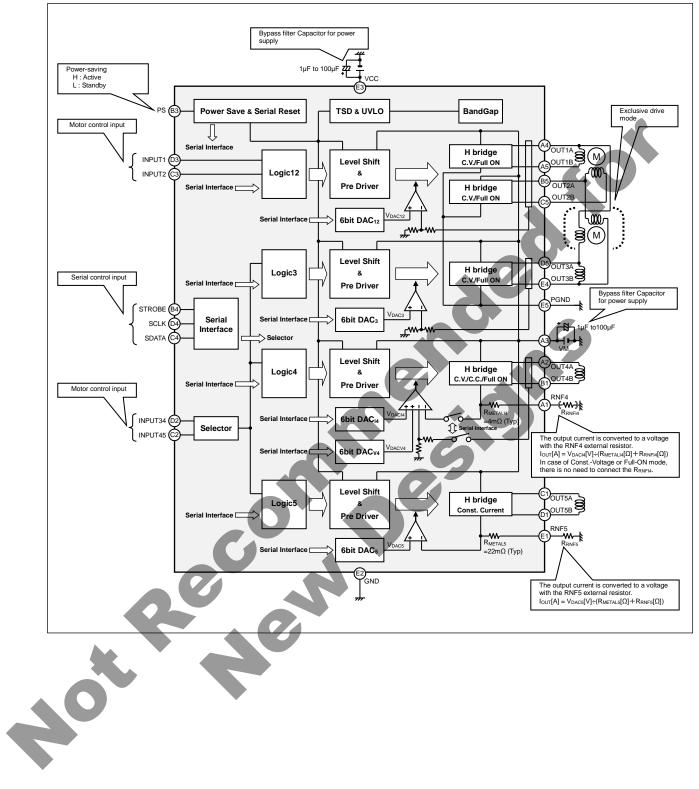
POHIN

Package VCSP50L2 W(Typ) x D(Typ) x H(Max) 2.60mm x 2.60mm x 0.55mm

VCSP50L2

Phase

Typical Application Circuit



Pin Configurations

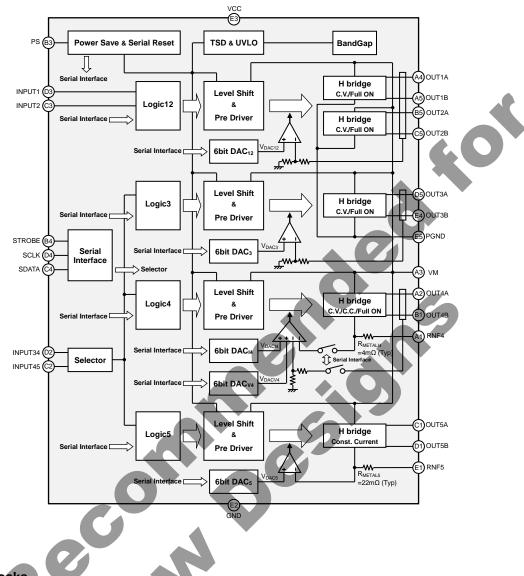
| 1 | 1 | 2 | 3 | 4 | 5 |
|---|-------|---------------|--------|--------|-------|
| A | RNF4 | OUT4A | VM | OUT1A | OUT1B |
| в | OUT4B | INDEX POST | PS | STROBE | OUT2A |
| с | OUT5A | INPUT45 | INPUT2 | SDATA | OUT2B |
| D | OUT5B | INPUT34 | INPUT1 | SCLK | OUT3A |
| E | RNF5 | GND | VCC | OUT3B | PGND |

(TOP VIEW)

Pin Descriptions

| | | | E | RNF5 GND | VCC | OUT3B | PGND | |
|-----|-------------|------------|-------------------|--------------|-----|--------|--------------------------|------------------------------|
| | | | | | | | | |
| | | | | | | | | 6 |
| Pir | n Descripti | ons | | | | | | |
| | Pin No. | Pin Name | Fund | tion | Pin | No. | Pin Nam | Function |
| | A1 | RNF4 | Current detect r | esistor ch.4 | Þ | 1 | OUT5E | 3 H-bridge output 5B |
| | A2 | OUT4A | H-bridge output | D | 2 | INPUT3 | 4 Control logic input 34 | |
| | A3 | VM | Motor power su | oply | D | 3 | INPUT | 1 Control logic input 1 |
| | A4 | OUT1A | H-bridge output | 1A | D | 4 | SCLK | Serial clock input |
| | A5 | OUT1B | H-bridge output | 1B | D | 5 | OUT3A | A H-bridge output 3A |
| | B1 | OUT4B | H-bridge output | 4B | E | 1 | RNF5 | Current detect resistor ch.5 |
| | B2 | INDEX POST | 1 | | E | 2 | GND | Ground |
| | B3 | PS | Power-saving | | E | 3 | VCC | Power supply |
| | B4 | STROBE | Serial enable in | out | E | 4 | OUT3E | 3 H-bridge output 3B |
| | B5 | OUT2A | H-bridge output | 2A | E | 5 | PGND | Motor ground ch.1 to ch.3 |
| | C1 | OUT5A | H-bridge output | 5A | | | | |
| | C2 | INPUT45 | Control logic inp | out 45 | | | | |
| | C3 | INPUT2 | Control logic inp | out 2 | | | | |
| | C4 | SDATA | Serial data input | t | | | | |
| | C5 | OUT2B | H-bridge output | 2B | | | | |

Block Diagram



Description of Blocks

1. Power-Saving and Serial Reset

A power-saving function is included, which allows the system to save power when not driving the motor. The voltage level on this pin should be set high so as to keep the operation mode. (See the Electrical Characteristics; p.7/32) Cancel power-saving mode after turning on power supply V_{CC} and V_M, because PS pin combines with power-saving function and serial reset function block. If PS pin is always short-circuited to the power supply VCC terminal, reset function may not work, and it may cause the device to malfunction. (See the Sequence of Serial Control Input; p.9/32)

Motor Control Input (INPUT1, INPUT2, INPUT34, INPUT45)

Logic level controls the output logic of H-Bridge.

(See the Electrical Characteristics; p.7/32 and I/O Truth Table; p.19/32 to p.23/32)

INPUT34 pin corresponds to channel 3 or channel 4, and INPUT45 pin to channel 4 or channel 5 respectively. These channels can be set via serial interface.

3. H-Bridge

Because the respective output transistors consist of power CMOS which consumes a motor power supply V_M , the high and low-side ON-Resistance value is dependent upon V_M voltage. Further, the application must be designed so that the maximum H-bridge current for each channel is 400mA or below. (See the Recommended Operating Conditions; p.6/32)

The 3 H-bridges (channel 1 to channel 3) can be driven as the exclusive 4-channel. As long as two stepping motors don't drive simultaneously, it is possible to drive them by channel 1 to channel 3.

Description of Blocks – continued

4. The D/A Converter Settings for Each Channel

The three H-Bridges (channel 1 to 3) can drive motors as Constant-Voltage or Full-ON mode. The H-Bridge of channel 4 can drive it as Constant-Voltage or Constant-Current or Full-ON mode, while the H-Bridge of channel 5 is always set for Constant-Current mode. In case of driving each H-bridge as Full-ON mode, serial data of each D/A Converter (DAC12 and DAC3) for Constant-Voltage mode should be set all bits high. If channel 4 is set to Constant-Voltage mode, serial data of D/A Converter (DAC14) for Constant-Current mode should be set all bits high. In case of driving H-bridge as Constant-Current mode, serial data of D/A Converter (DACV4) for Constant-Voltage mode should be set all bits high, while driving as Full-ON mode, serial data of both D/A Converters should be set all bits high. In case of driving channel 4 as Constant-Voltage or Full-ON mode, it is not necessary to connect the external resistor for output current detection at RNF4 pin. When driving as Constant-Current mode, design the application in consideration of both internal metal impedance and external resistor for output current detection.

(a) Full-ON Mode (Channel 1 to Channel 4)

D/A Converter Setting Range V_{DACx}: 6'b111111 Fixed (x = 12, 3, V4, and I4)

(b) Constant-Voltage Mode (Channel 1 to Channel 4)

Formula for Output High Voltage: $V_{VOHx}[V] = 8 \times V_{DACx}[V]$ (8 x $V_{DACx} \le V_M[V]$, x = 12, 3, and V4) $V_{VOHx}[V] = V_M[V]$ (8 x $V_{DACx} > V_M[V]$, x = 12, 3, and V4)

D/A Converter Setting Range 8 x V_{DACx} : 6'b010100 to 111111 (x = 12, 3, and V4) (In case of setting channel 4, set V_{DACl4} : 6'b111111, in addition to the above condition)

(c) Constant-Current Mode (Channel 4 & Channel 5)

Formula for Output Current: $I_{OUTx}[A] = V_{DACx}[V] / (R_{METALx}[\Omega] + R_{NFx}[\Omega]) (x = 14 and 5)$

 $\begin{array}{l} R_{\text{METALx}}; \mbox{ the internal metal impedance} \\ (Channel 4; R_{\text{METALI4}}[\Omega] = 0.004(Typ)) \\ (Channel 5; R_{\text{METAL5}}[\Omega] = 0.022(Typ)) \\ R_{\text{NFx}}; \mbox{ the resistor value for output current detection at RNFx pin} \end{array}$

D/A Converter Setting Range V_{DACx}: 6'b001010 to 111111 (x = I4 and 5) (In case of setting channel 4, set V_{DACV4}: 6'b111111, in addition to the above condition)

Absolute Maximum Ratings (Ta=25°C)

| Parameter | Symbol | Limit | Unit |
|----------------------------|------------------|----------------------------------|------|
| Power Supply Voltage | Vcc | -0.3 to +6.5 | V |
| Motor Power Supply Voltage | VM | -0.3 to +6.5 | V |
| Control Input Voltage | Vin | -0.3 to +Vcc+0.3 | V |
| Power Dissipation | Pd | 0.83 (Note 1) | W |
| H-bridge Output Current | I _{OUT} | -0.5 to +0.5 ^(Note 2) | A/ch |
| Storage Temperature Range | Tstg | -55 to +150 | °C |
| Junction Temperature | Tjmax | 150 | °C |

(Note 1) Reduced by 6.64mW/°C over 25°C, when mounted on a glass epoxy board (50mm x 58mm x 1.75mm; 8layers)

(Note 2) Must not exceed Pd, ASO, or Tjmax of 150°C

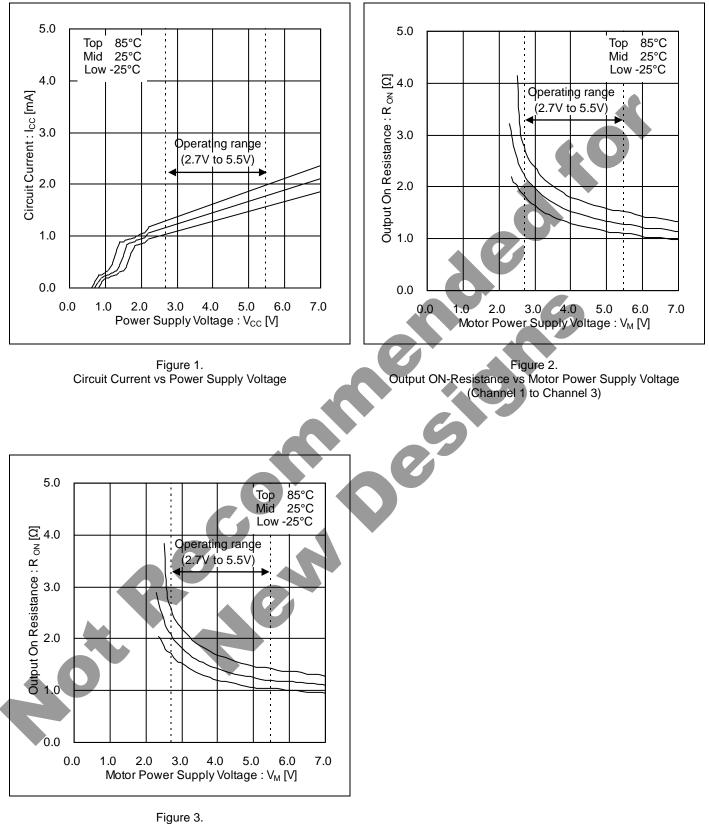
Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

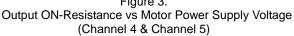
Recommended Operating Conditions

| Symbol | Min | Тур | Max | Unit |
|----------------|--|---|---|---|
| Vcc | 2.7 | | 5.5 | V |
| V _M | 2.7 | | 5.5 | V |
| VIN | 0 | - | Vcc | V |
| fın | 0 | - | 100 | kHz |
| fsclk | 0 | - | 10 | MHz |
| Іоцт | -0.4 | | +0.4 | A/ch |
| Topr | -25 | | +85 | °C |
| | | | | |
| | Vcc VM VIN fIN fsclk Iout | Vcc 2.7 Vm 2.7 ViN 0 fin 0 fscLk 0 lour -0.4 Topr -25 | Vcc 2.7 - V _M 2.7 - V _{IN} 0 - f _{IN} 0 - fsclk 0 - lour -0.4 - Topr -25 - | V _{CC} 2.7 - 5.5 V _M 2.7 - 5.5 V _{IN} 0 - Vcc fin 0 - 100 fsclk 0 - 10 lout -0.4 - +0.4 Topr -25 +85 |

Electrical Characteristics (Unless otherwise specified V_{CC}=3.0V, V_M=5.0V, Ta=25°C, Serial=Binary Notation) Parameter Symbol Min Unit Conditions Typ Max All Circuits Stand-by Current 0 3.0 μA VPS=0V ICCST _ mΑ Circuit Current 1.3 2.0 V_{PS}=3V with no signal, no load Icc Control Input (IN=PS, INPUT1 to INPUT45, STROBE, SCLK, SDATA) High Level Input Voltage 2.0 V VINH Vcc -Low Level Input Voltage VINL 0 0.7 V High Level Input Current 1 IINH1 15 30 60 μA VINH1 (PS, INPUTx) =3V High Level Input Current 2 7.5 30 VINH2 (STROBE, SCLK, SDATA) =3V I_{INH2} 15 μΑ Low Level Input Current IINL -1 0 μA VINL=0V Under Voltage Locked Out (UVLO) **UVLO** Voltage VUVLO 1.6 2.4 V Constant-Voltage Drive / Full-ON Drive Block (Channel 1 to Channel 3) lour=±400mA, High & Low-side Total **Output ON-Resistance** 1.75 Ron 1.40 Ω V DACx:010100, RL=20Ω Output High Voltage 1 Vон1 1.35 1.50 1.65 V Output High Voltage 2 V_{OH2} 2.85 3.00 3.15 DACx:101000, R_L=20Ω Vонз 4.49 4.96 DACx:111111, RL=20Ω Output High Voltage 3 4.73 V DVRES **DAC Resolution** 6 BITS 75mV/LSB _ **Differential Nonlinearity** $\mathsf{DV}_{\mathsf{DNL}}$ -1 _ LSB +1 -2 +2 LSB Integral Nonlinearity DVINL -1.5 DACx:010100 Min Voltage of DAC Setting DV_{RNG} V Constant-Voltage Drive / Constant-Current Drive / Full-ON Drive Block (Channel 4) **Output ON-Resistance** Ron 1.40 1.75 Ω 100T=±400mA, High & Low-side Total Voh1 1.35 Output High Voltage 1 1.50 1.65 V DACV4:010100, RL=20Ω Output High Voltage 2 VOH2 2.85 3.00 3.15 v DACV4:101000, RL=20Ω Output High Voltage 3 Vонз 4.49 4.73 4.96 V DACV4:111111, RL=20Ω DVRES BITS 75mV/LSB **DAC Resolution** -6 -LSB **Differential Nonlinearity** DVDNL -1 +1 LSB Integral Nonlinearity DVINL -2 +2 -Min Voltage of DAC Setting DVRNG 1.5 V DACV4:010100 _ _ **RNF** Voltage 1 VRNF1 40 50 60 mV DACI4:001010, R_{NF}=0.5Ω, R_L=10Ω **RNF** Voltage 2 VRNF2 94 99 104 mV DACI4:010100, R_{NF}=0.5Ω, R_L=10Ω 178 RNF Voltage 3 198 218 mV DACI4:101000, R_{NF}=0.5Ω, R_L=10Ω V_{RNF3} DIRES DAC Resolution 6 BITS 5mV/LSB _ -**Differential Nonlinearity** -1 LSB DIDNL -+1Integral Nonlinearity -2 LSB DINL +2 -Min Voltage of DAC Setting 50 mV DACI4:001010 DIRNG _ _ Constant-Current Drive Block (Channel 5) **Output ON-Resistance** Ron 1.40 1.75 Ω IOUT=±400mA, High & Low-side Total **RNF** Voltage 1 38 48 m٧ DAC5:001010, R_{NF}=0.5Ω, R_L=10Ω V_{RNF1} 58 **RNF** Voltage 2 VRNF2 91 96 101 mV DAC5:010100, R_{NF}=0.5Ω, R_L=10Ω 172 mV DAC5:101000, R_{NF}=0.5Ω, R_L=10Ω **RNF** Voltage 3 V_{RNF3} 192 212 6 BITS 5mV/LSB **DAC Resolution** DIRES ---1 **Differential Nonlinearity** DIDNL +1 LSB -2 Integral Nonlinearity DIINL -+2 LSB Min Voltage of DAC Setting DIRNG 50 mV DAC5:001010

Typical Performance Curves (Reference Data)





Timing chart

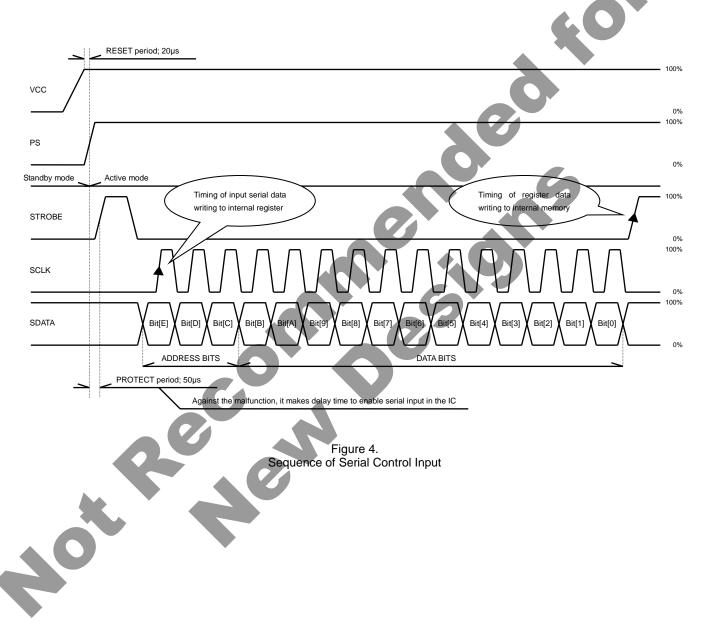
Serial Input (STROBE, SCLK, and SDATA)

The BD6370GUL provides the D/A converter and 3-line serial interface for setting output modes.

SDATA is sent to the internal shift register during the STROBE low interval at the SCLK rising edge. Shift register data (Bit[B] to Bit[0]) is written to the internal 12-bit memory simultaneously with STROBE rising edge, according to the addresses stored in Bit[E], Bit[D], and Bit[C]. The input first serial data is Bit[E] and the last is Bit[0].

In case of the exclusive drive mode (MODE13=1 and/or MODE23=1), each serial bit of DAC12 and DAC3 should be input the same data.

Cancel power-saving mode after turning on power supply V_{CC} and V_M . All serial data will be reset to 0 when the PS pin voltage changes to Low-level, because PS pin combines with power-saving function and serial data clear function block. These data will be also reset to 0 when the UVLO or TSD circuit operates.



Serial Register Bit Map

The Bit Map is consisted of 5 addresses and 60 data. There are some prohibited bits in the serial data MODExx, so set no kind of cases. (See the I/O Truth Table (Selection of Exclusive Drive Mode); p.11/32) Must not set TEST bits and initial data must be held at 0 (GND).

Table 1. Bit Map (ADDRESS BIT)

| No. | ADDRESS BIT | | | | | | |
|-------|-------------|--------|--------|--|--|--|--|
| INO. | Bit[E] | Bit[D] | Bit[C] | | | | |
| 00H | 0 | 0 | 0 | | | | |
| 01H | 0 | 0 | 1 | | | | |
| 02H | 0 | 1 | 0 | | | | |
| 03H | 03H 0 | | 1 | | | | |
| 04H 1 | | 0 | 0 | | | | |

Bit[41

Table 2. Bit Map (DATA BIT)

| No. | | | | | | DAT | A BIT | | | | | |
|-----|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|
| NU. | Bit[B] | Bit[A] | Bit[9] | Bit[8] | Bit[7] | Bit[6] | Bit[5] | Bit[4] | Bit[3] | Bit[2] | Bit[1] | Bit[0] |
| 00H | TEST | TEST | MODE 45 | MODE 34 | MODE 23 | MODE 13 | MODE 3C | MODE 3B | MODE 3A | MODE 12C | MODE 12B | MODE 12A |
| 01H | DAC 12[5] | DAC 12[4] | DAC 12[3] | DAC 12[2] | DAC 12[1] | DAC 12[0] | MODE 5B | MODE 5A | MODE 4D | MODE 4C | MODE 4B | MODE 4A |
| 02H | DAC 5[5] | DAC 5[4] | DAC 5[3] | DAC 5[2] | DAC 5[1] | DAC 5[0] | DAC 3[5] | DAC 3[4] | DAC 3[3] | DAC 3[2] | DAC 3[1] | DAC 3[0] |
| 03H | DAC V4[5] | DAC V4[4] | DAC V4[3] | DAC V4[2] | DAC V4[1] | DAC V4[0] | DAC 14[5] | DAC I4[4] | DAC I4[3] | DAC I4[2] | DAC I4[1] | DAC I4[0] |
| 04H | TEST | TEST | IN5B | IN5A | IN4B | IN4A | IN3B | IN3A | IN2B | IN2A | IN1B | IN1A |
| | | | | | | | | | | | | |

| Table 3. Bit Function | | | | |
|-------------------------------|--|--|--|--|
| Bit Name | Function | | | |
| MODExA (x=1 to 5) | Control mode selection for channel 1 to channel 5 | | | |
| MODExB (x=1 to 5) | Control mode selection for channel 1 to channel 5 | | | |
| MODExC (x=1 to 3) | Choice of Constant-Voltage or Full-ON mode for channel 1 to channel 3 | | | |
| MODExD (x=4) | Choice of Constant-Voltage or Constant-Current or Full-ON mode for channel 4 | | | |
| MODE13 | Exclusive drive mode selection for OUT1A-OUT3A | | | |
| MODE23 | Exclusive drive mode selection for OUT2A-OUT3B | | | |
| MODE34 | Choice to connect channel 3 or channel 4 via INPUT34 pin | | | |
| MODE45 | Choice to connect channel 4 or channel 5 via INPUT45 pin | | | |
| INxA (x=1 to 5) | Control mode selection for channel 1 to channel 5 | | | |
| INxB (x=1 to 5) | Control mode selection for channel 1 to channel 5 | | | |
| DACx[y] (x=12 to 5, y=0 to 5) | D/A Converter output selection for channel 1 to channel 5 | | | |
| TEST | TEST BIT (All bits must be held at GND) | | | |

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| ADR. | | DATA BIT | | | | | | | | | | |
|------|------------------|------------------|------------|------------|------------|------------|------------|------------|------------|-------------|-------------|-------------|
| ADR. | Bit[B] | Bit[A] | Bit[9] | Bit[8] | Bit[7] | Bit[6] | Bit[5] | Bit[4] | Bit[3] | Bit[2] | Bit[1] | Bit[0] |
| 000 | TEST (Note 5) | TEST (Note 5) | MODE 45 | MODE 34 | MODE 23 | MODE 13 | MODE 3C | MODE 3B | MODE 3A | MODE 12C | MODE 12B | MODE 12A |

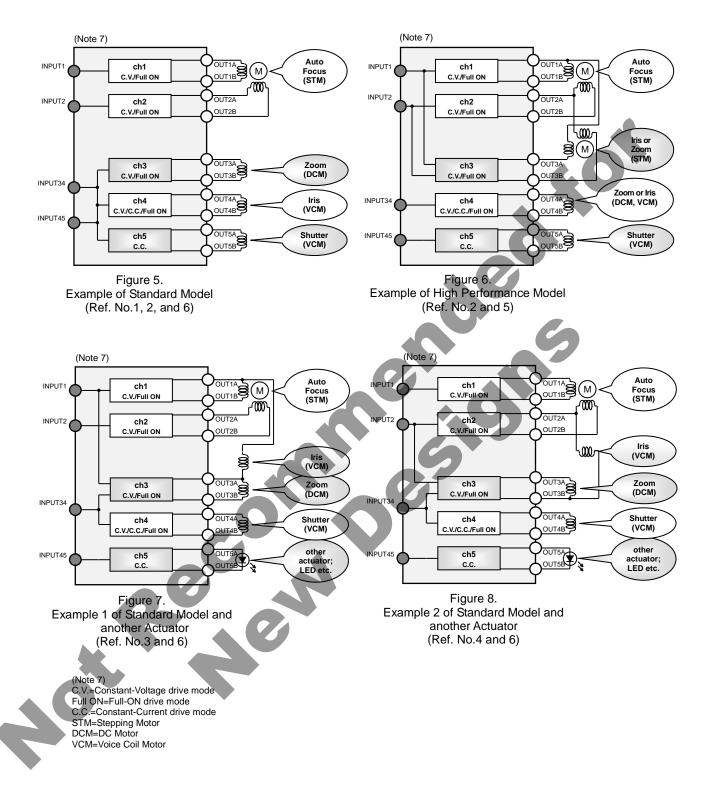
(Note 5) Must be held at 0 (GND)

| Refer to the | p.19/32 to p.2 p.20/32 about Truth Table fo | ~ | | | |
|--------------|---|------------------|----------------------|------------------|------------------|
| Bit[5] | Bit[2] | Drive | Mode for Output Terr | | |
| MODE3C | MODE12C | Channel 3 | Channel 2 | Channel 1 | Note |
| 0 | - | Full-ON | - | - | DAC3: 6'b111111 |
| 1 | - | Constant-Voltage | - | - | |
| - | 0 | - | Full-ON | Full-ON | DAC12: 6'b111111 |
| - | 1 | - | Constant-Voltage | Constant-Voltage | |

| Table 6 I/O | Truth Table | for Exclusive D | rive Mode Selection |
|-------------|--------------|-----------------|---------------------|
| | ITUILI IADIE | | |

| _ | | 1 | _ | | Constant-v | Shage C | Jonstant-volt | age | |
|-----------------------|-----------------------|-------------|------------|--------------|--------------|--------------|---------------|-------------------------|----------------------|
| Table 6. I | /O Truth ⁻ | Table for I | Exclusive | Drive Mode | Selection | | | 6 | |
| Bit[9] | Bit[8] | Bit[7] | Bit[6] | Input | t Pins Corre | spond to O | utputs | Note | |
| MODE 45 | MODE 34 | MODE 23 | MODE 13 | INPUT 45 | INPUT 34 | INPUT 2 | INPUT | Opened Output Terminals | Ref No. (Next) |
| 0 | 0 | 0 | 0 | OUT 4A-4B | OUT 3A-3B | OUT 2A-2B | OUT 1A-1B | OUT5A, 5B | 1 |
| 0 ^(Note 6) | 0 | 0 | 1 | | | | | | |
| 0 ^(Note 6) | 0 | 1 | 0 | | | | | | |
| 0 ^(Note 6) | 0 | 1 | 1 | | | | | | |
| 0 | 1 | 0 | 0 | OUT 5A-5B | OUT 4A-4B | OUT 2A-2B | OUT 1A-1B | OUT3A, 3B | 2 |
| 0 | 1 | 0 | 1 | OUT 5A-5B | OUT 4A-4B | OUT 2A-2B | OUT 1A-3A | OUT1B, 3B | 3 |
| 0 | 1 | 1 | 0 | OUT 5A-5B | OUT 4A-4B | OUT 2A-3B | OUT 1A-1B | OUT2B, 3A | 4 |
| 0 | 1 | 1 | 1 | OUT 5A-5B | OUT 4A-4B | OUT 2A-3B | OUT 1A-3A | OUT1B, 2B | 5 |
| 1 | 0 | 0 | 0 | OUT 5A-5B | OUT 3A-3B | OUT 2A-2B | OUT 1A-1B | OUT4A, 4B | 6 |
| ↑ (Not e 6) | 0 | 0 | 1 | | | | | | |
| 1 ^(Note 6) | 0 | 1 | 0 | | | | | | |
| 1 (Note 6) | 0 | 1 | 1 | | | | | | |
| 1 ^(Note 6) | 1 | 0 | 0 | | | | | | |
| 1 ^(Note 6) | 1 | 0 | 1 | | | | | | |
| 1 ^(Note 6) | 1 | 1 | 0 | | | | | | |
| 1 ^(Note 6) | 1 | 1 | 1 | | | | | | |
| (Marte C) Mar | at not oot do | 4- | | | | | | | |

(Note 6) Must not set data



| Table 7. DATA BIT MAP [001] |
|-----------------------------|
|-----------------------------|

| ADR. | | | | | | DAT | A BIT | | | | | |
|------|--------------|--------------|--------------|--------------|--------------|--------------|------------|------------|------------|------------|------------|------------|
| ADR. | Bit[B] | Bit[A] | Bit[9] | Bit[8] | Bit[7] | Bit[6] | Bit[5] | Bit[4] | Bit[3] | Bit[2] | Bit[1] | Bit[0] |
| 001 | DAC 12[5] | DAC 12[4] | DAC 12[3] | DAC 12[2] | DAC 12[1] | DAC 12[0] | MODE 5B | MODE 5A | MODE 4D | MODE 4C | MODE 4B | MODE 4A |

Refer to the p.22/32 about MODE4A & MODE4B. Refer to the p.23/32 about MODE5A & MODE5B.

| Table 8. Function Table for Output Drive M | Node Selection (Channel 4) |
|--|----------------------------|
|--|----------------------------|

| | | The Mode Select | |
|--------|--------|------------------|---|
| Bit[3] | Bit[2] | Drive Mode | Note |
| MODE4D | MODE4C | | |
| 0 | 0 | Full-ON | DACV4=DACI4: 6'b11111, RNF4 pin should be directly connected to ground |
| 0 | 1 | Full-ON | DACV4=DACI4: 6'b11111, RNF4 pin should be directly connected to ground |
| 1 | 0 | Constant Voltage | DACI4: 6'b111111, RNF4 pin should be directly connected to ground |
| 1 | 1 | Constant Current | DACV4: 6'b111111, RNF4 pin with resistor should be connected to ground |
| | | | |

| Table O. Function Table for Output | Valte ve in acce of Constant Valte ve | Made (Chapped 4.9 Chapped 2) |
|------------------------------------|---------------------------------------|------------------------------|
| Table 9. Function Table for Output | Voltage in case of Constant Voltage | Wode (Channel 1 & Channel Z) |
| | | |

| DAC12[5] 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 | DAC12[4] 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 | DAC12[3] 0 0 0 0 | DAC12[2] 1 1 1 | DAC12[1] 0 0 | DAC12[0] 0 | VDAC12 [V] 0.188 | Voltage; Vон [V] 1.500 |
|--|--|------------------------------|-------------------------|--------------------|---------------|---------------------|---------------------------|
| 0 0 0 0 0 0 | 1 1 1 1 1 | 0 0 0 | 1 | | | 0.100 | 1.500 |
| 0 0 0 0 0 | 1 1 1 | 0 0 | | Ų | 1 | 0.197 | 1.575 |
| 0 0 0 0 | 1 1 | 0 | 1 | 1 | 0 | 0.206 | 1.650 |
| 0 0 0 | 1 | | 1 | 1 | 1 | 0.216 | 1.725 |
| 0 0 | | 1 | 0 | 0 | 0 | 0.225 | 1.800 |
| 0 | | | | | | | |
| | | 1 | 0 | 0 | 1 | 0.234 | 1.875 |
| 0 | 1 | 1 | 0 | 1 | 0 | 0.244 | 1.950 |
| • | 1 | 1 | 0 | 1 | 1 | 0.253 | 2.025 |
| 0 | 1 | 1 | 1 | 0 | 0 | 0.263 | 2.100 |
| 0 | 1 | 1 | 1 | 0 | 1 | 0.272 | 2.175 |
| 0 | 1 | 1 | 1 | 1 | 0 | 0.281 | 2.250 |
| 0 | 1 | 1 | 1 | 1 | 1 | 0.291 | 2.325 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0.300 | 2.400 |
| 1 | 0 | 0 | 0 | 0 | 1 | 0.309 | 2.475 |
| 1 | 0 | 0 | 0 | 1 | 0 | 0.319 | 2.550 |
| 1 | 0 | 0 | 0 | 1 | 1 | 0.328 | 2.625 |
| 1 | 0 | 0 | 1 | 0 | 0 | 0.338 | 2.700 |
| 1 | 0 | 0 | 1 | 0 | 1 | 0.347 | 2.775 |
| 1 | 0 | 0 | 1 | 1 | 0 | 0.356 | 2.850 |
| 1 | 0 | 0 | 1 | 1 | 1 | 0.366 | 2.925 |
| 1 | 0 | 1 | 0 | 0 | 0 | 0.375 | 3.000 |
| 1 | 0 | 1 | 0 | 0 | 1 | 0.384 | 3.075 |
| 1 | 0 | 1 | 0 | 1 | 0 | 0.394 | 3.150 |
| 1 | 0 | 1 | 0 | 1 | 1 | 0.403 | 3.225 |
| 1 | 0 | 1 | 1 | 0 | 0 | 0.413 | 3.300 |
| 1 | 0 | 1 | 1 | 0 | 1 | 0.422 | 3.375 |
| 1 | 0 | 1 | | 1 | 0 | 0.431 | 3.450 |
| 1 | 0 | 1 | 1 | 1 | 1 | 0.441 | 3.525 |
| 1 | 1 | 0 | 0 | 0 | 0 | 0.450 | 3.600 |
| 1 | 1 | 0 | 0 | 0 | 1 | 0.459 | 3.675 |
| 1 | 1 | 0 | 0 | 1 | 0 | 0.469 | 3.750 |
| 1 | 1 | 0 | 0 | 1 | 1 | 0.478 | 3.825 |
| 1 | 1 | 0 | 1 | 0 | 0 | 0.488 | 3.900 |
| 1 | 1 | 0 | | 0 | 1 | 0.497 | 3.975 |
| 1 | 1 | 0 | 1 | 1 | 0 | 0.506 | 4.050 |
| 1 | 1 | 0 | 1 | 1 | 1 | 0.516 | 4.125 |
| 1 | 1 | 1 | 0 | 0 | 0 | 0.525 | 4.200 |
| 1 | 1 | 1 | 0 | 0 | 1 | 0.534 | 4.275 |
| 1 | 1 | 1 | 0 | 1 | 0 | 0.544 | 4.350 |
| | 1 | 1 | 0 | 1 | 1 | 0.553 | 4.425 |
| | 1 | 1 | 1 | 0 | 0 | 0.563 | 4.500 |
| 1 | 1 | 1 | 1 | 0 | 1 | 0.572 | 4.575 |
| 1 | 1 | 1 | 1 | 1 | 0 | 0.581 | 4.650 |
| 1 | 1 | 1 | 1 | 1 | 1 | 0.591 | 4.650 |

Table 10. DATA BIT MAP [010]

| | | | | | | DAT | A BIT | | | | | | | | | |
|-------|-------------|-------------|---------------|-------------|------------|-----------|-------------|----|-----------|-------------|-------------|--------------|-------------|--|--|--|
| ADR. | Bit[B] | Bit[A] | Bit[9] | Bit[8] | Bit[7 | 7] Bit[6] | Bit[5] | Bi | it[4] | Bit[3] | Bit[2] | Bit[1] | Bit[0] | | | |
| 010 | DAC 5[5] | DAC 5[4] | DAC 5[3] | DAC 5[2] | DA(5[1 | | DAC 3[5] | | AC [4] | DAC 3[3] | DAC 3[2] | DAC 3[1] | DAC 3[0] | | | |
| | 0[0] | 5[7] | 0[0] | J[2] | |] 0[0] | 0[0] | | [7] | 0[0] | 0[2] | 0[1] | 5[0] | | | |
| | | | | | | | | | | | | | | | | |
| | | | or Output Vol | | | | | | | | | | | | | |
| Bit[5 | - | Bit[4] | Bit[3] | Bit[| | Bit[1] | Bit[0] | | D | AC3 Volta | | Output | | | | |
| DAC3 | [5] D | AC3[4] | DAC3[3] | DAC | | DAC3[1] | DAC3[| 0] | | VDAC3 [V] | | Voltage; V | | | | |
| 0 | | 1 | 0 | 1 | | 0 | 0 | | | 0.188 | | 1.50 | | | | |
| 0 | | 1 | 0 | 1 | | 0 | 1 | | | 0.197 | | 1.57 | | | | |
| 0 | | 1 | 0 | 1 | | 1 | 0 | | | 0.206 | | 1.65 | | | | |
| 0 | | 1 | 0 | 1 | | 1 | 1 | | | 0.216 | | 1.72 | | | | |
| 0 | | 1 | 1 | 0 | | 0 | 0 | | | 0.225 | | 1.80 | | | | |
| 0 | | 1 | 1 | 0 | | 0 | 1 | | | 0.234 | | 1.87 | | | | |
| 0 | | 1 1 | 1 | 0 | | 1 | | | | 0.244 | | 1.95 2.02 | | | | |
| 0 | | 1 | 1 | 0 | | 0 | 1 | | | 0.253 | | 2.02 | | | | |
| 0 | | 1 | 1 | 1 | | 0 | | | | 0.263 | | 2.10 | | | | |
| 0 | | 1 | 1 | 1 | | 1 | 1 | | | 0.272 | | 2.17 | | | | |
| 0 | | 1 | 1 | 1 | | 1 | | | | 0.201 | | 2.23 | | | | |
| 1 | | 0 | 0 | 0 | | 0 | 0 | | | 0.291 | | 2.32 | | | | |
| 1 | | 0 | 0 | 0 | | 0 | 1 | | | 0.309 | | 2.40 | | | | |
| 1 | | 0 | 0 | 0 | | 1 | 0 | | | 0.309 | | 2.47 | | | | |
| 1 | | 0 | 0 | 0 | | 1 | 0 | | | 0.328 | | 2.62 | | | | |
| 1 | | 0 | 0 | 1 | | 0 | 0 | - | | 0.338 | | 2.02 | | | | |
| 1 | | 0 | 0 | 1 | | 0 | 1 | | | 0.347 | | 2.70 | | | | |
| 1 | | 0 | 0 | | | 1 | | | | 0.356 | | 2.85 | | | | |
| 1 | | 0 | 0 | | | 1 | | | | 0.366 | | 2.92 | | | | |
| 1 | | 0 | 1 | | | 0 | 0 | | | 0.375 | | 3.00 | | | | |
| 1 | | 0 | 1 | 0 | | 0 | 1 | | | 0.384 | | 3.07 | | | | |
| 1 | | 0 | 1 | 0 | | 1 | 0 | | | 0.394 | | 3.15 | | | | |
| 1 | | 0 | | 0 | | 1 | 1 | | | 0.403 | | 3.22 | | | | |
| 1 | | 0 | | 1 | | 0 | 0 | | | 0.413 | | 3.30 | | | | |
| 1 | | 0 | 1 | 1 | | 0 | 1 | | | 0.422 | | 3.37 | | | | |
| 1 | | 0 | 1 | | | 1 | 0 | | | 0.431 | | 3.45 | | | | |
| 1 | | 0 | 1 | 1 | | 1 | 1 | | | 0.441 | | 3.52 | | | | |
| 1 | <u></u> | 1 | 0 | 0 | | 0 | 0 | | | 0.450 | | 3.60 | | | | |
| 1 | | 1 | 0 | 0 | | 0 | 1 | | | 0.459 | | 3.67 | | | | |
| 1 | | 1 | 0 | 0 | | 1 | 0 | | | 0.469 | | 3.75 | | | | |
| | | 1 | 0 | 0 | | 1 | 1 | | | 0.478 | | 3.82 | | | | |
| - 1 | | 1 | 0 | 1 | | 0 | 0 | | | 0.488 | | 3.90 | | | | |
| 1 | | 1 | 0 | 1 | | 0 | 1 | | | 0.497 | | 3.97 | ' 5 | | | |
| 1 | | 1 | 0 | 1 | | 1 | 0 | | | 0.506 | | 4.05 | 50 | | | |
| 1 | | 1 | 0 | 1 | | 1 | 1 | | | 0.516 | | 4.12 | 25 | | | |
| 1 | | 1 | 1 | 0 | | 0 | 0 | | | 0.525 | | 4.20 | 00 | | | |
| 1 | | 1 | 1 | 0 | | 0 | 1 | | | 0.534 | | 4.27 | ' 5 | | | |
| 1 | | 1 | 1 | 0 | | 1 | 0 | | | 0.544 | | 4.35 | 50 | | | |
| 1 | | 1 | 1 | 0 | | 1 | 1 | | | 0.553 | | 4.42 | 25 | | | |
| 1 | | 1 | 1 | 1 | | 0 | 0 | | | 0.563 | | 4.50 | 00 | | | |
| | | 4 | - | | | • | - | | | 0.570 | | 4 6 7 | - | | | |

1

1

1

1

1

1

4.575

4.650

4.725

0

1

1

1

0

1

0.572

0.581

0.591

1

1

1

1

1

1

Table 12. Function Table for Output Current in case of Constant Current Mode (Channel 5)

| Table 12. F | | e ior Output | | case of Con | stant Curren | t Mode (Channel | 5) | |
|-------------|---------|---------------|---------|-------------|--------------|-----------------|--------------|-------------------------|
| Bit[B] | Bit[A] | Bit[9] | Bit[8] | Bit[7] | Bit[6] | DAC5 Voltage | Rrnf5=0.5Ω | R _{RNF5} =1.0Ω |
| DAC5[5] | DAC5[4] | DAC5[3] | DAC5[2] | DAC5[1] | DAC5[0] | Vdac5 [mV] | Current [mA] | Current [mA] |
| 0 | 0 | 1 | 0 | 1 | 0 | 50 | 96 | 49 |
| 0 | 0 | 1 | 0 | 1 | 1 | 55 | 105 | 54 |
| 0 | 0 | 1 | 1 | 0 | 0 | 60 | 115 | 59 |
| 0 | 0 | 1 | 1 | 0 | 1 | 65 | 125 | 64 |
| 0 | 0 | 1 | 1 | 1 | 0 | 70 | 134 | 68 |
| 0 | 0 | 1 | 1 | 1 | 1 | 75 | 144 | 73 |
| 0 | 1 | 0 | 0 | 0 | 0 | 80 | 153 | 78 |
| 0 | 1 | 0 | 0 | 0 | 1 | 85 | 163 | 83 |
| 0 | 1 | 0 | 0 | 1 | 0 | 90 | 172 | 88 |
| 0 | 1 | 0 | 0 | 1 | 1 | 95 | 182 | 93 |
| 0 | 1 | 0 | 1 | 0 | 0 | 100 | 192 | 98 |
| 0 | 1 | 0 | 1 | 0 | 1 | 105 | 201 | 103 |
| 0 | 1 | 0 | 1 | 1 | 0 | 110 | 211 | 108 |
| 0 | 1 | 0 | 1 | 1 | 1 | 115 | 220 | 113 |
| 0 | 1 | 1 | 0 | 0 | 0 | 120 | 230 | 117 |
| 0 | 1 | 1 | 0 | | 1 | 120 | 230 | 117 |
| | | | | 0 | | | | |
| 0 | 1 | 1 | 0 | 1 | 0 | 130 | 249 | 127 |
| 0 | 1 | 1 | 0 | 1 | 1 | 135 | 259 | 132 |
| 0 | 1 | 1 | 1 | 0 | 0 | 140 | 268 | 137 |
| 0 | 1 | 1 | 1 | 0 | 1 | 145 | 278 | 142 |
| 0 | 1 | 1 | 1 | 1 | 0 | 150 | 287 | 147 |
| 0 | 1 | 1 | 1 | 1 | 1 | 155 | 297 | 152 |
| 1 | 0 | 0 | 0 | 0 | 0 | 160 | 307 | 157 |
| 1 | 0 | 0 | 0 | 0 | | 165 | 316 | 161 |
| 1 | 0 | 0 | 0 | 1 | 0 | 170 | 326 | 166 |
| 1 | 0 | 0 | 0 | 1 | 1 | 175 | 336 | 171 |
| 1 | 0 | 0 | 1 | 0 | 0 | 180 | 345 | 176 |
| 1 | 0 | 0 | 1 | 0 | 1 | 185 | 355 | 181 |
| 1 | 0 | 0 | 1 | 1 | 0 | 190 | 364 | 186 |
| 1 | 0 | 0 | 1 | 1 | 1 | 195 | 374 | 191 |
| 1 | 0 | 1 | 0 | 0 | 0 | 200 | 383 | 196 |
| 1 | 0 | 1 | 0 | 0 | 1 | 205 | 393 | 201 |
| 1 | 0 | 1 | 0 | 1 | 0 | 210 | | 205 |
| 1 | 0 | 1 | 0 | 1 | 1 | 215 | | 210 |
| 1 | 0 | 1 | 1 | 0 | 0 | 220 | | 216 |
| 1 | 0 | 1.7 | 1 | 0 | 1 | 225 | | 220 |
| 1 | 0 | | 1 | | 0 | 230 | | 225 |
| 1 | 0 | 1 | 1 | 1 | 1 | 235 | | 230 |
| 1 | 1 | 0 | 0 | 0 | 0 | 240 | | 235 |
| 1 | 1 | 0 | 0 | 0 | 1 | 245 | | 240 |
| 1 | 1 | 0 | 0 | 1 | 0 | 250 | | 245 |
| 1 | 1 | 0 | 0 | 1 | 1 | 255 | | 250 |
| 1 | 1 | 0 | 1 | 0 | 0 | 260 | Over | 254 |
| | 1 | 0 | 1 | 0 | 1 | 265 | Operating | 259 |
| 1 | 1 | 0 | 1 | 1 | 0 | 270 | Condition | 264 |
| | 1 | 0 | 1 | 1 | 1 | 275 | | 269 |
| 1 | 1 | 1 | 0 | 0 | 0 | 280 | | 274 |
| 1 | 1 | 1 | 0 | 0 | 1 | 285 | | 274 |
| 1 | 1 | 1 | 0 | 1 | 0 | 290 | | 284 |
| 1 | 1 | 1 | 0 | 1 | 1 | 290 | | 289 |
| 1 | 1 | | | 0 | 0 | | | |
| 1 | 1 | <u>1</u> 1 | 1 | | 1 | 300 305 | | 294 298 |
| | | | | 0 | | | | |
| 1 | 1 | 1 | 1 | 1 | 0 | 310 | | 303 |
| 1 | 1 | 1 | 1 | 1 | 1 | 315 | | 308 |

Table 13. DATA BIT MAP [011]

| | - | | 011] | | DATA | A BIT | | | | | |
|----------|-----------|---------------|----------|---------------------|--------------------------|--------------|--------------|--------------------------|--------------|--------------|--------------|
| ADR. | Bit[l | B] Bit[A] | Bit[9] | Bit[8] Bit[| 7] Bit[6] | Bit[5] | Bit[4] | Bit[3] | Bit[2] | Bit[1] | Bit[0] |
| 011 | DA V4[| | | DAC DA V4[2] V4[| | DAC 14[5] | DAC I4[4] | DAC 14[3] | DAC 14[2] | DAC I4[1] | DAC I4[0] |
| | | -1 1 | 6-3 | | | r - 1 | | L-J | | | |
| Table 14 | 1 | otion Toble f | | ana in anan | of Constant V/ | ltogo Mode | Chan | nol 1) | | | |
| Bit[B | | Bit[A] | Bit[9] | Bit[8] | of Constant Vo Bit[7] | Bit[6] | | ACV4 Volt | 200 | Output | High |
| DACV4 | | DACV4[4] | DACV4[3] | DACV4[2] | DACV4[1] | DACV4[0 | | VDACV4 VOII VDACV4 [V | | Voltage; | |
| 0 | .[-] | 1 | 0 | 1 | 0 | 0 | | 0.188 | , | 1.50 | |
| 0 | | 1 | 0 | 1 | 0 | 1 | | 0.197 | | 1.57 | |
| 0 | | 1 | 0 | 1 | 1 | 0 | | 0.206 | | 1.65 | |
| 0 | | 1 | 0 | 1 | 1 | 1 | | 0.216 | | 1.72 | |
| 0 | | 1 | 1 | 0 | 0 | 0 | | 0.225 | | 1.80 | 00 |
| 0 | | 1 | 1 | 0 | 0 | 1 | | 0.234 | | 1.87 | ' 5 |
| 0 | | 1 | 1 | 0 | 1 | 0 | | 0.244 | | 1.95 | 50 |
| 0 | | 1 | 1 | 0 | 1 | 1 | | 0.253 | | 2.02 | 25 |
| 0 | | 1 | 1 | 1 | 0 | 0 | | 0.263 | | 2.10 | 00 |
| 0 | | 1 | 1 | 1 | 0 | 1 | | 0.272 | | 2.17 | 75 |
| 0 | | 1 | 1 | 1 | 1 | 0 | | 0.281 | | 2.25 | 50 |
| 0 | | 1 | 1 | 1 | 1 | | | 0.291 | | 2.32 | 25 |
| 1 | | 0 | 0 | 0 | 0 | 0 | | 0.300 | | 2.40 | 00 |
| 1 | | 0 | 0 | 0 | 0 | 1 | | 0.309 | | 2.47 | ′ 5 |
| 1 | | 0 | 0 | 0 | | 0 | | 0.319 | | 2.55 | 50 |
| 1 | | 0 | 0 | 0 | 1 | 1 | | 0.328 | | 2.62 | |
| 1 | | 0 | 0 | 1 | 0 | 0 | | 0.338 | | 2.70 | |
| 1 | | 0 | 0 | 1 | 0 | | | 0.347 | | 2.77 | |
| 1 | | 0 | 0 | 1 | 1 | 0 | | 0.356 | | 2.85 | |
| 1 | | 0 | 0 | | 1 | | | 0.366 | | 2.92 | |
| 1 | | 0 | 1 | 0 | 0 | 0 | | 0.375 | | 3.00 | |
| 1 | | 0 | 1 | 0 | 0 | 1 | | 0.384 | | 3.07 | |
| 1 | | 0 | 1 | 0 | 1 | 0 | | 0.394 | | 3.15 | |
| 1 | | 0 | | 0 | 1 | 1 | | 0.403 | | 3.22 | |
| 1 | | 0 | | 1 | 0 | 0 | | 0.413 | | 3.30 | |
| 1 | | 0 | 1 | | 0 | 1 | | 0.422 | | 3.37 | |
| 1 | | 0 | 1 | | 1 | 0 | | 0.431 | | 3.45 | |
| 1 | | 0 | 1 | | 1 | 1 | | 0.441 | | 3.52 | |
| 1 | | 1 | 0 | 0 | 0 | 0 | _ | 0.450 | | 3.60 | |
| 1 | | | | 0 | 0 | 1 | _ | 0.459 | | 3.67 | |
| | 5 | 1 | 0 | 0 | 1 | 0 | _ | 0.469 | | 3.75 | |
| | | 1 | 0 | 0 | 1 0 | 1 | | 0.478 | | 3.82 | |
| | | 1 1 | 0 | 1 | 0 | 0 | | 0.488 | | 3.90 3.97 | |
| 1 | | 1 | 0 | 1 | 0 | 1 0 | | 0.497 | | 4.05 | |
| 1 | | 1 | 0 | 1 | 1 | 1 | | 0.506 | | 4.05 | |
| 1 | | 1 | 1 | 0 | 0 | 0 | | 0.516 | | 4.12 | |
| 1 | | 1 | 1 | 0 | 0 | 1 | | 0.525 | | 4.20 | |
| 1 | | 1 | 1 | 0 | 1 | 0 | | 0.544 | | 4.27 | |
| 1 | | 1 | 1 | 0 | 1 | 1 | | 0.553 | | 4.30 | |
| 1 | | 1 | 1 | 1 | 0 | 0 | | 0.563 | | 4.50 | |
| 1 | -+ | 1 | 1 | 1 | 0 | 1 | | 0.572 | | 4.57 | |
| 1 | -+ | 1 | 1 | 1 | 1 | 0 | | 0.581 | | 4.65 | |
| 1 | -+ | 1 | 1 | 1 | 1 | 1 | | 0.591 | | 4.72 | |
| | | I | I | I | 1 | 1 | | 0.001 | | 4.72 | |

Table 15. Function Table for Output Current in case of Constant Current Mode (Channel 4)

| Table 15. Fu | inction Table | e for Output | Current in c | case of Cons | stant Curren | t Mode (Channel | 4) | |
|--------------|---------------|--------------|--------------|--------------|--------------|-------------------------|--------------|--------------------------|
| Bit[5] | Bit[4] | Bit[3] | Bit[2] | Bit[1] | Bit[0] | DACI4 Voltage | Rrnfi4=0.5Ω | R _{RNFI4} =1.0Ω |
| DACI4[5] | DACI4[4] | DACI4[3] | DACI4[2] | DACI4[1] | DACI4[0] | V _{DACI4} [mV] | Current [mA] | Current [mA] |
| 0 | 0 | 1 | 0 | 1 | 0 | 50 | 99 | 50 |
| 0 | 0 | 1 | 0 | 1 | 1 | 55 | 109 | 55 |
| 0 | 0 | 1 | 1 | 0 | 0 | 60 | 119 | 60 |
| 0 | 0 | 1 | 1 | 0 | 1 | 65 | 129 | 65 |
| | | | | | | | | |
| 0 | 0 | 1 | 1 | 1 | 0 | 70 | 139 | 70 |
| 0 | 0 | 1 | 1 | 1 | 1 | 75 | 149 | 75 |
| 0 | 1 | 0 | 0 | 0 | 0 | 80 | 159 | 80 |
| 0 | 1 | 0 | 0 | 0 | 1 | 85 | 169 | 85 |
| 0 | 1 | 0 | 0 | 1 | 0 | 90 | 179 | 90 |
| 0 | 1 | 0 | 0 | 1 | 1 | 95 | 188 | 95 |
| 0 | 1 | 0 | 1 | 0 | 0 | 100 | 198 | 100 |
| 0 | 1 | 0 | 1 | 0 | 1 | 105 | 208 | 105 |
| 0 | 1 | 0 | 1 | 1 | 0 | 110 | 218 | 110 |
| 0 | 1 | 0 | 1 | 1 | 1 | 115 | 228 | 115 |
| 0 | 1 | 1 | 0 | 0 | 0 | 120 | 238 | 120 |
| 0 | 1 | 1 | 0 | 0 | 1 | 125 | 248 | 125 |
| 0 | 1 | 1 | 0 | 1 | 0 | 130 | 258 | 129 |
| 0 | 1 | 1 | 0 | 1 | 1 | 135 | 268 | 134 |
| 0 | 1 | 1 | 1 | 0 | 0 | 140 | 278 | 139 |
| 0 | 1 | 1 | 1 | 0 | 1 | 145 | 288 | 144 |
| 0 | 1 | 1 | 1 | 1 | 0 | 150 | 298 | 149 |
| 0 | 1 | 1 | 1 | 1 | 1 | 155 | 308 | 154 |
| 1 | 0 | 0 | 0 | 0 | 0 | 160 | 317 | 159 |
| 1 | 0 | 0 | 0 | 0 | 1 | 165 | 327 | 164 |
| 1 | 0 | 0 | 0 | 1 | 0 | 170 | 337 | 169 |
| 1 | 0 | 0 | 0 | 1 | 1 | 175 | 347 | 174 |
| 1 | 0 | 0 | 1 | 0 | 0 | 180 | 357 | 174 |
| 1 | 0 | 0 | 1 | 0 | 1 | 185 | 367 | 184 |
| 1 | 0 | 0 | 1 | | | 190 | 377 | 189 |
| | | 0 | | | 0 | 190 | 387 | 109 |
| 1 | 0 | | 1 | | | | | |
| 1 | 0 | 1 | 0 | 0 | 0 | 200 | 397 | 199 |
| 1 | 0 | 1 | 0 | 0 | | 205 | | 204 |
| 1 | 0 | 1 | 0 | 1 | 0 | 210 | | 209 |
| 1 | 0 | 1 | 0 | 1 | 1 | 215 | | 214 |
| 1 | 0 | 1 | 1 | 0 | 0 | 220 | | 219 |
| 1 | 0 | 1 | 1 | 0 | 1 | 225 | | 224 |
| 1 | 0 | 1 | 1 | | 0 | 230 | | 229 |
| 1 | 0 | 1 | 1 | | 1 | 235 | | 234 |
| 1 | 1 | 0 | 0 | 0 | 0 | 240 | | 239 |
| 1 | 1 | 0 | 0 | 0 | 1 | 245 | | 244 |
| 1 | 1 | 0 | 0 | 1 | 0 | 250 | | 249 |
| 1 | 1 | 0 | 0 | 1 | 1 | 255 | Over | 254 |
| 1 | 4 | | 1 | 0 | | 260 | | 259 |
| 1 | | 0 | | | 0 | | Operating | |
| | 1 | 0 | 1 | 0 | 1 | 265 | Condition | 264 |
| | 1 | 0 | 1 | 1 | 0 | 270 | | 269 |
| 1 | 1 | 0 | 1 | 1 | 1 | 275 | | 274 |
| 1 | 1 | 1 | 0 | 0 | 0 | 280 | | 279 |
| 1 | 1 | 1 | 0 | 0 | 1 | 285 | | 284 |
| 1 | 1 | 1 | 0 | 1 | 0 | 290 | | 289 |
| 1 | 1 | 1 | 0 | 1 | 1 | 295 | | 294 |
| 1 | 1 | 1 | 1 | 0 | 0 | 300 | | 299 |
| 1 | 1 | 1 | 1 | 0 | 1 | 305 | | 304 |
| 1 | 1 | 1 | 1 | 1 | 0 | 310 | | 309 |
| 1 | 1 | 1 | 1 | 1 | 1 | 315 | | 314 |
| | 1 | 1 | | I | I | 315 | | 314 |

| Table 16 | . DATA BI | T MAP [10 | 20] | | | | | | | | | |
|------------|------------------|------------------|-------------|--------|--------|--------|-------|----------|--------|--------|-----------|-----------------------|
| ADR. | | | | | | DATA | BIT | | | | | |
| ADK. | Bit[B] | Bit[A] | Bit[9] | Bit[8] | Bit[7] | Bit[6] | Bit[5 |] Bit[4] | Bit[3] | Bit[2] | Bit[1] | Bit[0] |
| 100 | TEST (Note 8) | TEST (Note 8) | IN5B | IN5A | IN4B | IN4A | IN3E | 3 IN3A | IN2B | IN2A | IN1B | IN1A |
| (Note 8) M | ust be held a | t 0 (GND) | | | | | | k | | | | |
| | | | | | | | | | | | | |
| Table 17 | . I/O Truth | n Table (Cl | hannel 1) | | | | | | | | | |
| | | Serial Int | erface Bit | | | INPU | Г | | O | JTPUT | | • |
| MODE 23 | MODE 13 | MODE 12B | MODE 12A | IN1B | IN1A | INPUT | 1 | OUT1A | OUT1 | 3 Q | utput Mod | e ^(Note 9) |
| PWM D | Prive Mode | e via INPL | JT1 Pin | | | | | | | | | |
| 0 | 0 | 0 | 0 | 0 | 0 | Х | | Z | Z | | Open | |
| 0 | 0 | 0 | 0 | 0 | 1 | L | | L | 4 | | Short Br | ake |
| 0 | 0 | 0 | 0 | 0 | 1 | Н | | H | | | CW | |
| 0 | 0 | 0 | 0 | 1 | 0 | L | | L | Ľ | | Short Br | |
| 0 | 0 | 0 | 0 | 1 | 0 | Н | | L | Н | | CCW | |
| 0 | 0 | 0 | 0 | 1 | 1 | Х | | L | L | | Short Br | ake |
| PWM D | Prive Mode | e via INPL | JT1 Pin | | | | | | | | | |
| 0 | 0 | 0 | 1 | 0 | 0 | Х | | Z | Z | | Open | l |
| 0 | 0 | 0 | 1 | 0 | 1 | L | | Н | L | | CW | |
| 0 | 0 | 0 | 1 | 0 | 1 | Н | | L | | | Short Br | |
| 0 | 0 | 0 | 1 | 1 | 0 | - | | L | H | | CCW | |
| 0 | 0 | 0 | 1 | 1 | 0 | H | | Ļ | | | Short Br | ake |
| 0 | 0 | 0 | 1 | 1 | 1 | X | | L | | | Short Br | ake |
| CW / C | CW Drive | Mode via | INPUT1 | | | | | | | | | |
| 0 | 0 | 1 | 0 | Х | 0 | Х | | Z | Z | | Open | l |
| 0 | 0 | 1 | 0 | 0 | 1 | L | | | Н | | CCW | |
| 0 | 0 | 1 | 0 | 0 | | Н | | Н | L | | CW | |
| 0 | 0 | 1 | 0 | | | X | | L | L | | Short Br | ake |
| CW / C | CW Drive | Mode via | INPUT1 | | | | | | | | | |
| 0 | 0 | 1 | 1 | X | 0 | Х | | Z | Z | | Open | |
| 0 | 0 | 1 | 1 | 0 | 1 | | | Н | L | | CW | |
| 0 | 0 | 1 | 1 | 0 | 1 | Н | | L | Н | | CCW | |
| 0 | 0 | 1 | | 1 | 1 | Х | | L | L | | Short Br | ake |

ROL

L: Low, H: High, X: Don't care, Z: Hi impedance (Note 9) CW: Current flows from OUT1A to OUT1B, CCW: Current flows from OUT1B to OUT1A

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Table 18. I/O Truth Table (Channel 2)

| | | Serial Int | erface Bit | | | INPUT | | OUTP | UT |
|------------|------------|-------------|-------------|------|------|--------|-------|-------|-----------------------|
| MODE 23 | MODE 13 | MODE 12B | MODE 12A | IN2B | IN2A | INPUT2 | OUT2A | OUT2B | Output Mode (Note 10) |
| PWM D | rive Mode | via INPU | JT2 Pin | | | • | • | | |
| 0 | 0 | 0 | 0 | 0 | 0 | Х | Z | Z | Open |
| 0 | 0 | 0 | 0 | 0 | 1 | L | L | L | Short Brake |
| 0 | 0 | 0 | 0 | 0 | 1 | Н | Н | L | CW |
| 0 | 0 | 0 | 0 | 1 | 0 | L | L | L | Short Brake |
| 0 | 0 | 0 | 0 | 1 | 0 | Н | L | Н | CCW |
| 0 | 0 | 0 | 0 | 1 | 1 | Х | L | L | Short Brake |
| PWM D | rive Mode | e via INPU | IT2 Pin | | | | | | |
| 0 | 0 | 0 | 1 | 0 | 0 | Х | Z | Z | Open |
| 0 | 0 | 0 | 1 | 0 | 1 | L | Н | Ļ | CW |
| 0 | 0 | 0 | 1 | 0 | 1 | Н | L | LON | Short Brake |
| 0 | 0 | 0 | 1 | 1 | 0 | L | L | H | CCW |
| 0 | 0 | 0 | 1 | 1 | 0 | Н | L | L | Short Brake |
| 0 | 0 | 0 | 1 | 1 | 1 | Х | L | L | Short Brake |
| CW / CO | CW Drive | Mode via | INPUT2 | Pin | | | | | |
| 0 | 0 | 1 | 0 | Х | 0 | Х | Z | Z | Open |
| 0 | 0 | 1 | 0 | 0 | 1 | L | L | н | CCW |
| 0 | 0 | 1 | 0 | 0 | 1 | Н | H | L | CW |
| 0 | 0 | 1 | 0 | 1 | 1 | X | L | L | Short Brake |
| CW / CO | CW Drive | Mode via | INPUT2 | Pin | | | | | - |
| 0 | 0 | 1 | 1 | Х | 0 | X | Z | Z | Open |
| 0 | 0 | 1 | 1 | 0 | 1 | | H | | CW |
| 0 | 0 | 1 | 1 | 0 | 1 | Н | L | Н | CCW |
| 0 | 0 | 1 | 1 | 1 | 1 | Х | | L | Short Brake |
| | PUL V D | | | | | | | | |

L: Low, H: High, X: Don't care, Z: Hi impedance (Note 10) CW: Current flows from OUT2A to OUT2B, CCW: Current flows from OUT2B to OUT2

Table 19. I/O Truth Table (Channel 3)

| | | | erface Bit | | | INPUT | | OUTPUT | | | |
|------------|------------|------------|------------|------|------|---------|-------|--------|-----------------------|--|--|
| MODE 34 | MODE 23 | MODE 3B | MODE 3A | ІΝЗВ | IN3A | INPUT34 | OUT3A | OUT3B | Output Mode (Note 11) | | |
| PWM D | rive Mode | via INPU | JT34 Pin | | | | | | | | |
| 0 | 0 | 0 | 0 | 0 | 0 | Х | Z | Z | Open | | |
| 0 | 0 | 0 | 0 | 0 | | L | L | L | Short Brake | | |
| 0 | 0 | 0 | 0 | 0 | | Н | Н | L | CW | | |
| 0 | 0 | 0 | 0 | 1 | 0 | L | L | L | Short Brake | | |
| 0 | 0 | 0 | 0 | 1 | 0 | Н | L | Н | CCW | | |
| 0 | 0 | Ō | 0 | 1 | 1 | Х | L | L | Short Brake | | |
| PWM D | rive Mode | e via INPU | JT34 Pin | | | | | | | | |
| 0 | 0 | 0 | 1 | 0 | 0 | Х | Z | Z | Open | | |
| 0 | 0 | 0 | 1 | 0 | 1 | L | Н | L | CW | | |
| 0 | 0 | 0 | 1 | 0 | 1 | Н | L | L | Short Brake | | |
| 0 | 0 | 0 | 1 | 1 | 0 | L | L | Н | CCW | | |
| 0 | 0 | 0 | 1 | 1 | 0 | Н | L | L | Short Brake | | |
| 0 | 0 | 0 | 1 | 1 | 1 | Х | L | L | Short Brake | | |
| CW / CO | CW Drive | Mode via | INPUT34 | Pin | | | | | | | |
| 0 | 0 | 1 | 0 | Х | 0 | Х | Z | Z | Open | | |
| 0 | 0 | 1 | 0 | 0 | 1 | L | L | Н | CCW | | |
| 0 | 0 | 1 | 0 | 0 | 1 | Н | Н | L | CW | | |
| 0 | 0 | 1 | 0 | 1 | 1 | Х | L | L | Short Brake | | |
| CW / CO | CW Drive | Mode via | INPUT34 | Pin | | | | | | | |
| 0 | 0 | 1 | 1 | Х | 0 | Х | Z | Z | Open | | |
| 0 | 0 | 1 | 1 | 0 | 1 | L | Н | L | ĊW | | |
| 0 | 0 | 1 | 1 | 0 | 1 | Н | L | Н | CCW | | |
| 0 | 0 | 1 | 1 | 1 | 1 | Х | L | L | Short Brake | | |

L: Low, H: High, X: Don't care, Z: Hi impedance

(Note 11) CW: Current flows from OUT3A to OUT3B, CCW: Current flows from OUT3B to OUT3A

| | | | | into mout | | 1/(0010/() | 0 | | |
|------------|-------------|--------------|-------------|-----------|------|------------|-------|-------|-----------------------|
| | | Serial Int | erface Bit | | | INPUT | | OUTP | UT |
| MODE 23 | MODE 13 | MODE 12B | MODE 12A | IN1B | IN1A | INPUT1 | OUT1A | OUT3A | Output Mode (Note 12) |
| PWM D | rive Mode | via INPU | T1 Pin | | | | | | |
| ANY | 1 | 0 | 0 | 0 | 0 | Х | Z | Z | Open |
| ANY | 1 | 0 | 0 | 0 | 1 | L | L | L | Short Brake |
| ANY | 1 | 0 | 0 | 0 | 1 | Н | Н | L | CW |
| ANY | 1 | 0 | 0 | 1 | 0 | L | L | L | Short Brake |
| ANY | 1 | 0 | 0 | 1 | 0 | Н | L | Н | CCW |
| ANY | 1 | 0 | 0 | 1 | 1 | Х | L | L | Short Brake |
| PWM D | rive Mode | via INPU | T1 Pin | | | • | | | |
| ANY | 1 | 0 | 1 | 0 | 0 | Х | Z | Z | Open |
| ANY | 1 | 0 | 1 | 0 | 1 | L | Н | L | ĊW |
| ANY | 1 | 0 | 1 | 0 | 1 | Н | L | LON | Short Brake |
| ANY | 1 | 0 | 1 | 1 | 0 | L | L | H | CCW |
| ANY | 1 | 0 | 1 | 1 | 0 | Н | L | L | Short Brake |
| ANY | 1 | 0 | 1 | 1 | 1 | Х | L | L | Short Brake |
| CW / CO | CW Drive | Mode via | INPUT1 | Pin | | | | | |
| ANY | 1 | 1 | 0 | Х | 0 | Х | Z | Z | Open |
| ANY | 1 | 1 | 0 | 0 | 1 | L | | н | CCW |
| ANY | 1 | 1 | 0 | 0 | 1 | Н | H | L | CW |
| ANY | 1 | 1 | 0 | 1 | 1 | Х | L | Ĺ | Short Brake |
| CW / CO | CW Drive | Mode via | INPUT1 | Pin | | | | | |
| ANY | 1 | 1 | 1 | Х | 0 | X | Z | Z | Open |
| ANY | 1 | 1 | 1 | 0 | 1 | | H | | ĊW |
| ANY | 1 | 1 | 1 | 0 | 1 | Н | L | Н | CCW |
| ANY | 1 | 1 | 1 | 1 | 1 | X | | L | Short Brake |
| | ligh V. Dan | t care 7. Hi | impodopoo | | | | | | |

L: Low, H: High, X: Don't care, Z: Hi impedance (Note 12) CW: Current flows from OUT1A to OUT3A, CCW: Current flows from OUT3A to OUT1A.

Table 21. I/O Truth Table (Exclusive Drive Mode for OUT2A-OUT3B)

| | | Serial Int | erface Bit | | | INPUT | | OUTP | UT |
|------------|------------|-------------|-------------|------|------|--------|-------|-------|-----------------------|
| MODE 23 | MODE 13 | MODE 12B | MODE 12A | IN2B | IN2A | INPUT2 | OUT2A | OUT3B | Output Mode (Note 13) |
| PWM D | rive Mode | via INPU | IT2 Pin | | | | | | · |
| 1 | ANY | 0 | 0 | 0 | 0 | Х | Z | Z | Open |
| 1 | ANY | 0 | 0 | 0 | | L | L | L | Short Brake |
| 1 | ANY | 0 | 0 | 0 | | Н | Н | L | CW |
| 1 | ANY | 0 | 0 | 1 | 0 | L | L | L | Short Brake |
| 1 | ANY | 0 | 0 | | 0 | Н | L | Н | CCW |
| 1 | ANY | 0 | 0 | 1 | 1 | Х | L | L | Short Brake |
| PWM D | rive Mode | via INPU | IT2 Pin | | | | | | |
| 1 | ANY | 0 | 1 | 0 | 0 | Х | Z | Z | Open |
| 1 | ANY | 0 | 1 | 0 | 1 | L | Н | L | CW |
| | ANY | 0 | 1 | 0 | 1 | Н | L | L | Short Brake |
| 1 | ANY | 0 | 1 | 1 | 0 | L | L | Н | CCW |
| | ANY | 0 | 1 | 1 | 0 | Н | L | L | Short Brake |
| 1 | ANY | 0 | 1 | 1 | 1 | Х | L | L | Short Brake |
| CW / CO | CW Drive | Mode via | INPUT2 | Pin | | | | | |
| 1 | ANY | 1 | 0 | Х | 0 | Х | Z | Z | Open |
| 1 | ANY | 1 | 0 | 0 | 1 | L | L | Н | CCW |
| 1 | ANY | 1 | 0 | 0 | 1 | Н | Н | L | CW |
| 1 | ANY | 1 | 0 | 1 | 1 | Х | L | L | Short Brake |
| CW / CO | CW Drive | Mode via | INPUT2 | Pin | | | | | |
| 1 | ANY | 1 | 1 | Х | 0 | Х | Z | Z | Open |
| 1 | ANY | 1 | 1 | 0 | 1 | L | Н | L | ĊW |
| 1 | ANY | 1 | 1 | 0 | 1 | Н | L | Н | CCW |
| 1 | ANY | 1 | 1 | 1 | 1 | Х | L | L | Short Brake |

L: Low, H: High, X: Don't care, Z: Hi impedance (Note 13) CW: Current flows from OUT2A to OUT3B, CCW: Current flows from OUT3B to OUT2A

Table 22. I/O Truth Table (Channel 4, Driving via INPUT34 pin)

| 45 34 4B 4A PWM Drive Mode via INPUT34 Pin 0 0 0 1 0 0 0 1 0 0 0 1 0 0 0 1 0 0 0 1 0 0 0 1 0 0 0 1 0 0 0 1 0 0 PWM Drive Mode via INPUT34 Pin 0 1 0 1 0 1 0 1 0 1 0 1 0 1 | 4B IN4A 0 0 0 1 0 1 1 0 1 0 | X L H | OUT4A Z L | OUT4B | Output Mode ^(Note 14) |
|---|--|-------------|-----------------|-------|----------------------------------|
| 0 1 0 0 0 1 0 0 1 0 1 0 0 1 0 1 0 0 1 0 1 0 0 1 0 1 0 0 1 0 1 0 1 1 0 1 0 1 1 0 1 0 1 1 0 1 0 1 1 0 1 0 1 1 | 0 1 0 1 1 0 | L | L | Z | |
| 0 1 0 0 0 1 0 0 0 1 0 0 0 1 0 0 0 1 0 0 0 1 0 0 0 1 0 0 PWM Drive Mode via INPUT34 Pin 0 1 0 1 0 1 0 1 0 1 0 1 0 1 | 0 1 0 1 1 0 | L | L | Z | |
| 0 1 0 0 0 1 0 0 0 1 0 0 0 1 0 0 0 1 0 0 0 1 0 0 PWM Drive Mode via INPUT34 Pin 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 | 0 1 1 0 | | L | | |
| 0 1 0 0 0 1 0 0 0 1 0 0 PWM Drive Mode via INPUT34 Pin 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 | 1 0 | | 11 | - | Short Brake |
| 0 1 0 0 0 1 0 0 PWM Drive Mode via INPUT34 Pin 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 | - | | Н | L | CW |
| 0 1 0 0 PWM Drive Mode via INPUT34 Pin 0 1 0 0 1 0 1 0 0 1 0 1 0 0 1 0 1 0 0 1 0 1 0 | 1 0 | L | L | L | Short Brake |
| PWM Drive Mode via INPUT34 Pin 0 1 0 1 0 1 0 1 0 0 1 0 1 0 0 1 0 1 0 | . 0 | Н | L | Н | CCW |
| 0 1 0 1 0 1 0 1 0 0 1 0 1 0 | 1 1 | Х | L | L | Short Brake |
| 0 1 0 1 0 1 0 1 | | | | | |
| 0 1 0 1 | 0 0 | Х | Z | Z | Open |
| | 0 1 | L | Н | Ļ | CW |
| 0 1 0 1 | 0 1 | Н | L | L | Short Brake |
| | 1 0 | L | L | H | CCW |
| 0 1 0 1 | 1 0 | Н | L | | Short Brake |
| 0 1 0 1 | 1 1 | Х | L | L | Short Brake |
| CW / CCW Drive Mode via INPUT34 Pin | | | | | |
| 0 1 1 0 | X 0 | Х | Z | Z | Open |
| 0 1 1 0 | 0 1 | L | | Н | CCW |
| 0 1 1 0 | 0 1 | Н | Н | L | CW |
| 0 1 1 0 | 1 1 | Х | L | | Short Brake |
| CW / CCW Drive Mode via INPUT34 Pin | | | | | Þ |
| 0 1 1 1 1 | X 0 | Х | Z | Z | Open |
| 0 1 1 1 | 0 1 | 4 | H | | ĊW |
| 0 1 1 1 | 0 1 | Н | L | Н | CCW |
| 0 1 1 1 | ~ ' | X | | | Short Brake |

L: Low, H: High, X: Don't care, Z: Hi impedance (Note 14) CW: Current flows from OUT4A to OUT4B, CCW: Current flows from OUT4B to OUT4A

Table 23. I/O Truth Table (Channel 4, Driving via INPUT45 pin)

| | | Serial Int | erface Bit | | | INPUT | | OUTP | UT |
|------------|------------|------------|------------|-------|------|---------|-------|-------|-----------------------|
| MODE 45 | MODE 34 | MODE 4B | MODE 4A | IN4B | IN4A | INPUT45 | OUT4A | OUT4B | Output Mode (Note 15) |
| PWM D | rive Mode | via INPL | T45 Pin | | | | | | |
| 0 | 0 | 0 | 0 | 0 | 0 | Х | Z | Z | Open |
| 0 | 0 | 0 | 0 | 0 | | L | L | L | Short Brake |
| 0 | 0 | | 0 | 0 | Ì | Н | Н | L | CW |
| 0 | 0 | 0 | 0 | 1 | 0 | L | L | L | Short Brake |
| 0 | 0 | 0 | 0 | 1 | 0 | Н | L | Н | CCW |
| 0 | 0 | 0 | 0 | 1 | 1 | Х | L | L | Short Brake |
| PWM D | rive Mode | via INPL | JT45 Pin | | | | | | |
| 0 | 0 | 0 | 1 | Õ | 0 | Х | Z | Z | Open |
| 0 | 0 | 0 | 1 | 0 | 1 | L | Н | L | CW |
| 0 | 0 | 0 | 1 | 0 | 1 | Н | L | L | Short Brake |
| 0 | 0 | 0 | 1 | 1 | 0 | L | L | Н | CCW |
| 0 | 0 | 0 | 1 | 1 | 0 | Н | L | L | Short Brake |
| 0 | 0 | 0 | 1 | 1 | 1 | Х | L | L | Short Brake |
| CW / CO | CW Drive | Mode via | INPUT45 | i Pin | | | | | |
| 0 | 0 | 1 | 0 | Х | 0 | Х | Z | Z | Open |
| 0 | 0 | 1 | 0 | 0 | 1 | L | L | Н | CCW |
| 0 | 0 | 1 | 0 | 0 | 1 | Н | Н | L | CW |
| 0 | 0 | 1 | 0 | 1 | 1 | Х | L | L | Short Brake |
| CW / CO | CW Drive | Mode via | INPUT45 | i Pin | | | | | |
| 0 | 0 | 1 | 1 | Х | 0 | Х | Z | Z | Open |
| 0 | 0 | 1 | 1 | 0 | 1 | L | Н | L | ĊW |
| 0 | 0 | 1 | 1 | 0 | 1 | Н | L | Н | CCW |
| 0 | 0 | 1 | 1 | 1 | 1 | Х | L | L | Short Brake |

L: Low, H: High, X: Don't care, Z: Hi impedance

(Note 15) CW: Current flows from OUT4A to OUT4B, CCW: Current flows from OUT4B to OUT4A

Table 24. I/O Truth Table (Channel 5)

| | | Serial Int | erface Bit | | | INPUT | | OUTP | UT |
|------------|-------------|--------------|------------|-------|------|---------|-------|-------|-----------------------|
| MODE 45 | MODE 34 | MODE 5B | MODE 5A | IN5B | IN5A | INPUT45 | OUT5A | OUT5B | Output Mode (Note 16) |
| PWM D | rive Mode | via INPL | JT45 Pin | | | | | | |
| 0 | 1 | 0 | 0 | 0 | 0 | Х | Z | Z | Open |
| 0 | 1 | 0 | 0 | 0 | 1 | L | L | L | Short Brake |
| 0 | 1 | 0 | 0 | 0 | 1 | Н | Н | L | CW |
| 0 | 1 | 0 | 0 | 1 | 0 | L | L | L | Short Brake |
| 0 | 1 | 0 | 0 | 1 | 0 | Н | L | Н | CCW |
| 0 | 1 | 0 | 0 | 1 | 1 | Х | L | L | Short Brake |
| PWM D | rive Mode | via INPL | JT45 Pin | | | | | | |
| 0 | 1 | 0 | 1 | 0 | 0 | Х | Z | Z | Open |
| 0 | 1 | 0 | 1 | 0 | 1 | L | Н | Ļ | ĊW |
| 0 | 1 | 0 | 1 | 0 | 1 | Н | L | | Short Brake |
| 0 | 1 | 0 | 1 | 1 | 0 | L | L | H | CCW |
| 0 | 1 | 0 | 1 | 1 | 0 | Н | L | | Short Brake |
| 0 | 1 | 0 | 1 | 1 | 1 | Х | L | L | Short Brake |
| CW / CO | CW Drive | Mode via | INPUT45 | Pin | | • | | | |
| 0 | 1 | 1 | 0 | Х | 0 | Х | Z | Z | Open |
| 0 | 1 | 1 | 0 | 0 | 1 | L | | Н | CCW |
| 0 | 1 | 1 | 0 | 0 | 1 | Н | H | L | CW |
| 0 | 1 | 1 | 0 | 1 | 1 | Х | L | Ļ | Short Brake |
| CW / CO | CW Drive | Mode via | INPUT45 | i Pin | | | | | |
| 0 | 1 | 1 | 1 | Х | 0 | Х | Z | Z | Open |
| 0 | 1 | 1 | 1 | 0 | 1 | | H | | ĊW |
| 0 | 1 | 1 | 1 | 0 | 1 | Н | L | Н | CCW |
| 0 | 1 | 1 | 1 | 1 | 1 | X | | | Short Brake |
| | ligh V. Don | t care 7. Hi | impodopoo | | | | | | |

L: Low, H: High, X: Don't care, Z: Hi impedance (Note 16) CW: Current flows from OUT5A to OUT5B, CCW: Current flows from OUT5B to OUT5A

Table 25. I/O Truth Table (Channel 5)

| | | | erface Bit | | | INPUT | | OUTP | UT |
|------------|------------|------------|------------|-------|------|---------|-------|-------|-----------------------|
| MODE 45 | MODE 34 | MODE 5B | MODE 5A | IN5B | IN5A | INPUT45 | OUT5A | OUT5B | Output Mode (Note 17) |
| PWM D | rive Mode | via INPU | IT45 Pin | | | | | | • |
| 1 | 0 | 0 | 0 | 0 | 0 | Х | Z | Z | Open |
| 1 | 0 | 0 | 0 | 0 | | L | L | L | Short Brake |
| 1 | 0 | 0 | 0 | 0 | | Н | Н | L | CW |
| 1 | 0 | 0 | 0 | 1 | 0 | L | L | L | Short Brake |
| 1 | 0 | 0 | 0 | 1 | 0 | Н | L | Н | CCW |
| 1 | 0 | 0 | 0 | 1 | 1 | Х | L | L | Short Brake |
| PWM D | rive Mode | via INPU | JT45 Pin | | | | | | |
| 1 | 0 | 0 | 1 | Ō | 0 | Х | Z | Z | Open |
| _ 1 | 0 | 0 | 1 | 0 | 1 | L | Н | L | ĊW |
| | 0 | 0 | 1 | 0 | 1 | Н | L | L | Short Brake |
| 1 | 0 | 0 | 1 | 1 | 0 | L | L | Н | CCW |
| 1 | 0 | 0 | 1 | 1 | 0 | Н | L | L | Short Brake |
| 1 | 0 | 0 | 1 | 1 | 1 | Х | L | L | Short Brake |
| CW / CO | CW Drive | Mode via | INPUT45 | Pin | | | | | |
| 1 | 0 | 1 | 0 | Х | 0 | Х | Z | Z | Open |
| 1 | 0 | 1 | 0 | 0 | 1 | L | L | Н | CCW |
| 1 | 0 | 1 | 0 | 0 | 1 | Н | Н | L | CW |
| 1 | 0 | 1 | 0 | 1 | 1 | Х | L | L | Short Brake |
| CW / CO | CW Drive | Mode via | INPUT45 | i Pin | | | | | |
| 1 | 0 | 1 | 1 | Х | 0 | Х | Z | Z | Open |
| 1 | 0 | 1 | 1 | 0 | 1 | L | Н | L | ĊW |
| 1 | 0 | 1 | 1 | 0 | 1 | Н | L | Н | CCW |
| 1 | 0 | 1 | 1 | 1 | 1 | Х | L | L | Short Brake |

L: Low, H: High, X: Don't care, Z: Hi impedance (Note 17) CW: Current flows from OUT5A to OUT5B, CCW: Current flows from OUT5B to OUT5A

| | 9 | Serial Int | erface Bit | | | INF | Mode PUT | | | OU | TPUT | |
|-----------|----------------|--------------|--------------|------|-------|----------|-------------|----------|----------|---------|------|---------------|
| MODE | MODE | | | | | INPUT | INPUT | OUT | OUT | OUT | OUT | Output Mod |
| 12B | 12A | IN2B | IN2A | IN1B | IN1A | 1 | 2 | 1A | 1B | 2A | 2B | (Note 18) |
| 1 | 0 | 0 | 1 | 0 | 1 | H | H | H | L | H | L | 1. CW / CW |
| 1 | 0 | 0 | 1 | 0 | 1 | H | L | H | L | L | Н | 2. CCW / CV |
| 1 | 0 | 0 | 1 | 0 | 1 | L | L | L | Н | L | H | 3. CCW / CC |
| 1 | 0 | 0 | 1 | 0 | 1 | L | H | L | H | Н | L | 4. CW / CCV |
| | ligh, X: Don't | | - | | | | | | | | - | 1 4. 0117 001 |
| | | | | | | | | | | 2 | | |
| PS | | | ╶╺┤┝ | , | | | | | | \sum | | |
| STROBE | | 님님 | • [] 신 | L4 | | | | | | | | Ŀ |
| SCLK | | | | | | | | | | | 5 | |
| SDATA | (i) (ii) |) (iii) (iv) | (v) | (vi) | | | | | | | | (vii) |
| INPUT1 | | | | |] | | | | | | | |
| INPUT2 | | | | | | | | | | |] | |
| OUT1A [V] | ///// | | | | | | | | | | | |
| OUT1B [V] | ///// | | | | | ĺ | | | | | | 7772 |
| OUT2A [V] | //// | | | | | | | | | | | |
| OUT2B [V] | ///// | | | | | | | | <u> </u> | ĺ. | Ī | |
| OUT1A-1B | A] | | 2 | | | | | | | | | |
| OUT2A-2B | A] | | | | 3 (4) | | 3 4 | 1 4 | | | | |
| | ; Don't care | | li impedance | | | rward | | <u> </u> | | Reverse | | |
| | | | | | | | | | | | | |
| | | | | | | Figure 9 |) . | | | | | |

| Table 27 | 7. An Exan | nple of Se | erial Contro | ol from Ini | itial Set U | | | vii) (SDA | TA image i | in Figure 9 | 9.) | |
|---------------------|------------|-------------|--------------|-------------|-------------|----------------|-----------|-----------|------------|-------------|--------|--------|
| ADR. | | 1 | 1 | | | DAT | A BIT | | | | 1 | |
| <i>,</i> . 2 | Bit[B] | Bit[A] | Bit[9] | Bit[8] | Bit[7] | Bit[6] | Bit[5] | Bit[4] | Bit[3] | Bit[2] | Bit[1] | Bit[0] |
| | | | | | I | nitial set u | qı | | | | | |
| (i) ADD | RESS BI | Г [000]; Se | etup of cha | annel 1 & | channel 2 | 2 to drive | Constant- | Voltage m | ode | | | |
| | | | MODE | MODE | MODE | MODE | MODE | MODE | MODE | MODE | MODE | MODE |
| 000 | | | 45 | 34 | 23 | 13 | 3C | 3B | ЗA | 12C | 12B | 12A |
| | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | | 0 |
| (ii) ADD | DRESS BI | T [001]; S | etup of ou | itput high | voltage=3 | .0V for ch | annel 1 8 | channel | 2 | | | |
| | DAC | DAC | DAC | DAC | DAC | DAC | MODE | MODE | MODE | MODE | MODE | MODE |
| 001 | 12[5] | 12[4] | 12[3] | 12[2] | 12[1] | 12[0] | 5B | 5A | 4D | 4C | 4B | 4A |
| | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| (iii) AD | DRESS B | IT [010]; N | No need in | this case | • | | L | | | | | Ľ |
| | DAC | DAC | DAC | DAC | DAC | DAC | DAC | DAC | DAC | DAC | DAC | DAC |
| 010 | 5[5] | 5[4] | 5[3] | 5[2] | 5[1] | 5[0] | 3[5] | 3[4] | 3[3] | 3[2] | 3[1] | 3[0] |
| 0.0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| (iv) AD | DRESS B | IT [011]; N | No need in | this case | • | | | | | | | |
| | DAC | DAC | DAC | DAC | DAC | DAC | DAC | DAC | DAC | DAC | DAC | DAC |
| 011 | V4[5] | V4[4] | V4[3] | V4[2] | V4[1] | V4[0] | 14[5] | 14[4] | 14[3] | 14[2] | I4[1] | I4[0] |
| | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| (v) ADI | DRESS BI | T [100]; S | Setup of sta | and-by m | ode | | | | | | | · |
| 100 | | | IN5B | IN5A | IN4B | IN4A | IN3B | IN3A | IN2B | IN2A | IN1B | IN1A |
| 100 | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | | | | | Oto et timo in | | | | | | |
| | DRESS B | IT [100] | | | | Start timin | y | | | | | |
| | | | | | | | | | | | | |
| 100 | | | IN5B | IN5A | IN4B | IN4A | IN3B | IN3A | IN2B | IN2A | IN1B | IN1A |
| 100 | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |
| | | | | | | | | | | | | |
| (| | | | | | End timin | g | | | | | |
| (VII) AD | DRESS B | 511 [100] | | | 1 | | 1 | 1 | | | 1 | 1 |

| 100 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
|-----|---|---|---|---|---|---|---|---|---|
| · · | | | | | | | | | |

IN4B

IN4A

IN3B

IN3A

IN2B

IN2A

IN1B

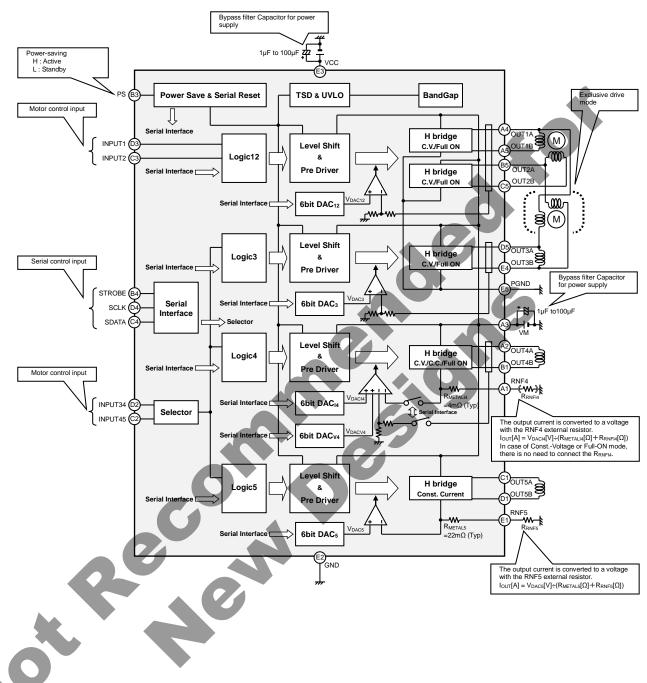
IN1A

0

IN5B

IN5A

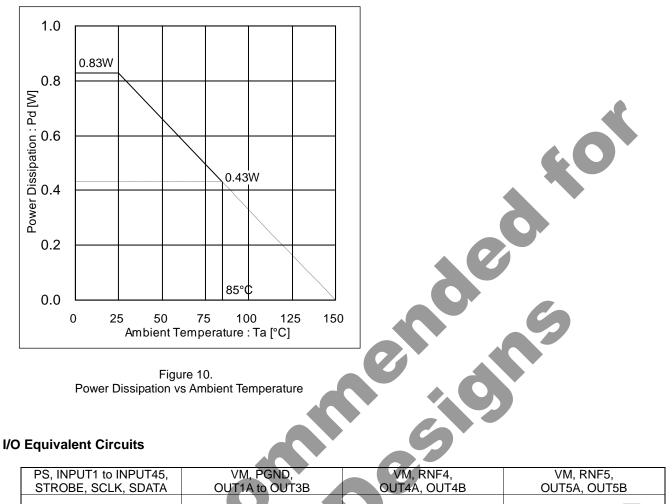
Application Example

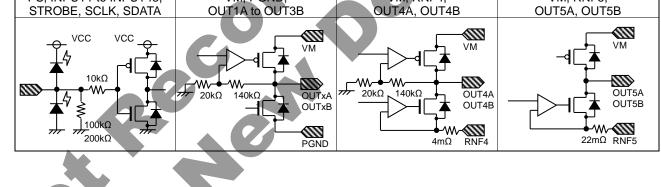


Selection of Components Externally Connected

When using the circuit with changes to the external circuit constants, make sure to leave an adequate margin for external components including static and transitional characteristics as well as dispersion of the IC.

Power Dissipation





Operational Notes

1. Reverse Connection of Power Supply

Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. Power Supply Lines

Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. Ground Voltage

Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. Ground Wiring Pattern

When using both small-signal(GND) and large-current ground(PGND) traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. Thermal Consideration

Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

6. Recommended Operating Conditions

These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. Inrush Current

When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. Operation Under Strong Electromagnetic Field

Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. Testing on Application Boards

When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. Inter-pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

11. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

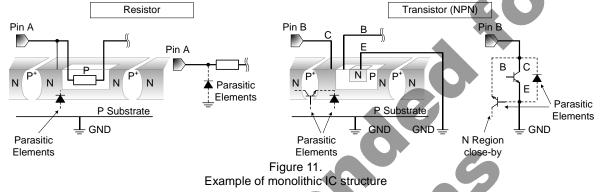
Operational Notes – continued

12. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode. When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.



13. Ceramic Capacitor

When using a ceramic capacitor, determine the dielectric constant considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

14. Area of Safe Operation (ASO)

Operate the IC such that the output voltage, output current, and power dissipation are all within the Area of Safe Operation (ASO).

15. Thermal Shutdown Circuit(TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's power dissipation rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF all output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.

Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

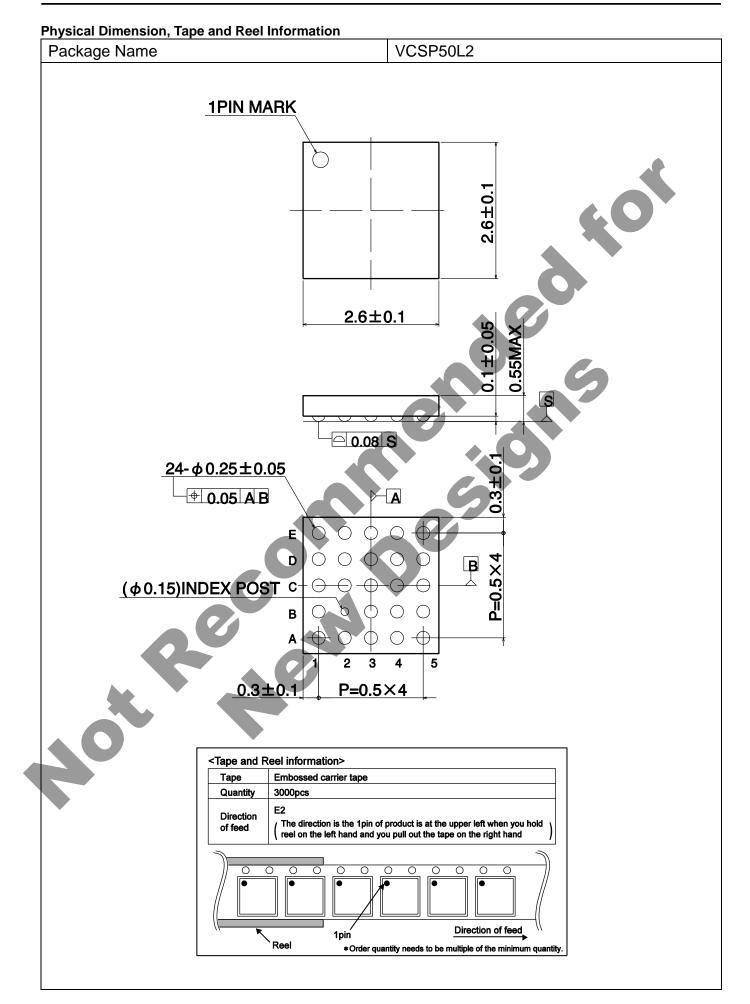
16. Disturbance light

In a device where a portion of silicon is exposed to light such as in a WL-CSP, IC characteristics may be affected due to photoelectric effect. For this reason, it is recommended to come up with countermeasures that will prevent the chip from being exposed to light.



Ordering Information

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Revision History

| Date | Revision | Changes |
|-------------|----------|-------------|
| 09.Dec.2015 | 001 | New Release |

Recomberions

Notice

Precaution on using ROHM Products

Our Products are designed and manufactured for application in ordinary electronic equipments (such as AV equipment, 1. OA equipment, telecommunication equipment, home electronic appliances, amusement equipment, etc.). If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment ^(Note 1), transport equipment, traffic equipment, aircraft/spacecraft, nuclear power controllers, fuel controllers, car equipment including car accessories, safety devices, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

| (Note1) Medical Equipment Classification of the Specific Applicatio | | | | | | |
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- 2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:

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 - [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
 - [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
 - [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl2, H2S, NH3, SO2, and NO2
 - [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
 - [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
 - [f] Sealing or coating our Products with resin or other coating materials
 - [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
 - [h] Use of the Products in places subject to dew condensation
- 4. The Products are not subject to radiation-proof design.
- Please verify and confirm characteristics of the final or mounted products in using the Products. 5.
- 6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power, exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

- Confirm that operation temperature is within the specified range described in the product specification. 8.
- ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in 9. this document.

Precaution for Mounting / Circuit board design

- When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.
- In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must 2. be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

7.

Precautions Regarding Application Examples and External Circuits

- 1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.
- 2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of lonizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

- 1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
 - [a] the Products are exposed to sea winds or corrosive gases, including Cl2, H2S, NH3, SO2, and NO2
 - [b] the temperature or humidity exceeds those recommended by ROHM
 - [c] the Products are exposed to direct sunshine or condensation
 - [d] the Products are exposed to high Electrostatic
- 2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.
- 3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.
- 4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

Precaution for Product Label

QR code printed on ROHM Products label is for ROHM's internal use only.

Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

Precaution for Foreign Exchange and Foreign Trade act

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