

SILICON POWER MOS FET NE552R479A

3.0 V OPERATION SILICON RF POWER LDMOS FET FOR 2.45 GHz 0.4 W TRANSMISSION AMPLIFIERS

DESCRIPTION

The NE552R479A is an N-channel silicon power laterally diffused MOS FET specially designed as the transmission power amplifier for 3.0 V WLL products. Dies are manufactured using our NEWMOS2 technology (our WSi gate laterally diffused MOS FET) and housed in a surface mount package. This device can deliver 26.0 dBm output power with 45% power added efficiency at 2.45 GHz under the 3.0 V supply voltage.

FEATURES

•	High output power	: Pout = 26.0 dBm 7	TYP. (VDS = 3.0	V, IDset = 200 mA, f =	= 2.45 GHz, Pin = 19 dBm)
	Ligh newer added officiency			200 mA f 2.4	

- High linear gain
- High power added efficiency : $\eta_{add} = 45\%$ TYP. (Vos = 3.0 V, IDset = 200 mA, f = 2.45 GHz, Pin = 19 dBm) : GL = 11 dB TYP. (VDS = 3.0 V, IDset = 200 mA, f = 2.45 GHz, Pin = 10 dBm) : 5.7 × 5.7 × 1.1 mm MAX.
- Surface mount package Single supply

: VDS = 2.8 to 6.0 V

APPLICATIONS

- Digital cellular phones : 3.0 V GSM1900 Pre Driver
- Analog cellular phones : 2.8 V AMPS Handsets
- Bluetooth[™] applications : 3.0 V Class 1 Devices
- Others : 3.0 V Two-Way Pagers

ORDERING INFORMATION

Part Number	Package	Marking	Supplying Form
NE552R479A-T1	79A	AW	 12 mm wide embossed taping Gate pin face the perforation side of the tape Qty 1 kpcs/reel
NE552R479A-T1A			 12 mm wide embossed taping Gate pin face the perforation side of the tape Qty 5 kpcs/reel

Remark To order evaluation samples, contact your nearby sales office. Part number for sample order: NE552R479A-A

Caution: Observe precautions when handling because these devices are sensitive to electrostatic discharge

The information in this document is subject to change without notice. Before using this document, please confirm that this is the latest version.

ABSOLUTE MAXIMUM RATINGS (TA = +25°C)

Parameter	Symbol	Ratings	Unit
Drain to Source Voltage	Vds	15.0	V
Gate to Source Voltage	Vgs	5.0	V
Drain Current	lo	300	mA
Drain Current (Pulse Test)	D Note	600	mA
Total Power Dissipation	Ptot	10	W
Channel Temperature	Tch	125	°C
Storage Temperature	Tstg	-55 to +125	°C

Note Duty Cycle 50%, $T_{on} \le 1$ s

RECOMMENDED OPERATING CONDITIONS

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- 5	-	

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Drain to Source Voltage	Vds		2.8	3.0	6.0	V
Gate to Source Voltage	Vgs		0	2.0	3.0	V
Drain Current	lo	Duty Cycle 50%, $T_{on} \leq 1 s$	-	200	500	mA
Input Power	Pin	f = 2.45 GHz, V _{DS} = 3.0 V	18	19	25	dBm

ELECTRICAL CHARACTERISTICS

(T_A = +25°C, unless otherwise specified, using NEC standard test fixture)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Gate to Source Leak Current	IGSS	Vgs = 5.0 V	-	-	100	nA
Drain to Source Leakage Current (Zero Gate Voltage Drain Current)	loss	V _{DS} = 6.0 V	_	-	100	nA
Gate Threshold Voltage	Vth	V _{DS} = 3.5 V, I _D = 1 mA	1.0	1.4	1.9	V
Thermal Resistance	Rth	Channel to Case	-	-	10	°C/W
Transconductance	Gm	V _{DS} = 3.5 V, I _D = 100 mA	-	0.4	_	S
Drain to Source Breakdown Voltage	BVDSS	Ibss = 10 μ A	15	18	-	V
Output Power	Pout	f = 2.45 GHz, V _{DS} = 3.0 V,	24.0	26.0	-	dBm
Drain Current	lo	P _{in} = 19 dBm,	-	230	-	mA
Power Added Efficiency	η add	I _{Dset} = 200 mA (RF OFF), Note1	35	45	-	%
Linear Gain ^{Note2}	G∟		-	11	_	dB

Notes 1. DC performance is 100% testing. RF performance is testing several samples per wafer. Wafer rejection criteria for standard devices is 1 reject for several samples.

2. Pin = 10 dBm

 η d, η add vs. INPUT POWER

%

 η_{add}

Drain Efficiency η_{d} (%) Power Added Efficiency

OUTPUT POWER, DRAIN CURRENT

 $\eta d, \eta a d vs.$ GATE TO SOURCE VOLTAGE

Drain Current b (mA) Drain Current b (mA) 30 30 f = 2.45 GHz V_{DS} = 3.0 V P_{in} = 19 dBm f = 2.45 GHz V_{DS} = 3.0 V I_{Dset} = 100 mA Pout 25 100 25 1 000 100 Pout (dBm) Pout (dBm) η_{add} (%) Pout 20 750 20 75 750 75 Power Added Efficiency (%) η d Output Power ηd Output Power рμ η ado 15 500 50 15 500 50 25 Efficiency η_{add} 10 250 10 250 25 lь Drain 5 n 0 5 0 0 0 5 10 15 20 25 0 2 3 Δ Input Power Pin (dBm) Gate to Source Voltage Vgs (V) Drain Current Dra(mA) OUTPUT POWER, DRAIN CURRENT INTERMODULATION DISTORTION vs. 2 TONES TO OUTPUT POWER η d, η add vs. INPUT POWER 30 IM5 (dBc) f = 2.45 GHz f = 2.45 GHz Δf = 1 MHz $V_{DS} = 3.0 V$ Pout I_{Dset} = 200 mA -20 Vps = 3.0 V 25 1 000 $\begin{array}{ccccccc} 0 & 5 & 6 & 5 \\ \text{Drain Efficiency} & \eta_{\text{d}} \ (\%) \\ \text{Power Added Efficiency} & \eta_{\text{add}} \ (\%) \\ \end{array}$ Output Power Pout (dBm) $J_{Dset} = 200 \text{ mA}$ IN3, IM 30 20 750 Intermodulation Distortion IM5 η d -40 15 500 η_{add} -50 ID 10 250 -60 5 0 0 -70 0 5 10 15 20 25 5 10 15 20 25 30 Input Power Pin (dBm) 2 Tones to Output Power Pout (dBm) ر Drain Current در mA) OUTPUT POWER, DRAIN CURRENT Drain Current b (mA) OUTPUT POWER, DRAIN CURRENT η d, η add vs. GATE TO SOURCE VOLTAGE ηd, ηadd vs. INPUT POWER 30 30 f = 2.00 GHz f = 2.00 GHz $V_{DS} = 3.0 V$ $P_{in} = 19 dBn$ Pout Vps = 3.0 V Pout $I_{Dset} = 150 \text{ mA}$ 25 000 25 1 000 100 100 η_{add} (%) Pout (dBm) Output Power Pout (dBm) 20 750 20 750 75 75 Added Efficiency η d (%) PU $\eta \sigma$ Output Power η add nado 15 500 15 500 50 50 Efficiency lь D 250 250 10 25 10 25 Power, Drain

TYPICAL CHARACTERISTICS ($T_A = +25^{\circ}C$)

OUTPUT POWER, DRAIN CURRENT



15

20

5

0

5

10

Input Power Pin (dBm)

0_ 25

0

5

0

1

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η_{add} (%)

Drain Efficiency η_{d} (%) Power Added Efficiency

0

0

4

2

Gate to Source Voltage VGS (V)

3

S-PARAMETERS

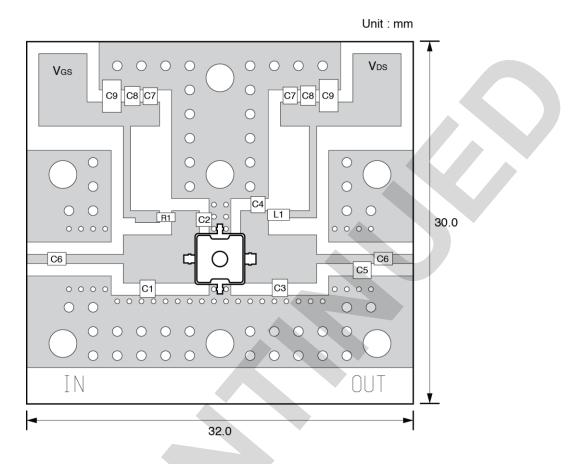
- S-parameters and noise parameters are provided on our Web site in a format (S2P) that enables the direct import of the parameters to microwave circuit simulators without the need for keyboard inputs.
- · Click here to download S-parameters.
- [RF and Microwave] ® [Device Parameters]
- URL http://www.necel.com/microwave/en/

LARGE SIGNAL IMPEDANCE (VDS = 3.0 V, ID = 200 mA, f = 2.45 GHz, Pout = 400 mW)

f (GHz)	$Z_{in}\left(\Omega ight)$	$Z_OL\left(\Omega ight)^{Note}$
2.45	2.96 –j7.78	3.36 –j8.42

Note ZoL is the conjugate of optimum load impedance at given voltage, idling current, input power and frequency.

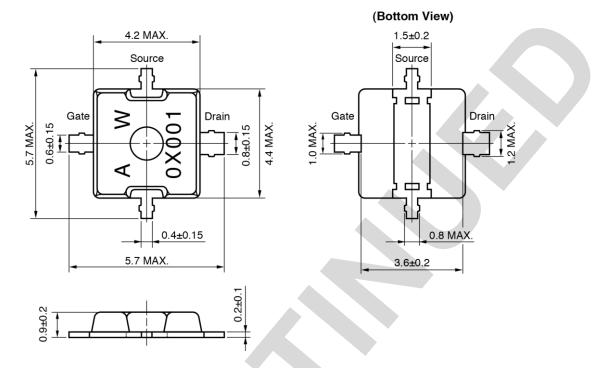
EVALUATION BOARD FOR 2.45 GHz



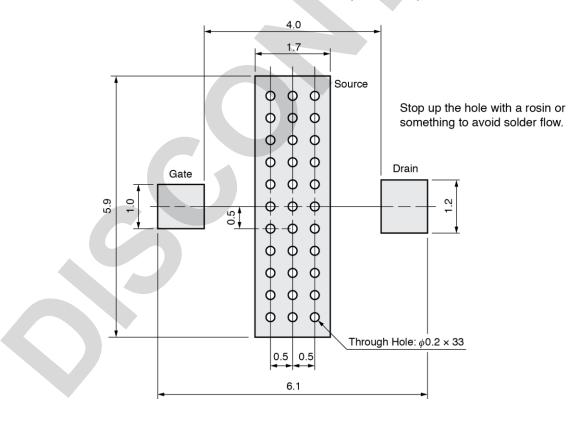
Symbol	Value	Comment
C1	2.0 pF	
C2	1.4 pF	
C3	2.2 pF	
C4	0.8 pF	
C5	0.5 pF	
C6	10 pF	
C7	1 000 pF	
C8	0.22 μF	
C9	3.3 μF - 16V	
R1	1 000 Ω	
L1	22 nH	
Circuit Board	t = 0.4 mm, ϵ r = 4.5	R4775

PACKAGE DIMENSIONS

79A (UNIT: mm)



79A PACKAGE RECOMMENDED P.C.B. LAYOUT (UNIT: mm)



Data Sheet PU10124EJ03V0DS

RECOMMENDED SOLDERING CONDITIONS

This product should be soldered and mounted under the following recommended conditions. For soldering methods and conditions other than those recommended below, contact your nearby sales office.

Soldering Method	Soldering Conditions	Condition Symbol	
Infrared Reflow	Peak temperature (package surface temperature) Time at peak temperature Time at temperature of 220°C or higher Preheating time at 120 to 180°C Maximum number of reflow processes Maximum chlorine content of rosin flux (% mass)	: 260°C or below : 10 seconds or less : 60 seconds or less : 120±30 seconds : 3 times : 0.2%(Wt.) or below	IR260
VPS	Peak temperature (package surface temperature) Time at temperature of 200°C or higher Preheating time at 120 to 150°C Maximum number of reflow processes Maximum chlorine content of rosin flux (% mass)	: 215°C or below : 25 to 40 seconds : 30 to 60 seconds : 3 times : 0.2%(Wt.) or below	VP215
Wave Soldering	Peak temperature (molten solder temperature) Time at peak temperature Preheating temperature (package surface temperature) Maximum number of flow processes Maximum chlorine content of rosin flux (% mass)	: 260°C or below : 10 seconds or less : 120°C or below : 1 time : 0.2%(Wt.) or below	W \$260
Partial Heating	Peak temperature (pin temperature) Soldering time (per pin of device) Maximum chlorine content of rosin flux (% mass)	: 350°C or below : 3 seconds or less : 0.2%(Wt.) or below	HS350-P3

Caution Do not use different soldering methods together (except for partial heating).