



# MTM763200LBF

Silicon N-channel MOSFET (FET1)

Silicon P-channel MOSFET (FET2)

For Switching

For DC-DC Converter

■ Features

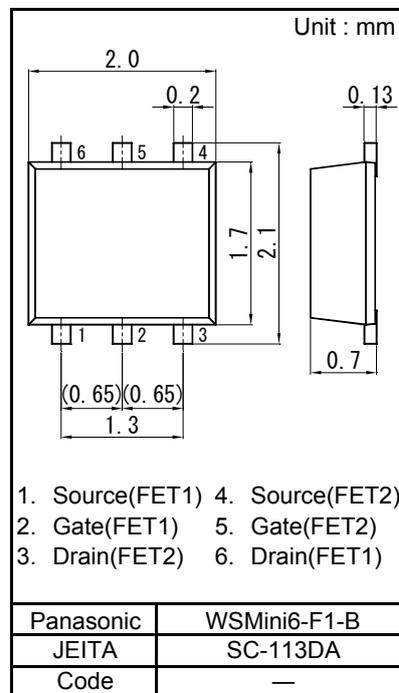
- Low Drain-source On-state Resistance :  
 $R_{DS(on)}$  typ. N-ch = 80 m $\Omega$  (VGS = 4.0 V) P-ch: 100 m $\Omega$  (VGS = -4.0 V)
- Halogen-free / RoHS compliant  
 (EU RoHS / UL-94 V-0 / MSL : Level 1 compliant)

■ Marking Symbol JB

■ Basic Part Number Nch+Pch MOS 20V (Individual)

■ Packaging

Embossed type (Thermo-compression sealing) 3 000 pcs / reel (standard)

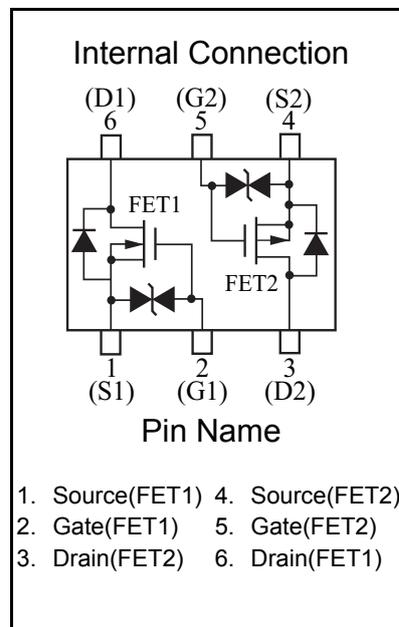


■ Absolute Maximum Ratings Ta = 25 °C

Parameter		Symbol	Rating	Unit
FET1 (N-ch.)	Drain-source Voltage	VDS	20	V
	Gate-source Voltage	VGS	±10	V
	Drain current	ID	1.9	A
	Peak drain current	IDp	12	A
FET2 (P-ch.)	Drain-source Voltage	VDS	-20	V
	Gate-source Voltage	VGS	±10	V
	Drain current	ID	-1.2	A
	Peak drain current	IDp	-7	A
Overall	Total power dissipation *1	PD	700	mW
	Channel temperature	Tch	150	°C
	Operating ambient temperature	Topr	-40 to +85	°C
	Storage Temperature Range	Tstg	-55 to +150	°C

Note \*1 Measuring on ceramic substrate at 40 mm · 38 mm · 0.2 mm.

PD absolute maximum rating Non-heat sink: 150 mW.



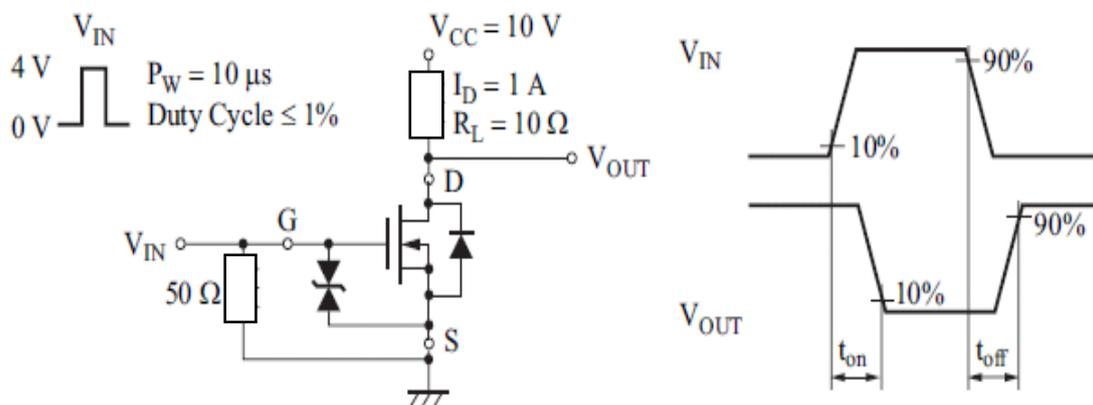
■ Electrical Characteristics Ta = 25 °C ± 3 °C  
 FET1 (N-ch.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Drain-source Breakdown Voltage	VDSS	ID = 1.0 mA, VGS = 0 V	20			V
Zero Gate Voltage Drain Current	IDSS	VDS = 20 V, VGS = 0 V			1.0	μA
Gate-source Leakage Current	IGSS	VGS = ±8.0 V, VDS = 0 V			±10	μA
Gate-source Threshold Voltage	Vth	ID = 1.0 mA, VDS = 10 V	0.4	0.85	1.3	V
Drain-source ON resistance *1	RDS(ON)1	ID = 1.0 A, VGS = 4.0 V		80	105	mΩ
	RDS(ON)2	ID = 0.5 A, VGS = 2.5 V		100	150	
Forward transfer admittance *1	Yfs	ID = 1.0 A, VDS = 10 V	3.0			S
Input Capacitance	Ciss	VDS = 10 V, VGS = 0, f = 1 MHz		280		pF
Output Capacitance	Coss			18		
Reverse Transfer Capacitance	Crss			17		
Turn-on time *2	ton	VDD = 10 V, VGS = 0 to 4 V, ID = 1.0 A		12		ns
Turn-off time *2	toff	VDD = 10 V, VGS = 4 to 0 V, ID = 1.0 A		50		

Note : 1. Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 Measuring methods for transistors.

2. \*1 Pulse measurement

\*2 Measurement circuit for Turn-on Time / Turn-off Time



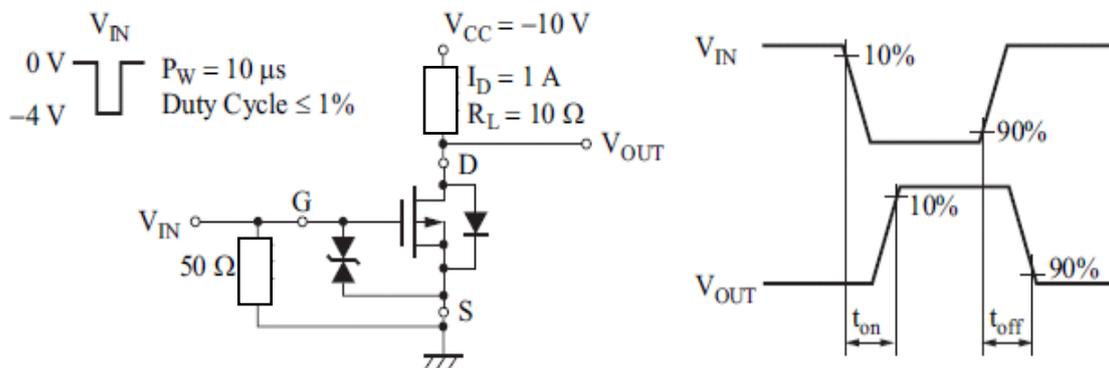
FET2 (P-ch.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Drain-source Breakdown Voltage	VDSS	ID = -1 mA, VGS = 0 V	-20			V
Zero Gate Voltage Drain Current	IDSS	VDS = -20 V, VGS = 0 V			-1.0	μA
Gate-source Leakage Current	IGSS	VGS = ±8 V, VDS = 0 V			±10	μA
Gate-source Threshold Voltage	Vth	ID = -1.0 mA, VDS = -10 V	-0.4	-0.85	-1.3	V
Drain-source On-state Resistance *1	RDS(ON)1	ID = -1.0 A, VGS = -4.0 V		100	130	mΩ
	RDS(ON)2	ID = -0.6 A, VGS = -2.5 V		130	200	
Forward transfer admittance *1	Yfs	ID = -1.0 A, VDS = -10 V	3.0			S
Input Capacitance	Ciss	VDS = -10 V, VGS = 0, f = 1 MHz		440		pF
Output Capacitance	Coss			40		
Reverse Transfer Capacitance	Crss			38		
Turn-on Time *2	ton	VDD = -10 V, VGS = 0 to -4 V ID = -1 A		35		ns
Turn-off Time *2	toff	VDD = -10 V, VGS = -4 to 0 V ID = -1 A		100		

Note: 1. Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 Measuring methods for transistors.

2. \*1 Pulse measurement

\*2 Measurement circuit for Turn-on Time / Turn-off Time

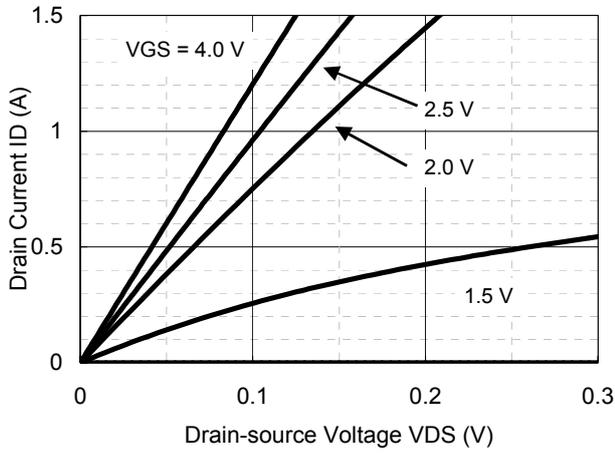




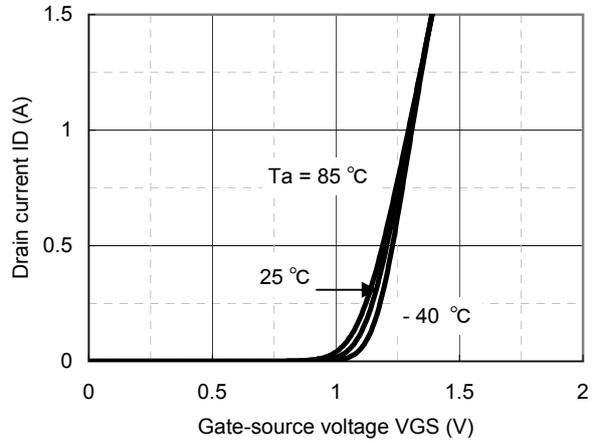
FET1(Nch.)

Technical Data ( reference )

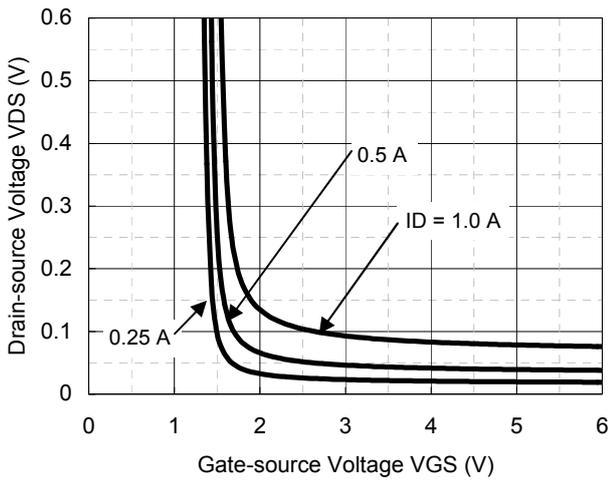
ID - VDS



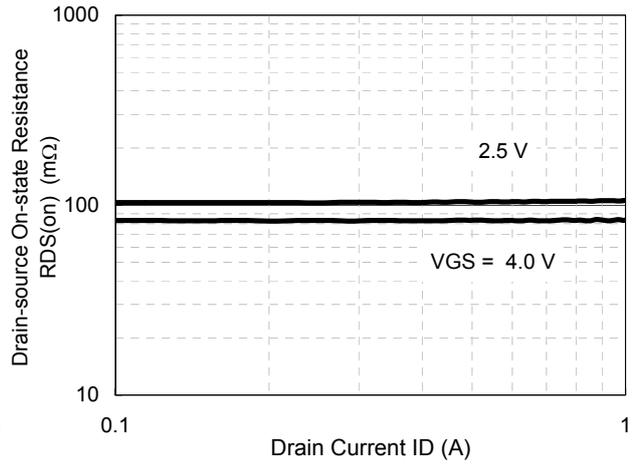
ID - VGS



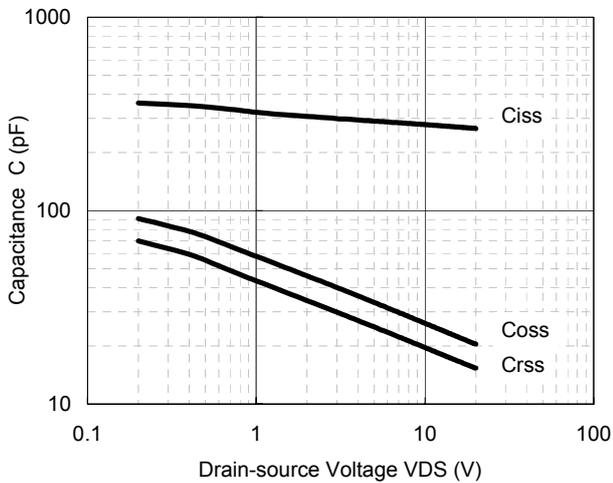
VDS - VGS



RDS(on) - ID



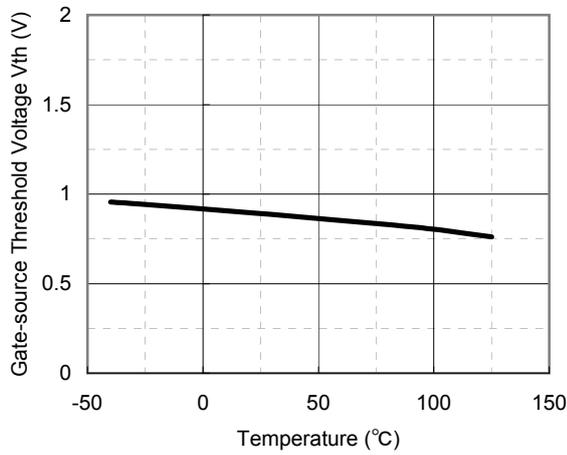
Capacitance - VDS



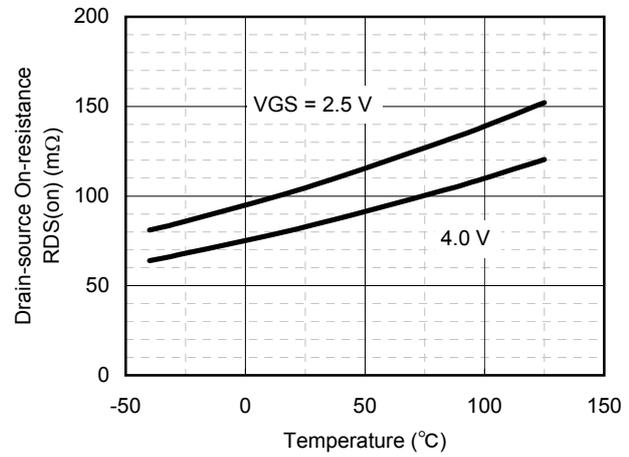
FET1(Nch.)

Technical Data ( reference )

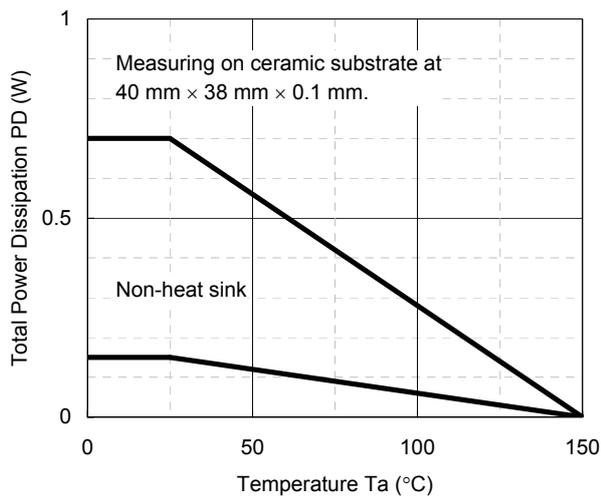
V<sub>th</sub> - T<sub>a</sub>



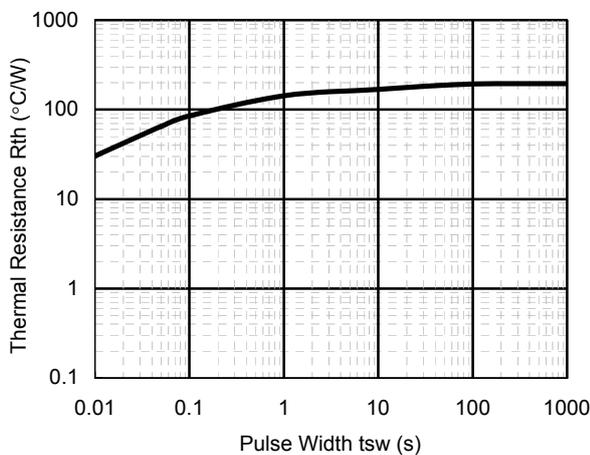
R<sub>DS(on)</sub> - T<sub>a</sub>



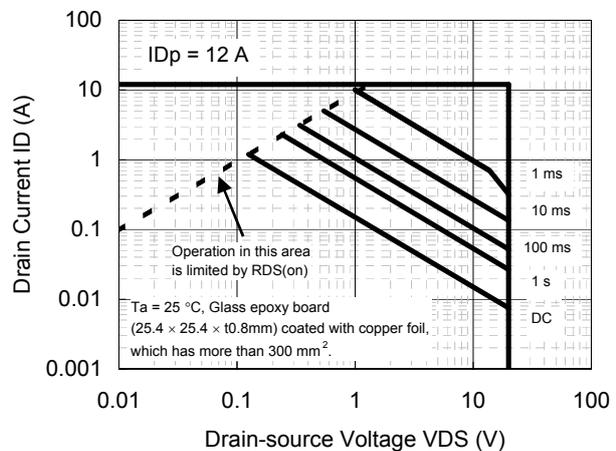
P<sub>D</sub> - T<sub>a</sub>



R<sub>th</sub> - t<sub>sw</sub>



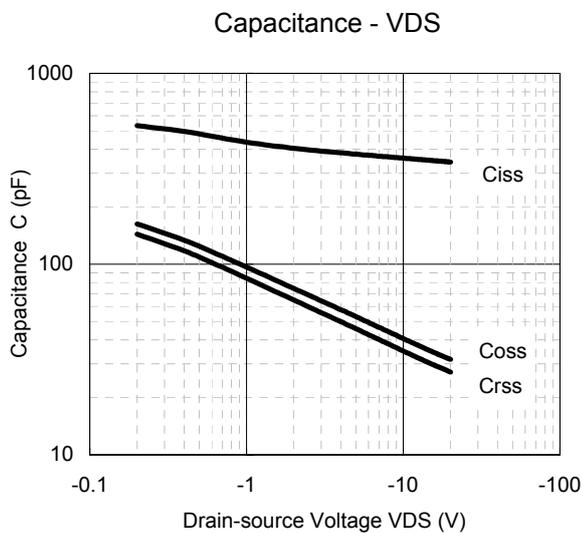
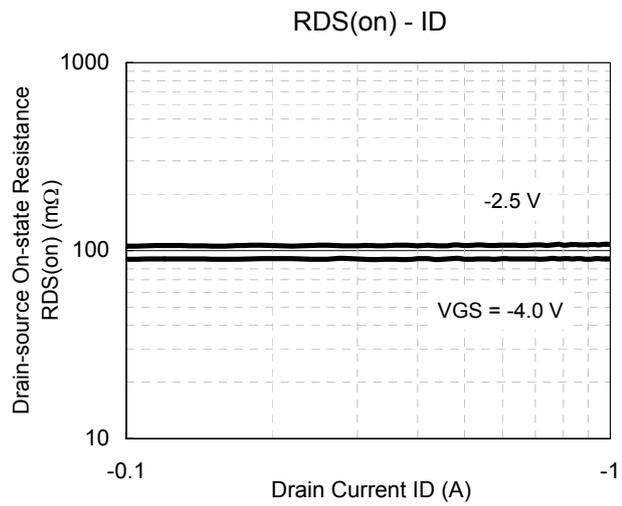
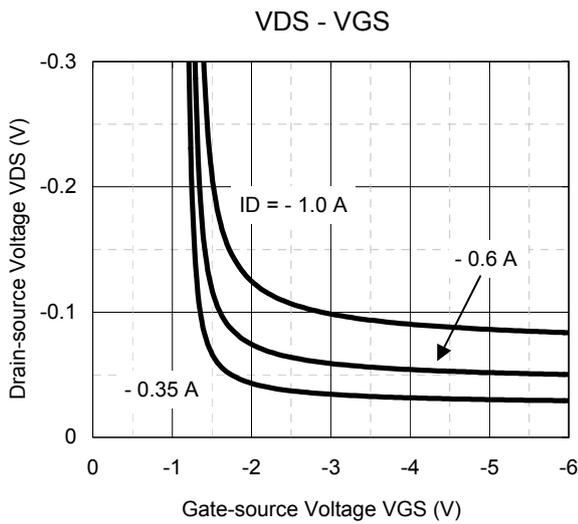
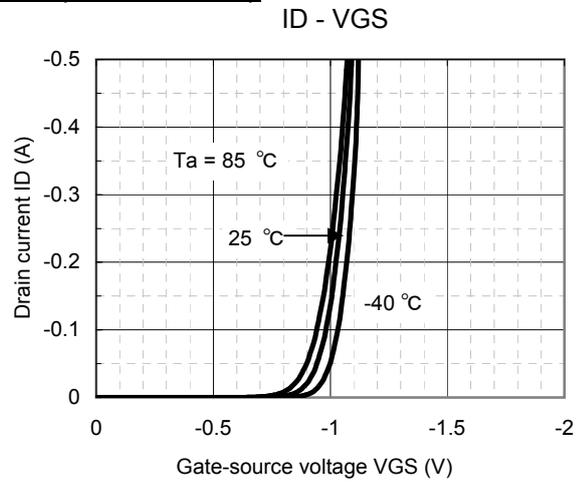
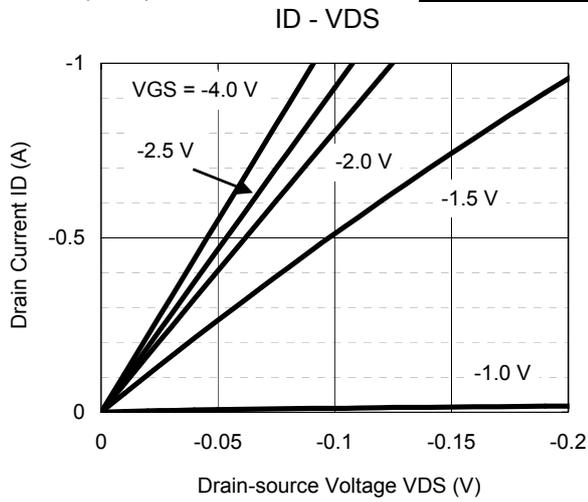
Safe Operating Area





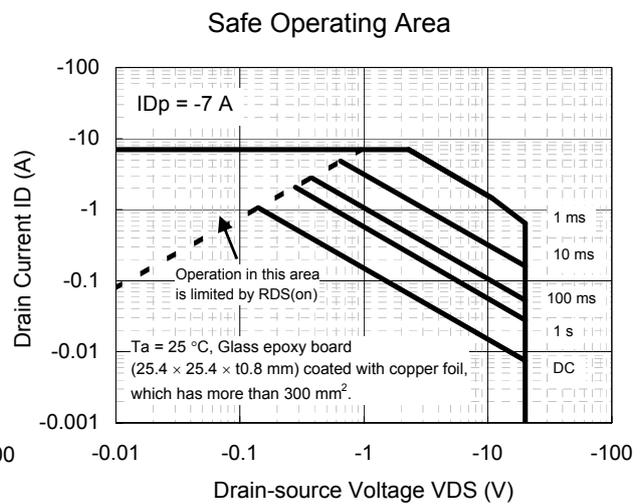
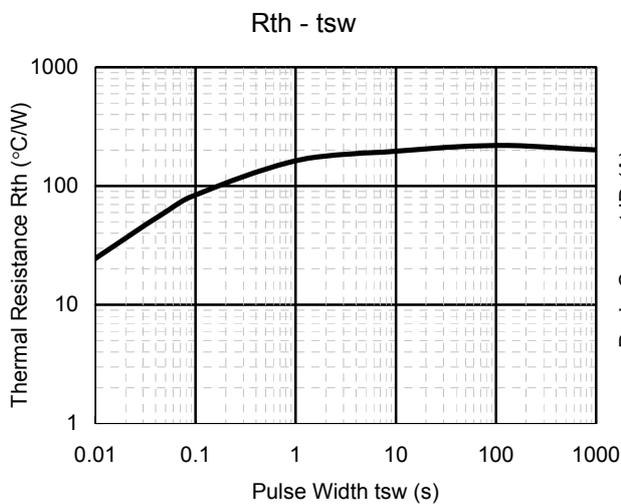
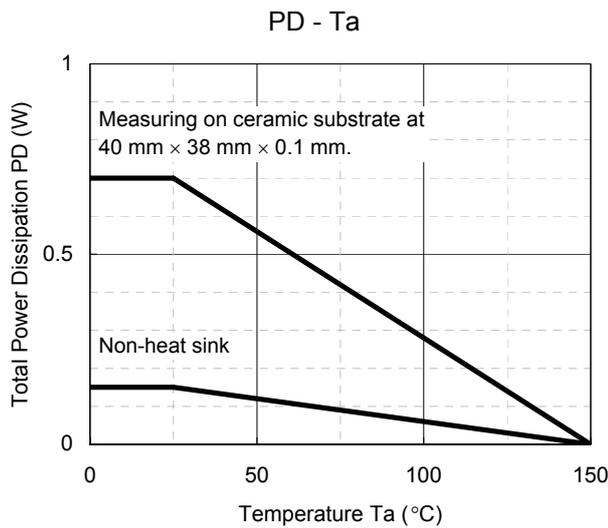
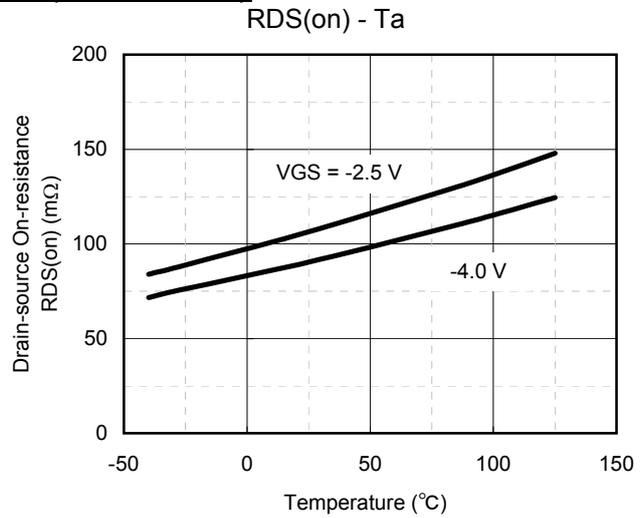
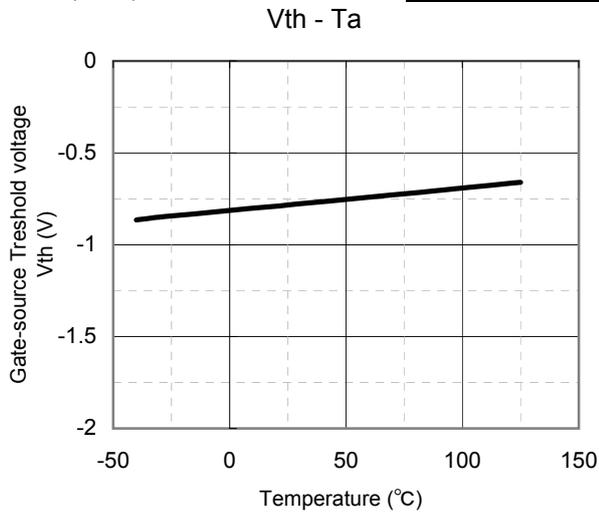
FET2(Pch.)

Technical Data ( reference )



FET2(Pch.)

Technical Data ( reference )





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