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Please note: As part of the Fairchild Semiconductor integration, some of the Fairchild orderable part numbers will need to change in order to meet ON Semiconductor's system requirements. Since the ON Semiconductor product management systems do not have the ability to manage part nomenclature that utilizes an underscore (_), the underscore (_) in the Fairchild part numbers will be changed to a dash (-). This document may contain device numbers with an underscore (_). Please check the ON Semiconductor website to verify the updated device numbers. The most current and up-to-date ordering information can be found at www.onsemi.com. Please email any questions regarding the system integration to Fairchild_questions@onsemi.com.

March 2016

QFET™
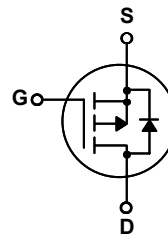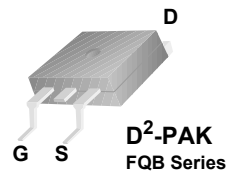
FQB34P10TM_F085

100V P-Channel MOSFET

General Description

These P-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar stripe, DMOS technology.

This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for low voltage applications such as audio amplifier, high efficiency switching DC/DC converters, and DC motor control.

Features

- -33.5A, -100V, $R_{DS(on)}$ = 0.06Ω @V_{GS} = -10 V
- Low gate charge (typical 85 nC)
- Low Crss (typical 170 pF)
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability
- 175°C maximum junction temperature rating
- Qualified to AEC Q101
- RoHS Compliant

100% LEAD-FREE IMPLEMENTATION

D

D²-PAK
FQB Series

G **S**

S

G

D

Absolute Maximum Ratings T_C = 25°C unless otherwise noted

Symbol	Parameter			FQB34P10TM_F085	Units
V_{DSS}	Drain-Source Voltage			-100	V
I_D	Drain Current	- Continuous (T_C = 25°C)		-33.5	A
		- Continuous (T_C = 100°C)		-23.5	A
I_{DM}	Drain Current	- Pulsed	(Note 1)	-134	A
V_{GSS}	Gate-Source Voltage			± 25	V
E_{AS}	Single Pulsed Avalanche Energy		(Note 2)	2200	mJ
I_{AR}	Avalanche Current		(Note 1)	-33.5	A
E_{AR}	Repetitive Avalanche Energy		(Note 1)	15.5	mJ
dv/dt	Peak Diode Recovery dv/dt		(Note 3)	-6.0	V/ns
P_D	Power Dissipation (T_A = 25°C) *			3.75	W
	Power Dissipation (T_C = 25°C)			155	W
	- Derate above 25°C			1.03	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range			-55 to +175	°C
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds			300	°C

Thermal Characteristics

Symbol	Parameter	Typ	Max	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	--	0.97	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient *	--	40	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	--	62.5	°C/W

* When mounted on the minimum pad size recommended (PCB Mount)

Electrical Characteristics T_C = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = -250 μA	-100	--	--	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	I_D = -250 μA, Referenced to 25°C	--	-0.1	--	V/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = -100 V, V_{GS} = 0 V	--	--	-1	μA
		V_{DS} = -80 V, T_C = 150°C	--	--	-10	μA
I_{GSSF}	Gate-Body Leakage Current, Forward	V_{GS} = -25 V, V_{DS} = 0 V	--	--	-100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	V_{GS} = 25 V, V_{DS} = 0 V	--	--	100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = -250 μA	-2.0	--	-4.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	V_{GS} = -10 V, I_D = -16.75 A	--	0.049	0.06	Ω
g_{FS}	Forward Transconductance	V_{DS} = -40 V, I_D = -16.75 A (Note 4)	--	23	--	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = -25 V, V_{GS} = 0 V, f = 1.0 MHz	--	2240	2910	pF
C_{oss}	Output Capacitance		--	730	950	pF
C_{rss}	Reverse Transfer Capacitance		--	170	220	pF
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = -50 V, I_D = -33.5 A, R_G = 25 Ω	--	25	60	ns
t_r	Turn-On Rise Time		--	250	510	ns
$t_{d(off)}$	Turn-Off Delay Time		--	160	330	ns
t_f	Turn-Off Fall Time	(Note 4, 5)	--	210	430	ns
Q_g	Total Gate Charge	V_{DS} = -80 V, I_D = -33.5 A, V_{GS} = -10 V	--	85	110	nC
Q_{gs}	Gate-Source Charge		--	15	--	nC
Q_{gd}	Gate-Drain Charge	(Note 4, 5)	--	45	--	nC
Drain-Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain-Source Diode Forward Current		--	--	-33.5	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current		--	--	-134	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = -33.5 A	--	--	-4.0	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_S = -33.5 A, dI_F / dt = 100 A/μs (Note 4)	--	160	--	ns
Q_{rr}	Reverse Recovery Charge		--	0.88	--	μC

Notes:
1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. L =3.9mH, I_{AS} = -33.5A, V_{DD} = -25V, R_G = 25 Ω, Starting T_J = 25°C
3. $I_{SD} \leq$ -33.5A, di/dt $\leq$ 300A/μs, $V_{DD} \leq BV_{DSS}$, Starting T_J = 25°C
4. Pulse Test : Pulse width $\leq$ 300μs, Duty cycle $\leq$ 2%
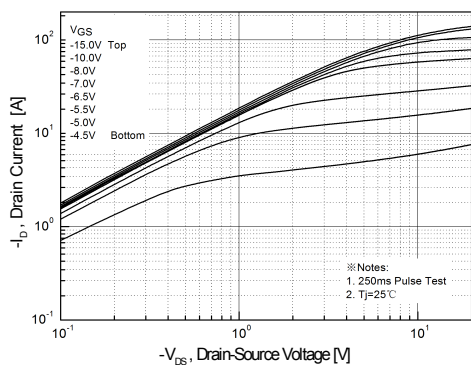5. Essentially independent of operating temperature
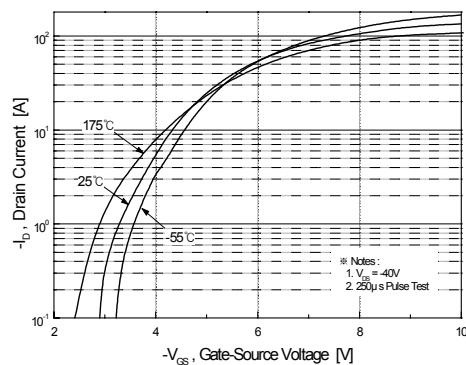
Figure 1. On-Region Characteristics
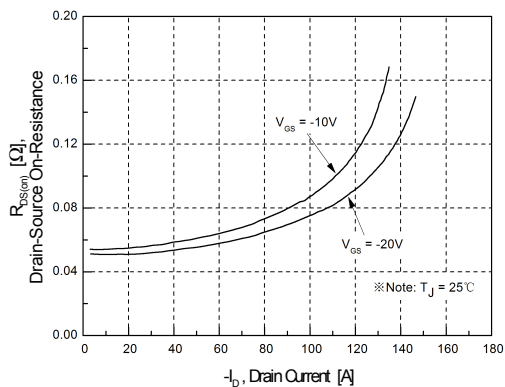

Figure 2. Transfer Characteristics

Figure 3. On-Resistance Variation vs.
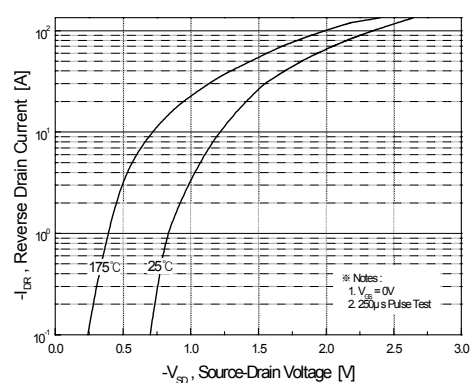Drain Current and Gate Voltage

Figure 4. Body Diode Forward Voltage
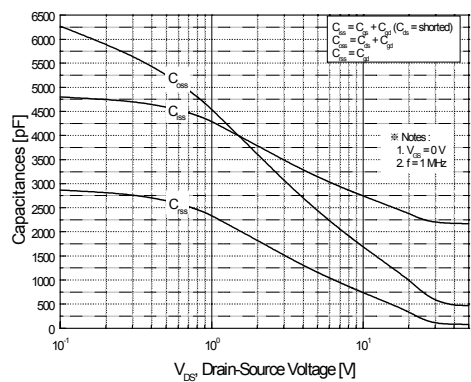Variation vs. Source Current
and Temperature
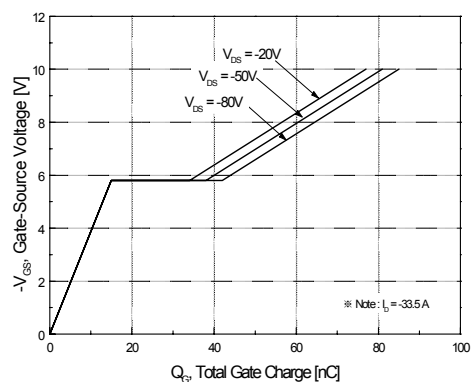

Figure 5. Capacitance Characteristics

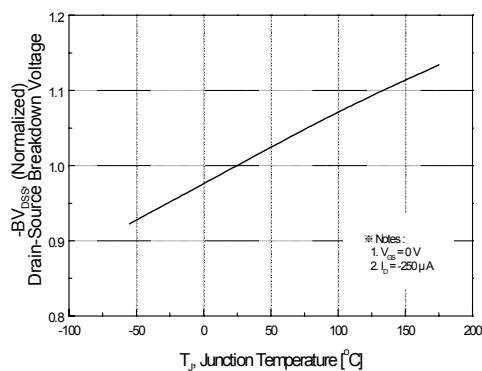Figure 6. Gate Charge Characteristics

Typical Characteristics (Continued)
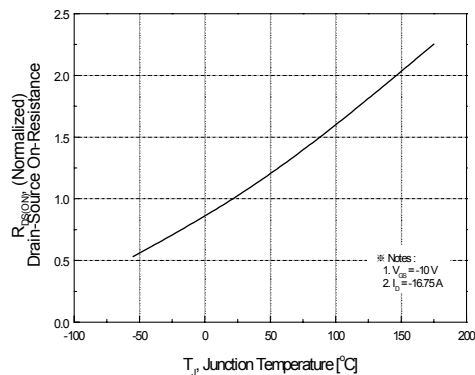

Figure 7. Breakdown Voltage Variation vs. Temperature
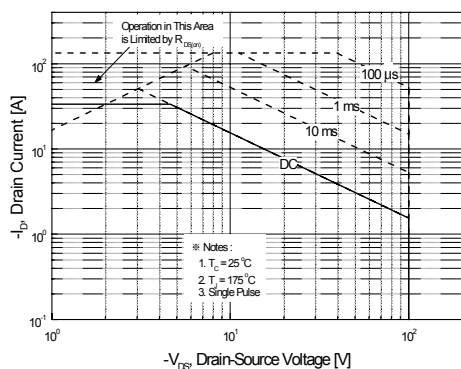

Figure 8. On-Resistance Variation vs. Temperature

Figure 9. Maximum Safe Operating Area
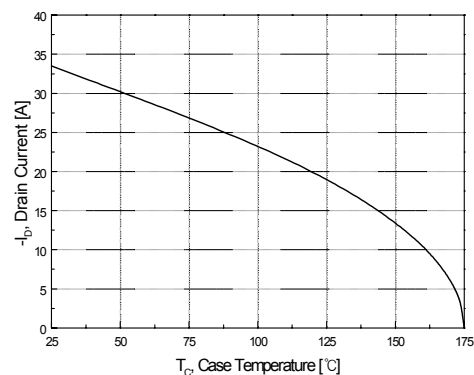
Figure 10. Maximum Drain Current vs. Case Temperature
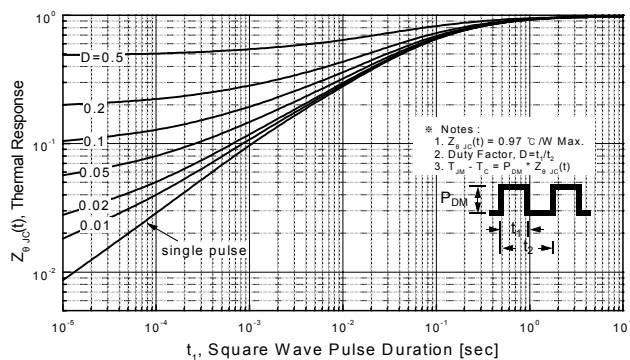
Figure 11. Transient Thermal Response Curve
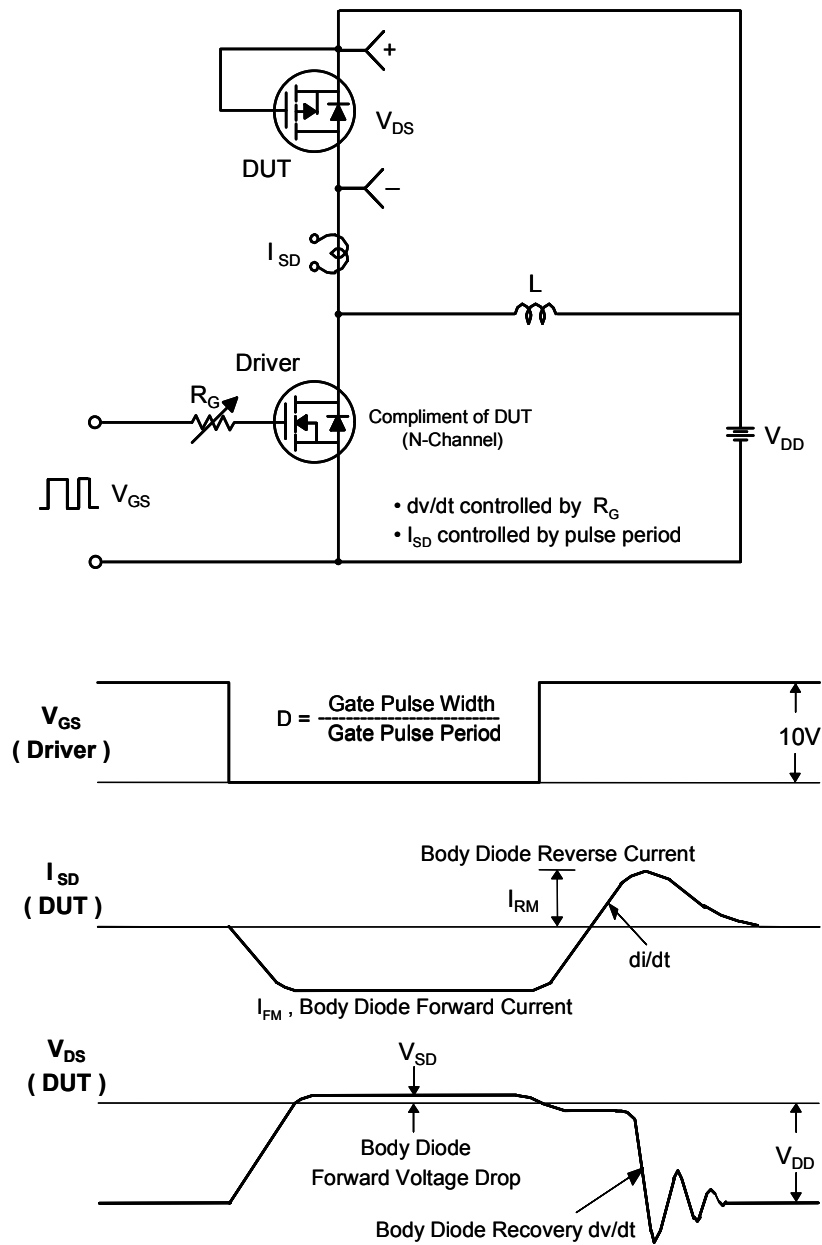
Gate Charge Test Circuit & Waveform

12V 200nF 50KΩ 300nF

Same Type as DUT

V_{GS}

DUT

-3mA

V_{DS}

V_{GS}

-10V

Q_g

Q_{gs} Q_{gd}

Charge

Resistive Switching Test Circuit & Waveforms

V_{DS} R_L

V_{GS}

R_G

-10V

DUT

V_{DD}

t_{on} t_{off}

$t_{d(on)}$ t_r $t_{d(off)}$ t_f

V_{GS} 10%

V_{DS} 90%
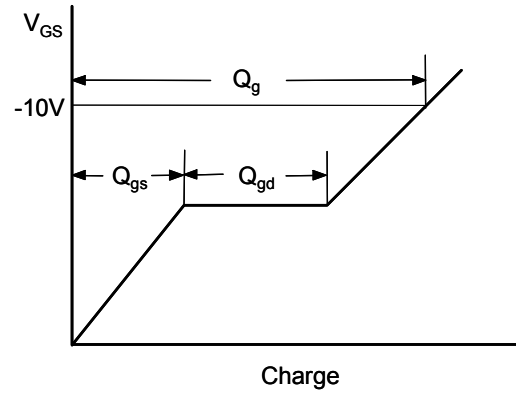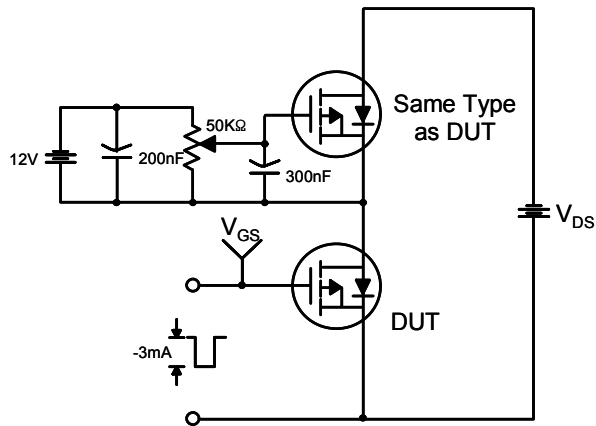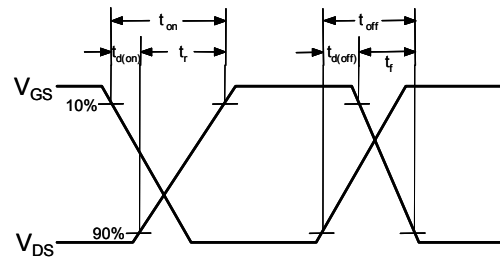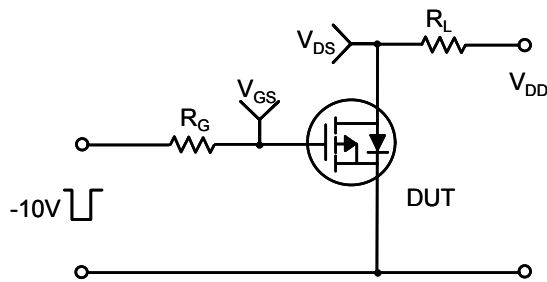
Unclamped Inductive Switching Test Circuit & Waveforms

V_{DS} L

I_D

R_G

-10V

t_p

DUT

V_{DD}

$$E_{AS} = \frac{1}{2} L I_{AS}^2 \frac{BV_{DSS}}{BV_{DSS} - V_{DD}}$$

t_p Time

V_{DD}

$I_D (t)$

$V_{DS} (t)$

I_{AS}

BV_{DSS}
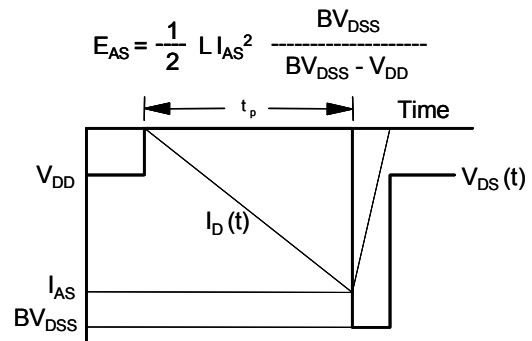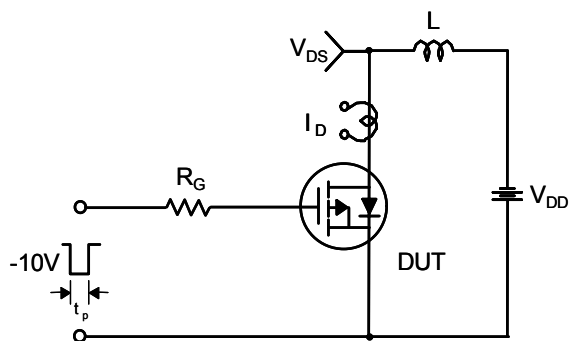
Peak Diode Recovery dv/dt Test Circuit & Waveforms

V_{DS}

DUT

I_{SD}

L

Driver

R_G

Compliment of DUT
(N-Channel)

V_{DD}

V_{GS}

• dv/dt controlled by R_G
• I_{SD} controlled by pulse period

V_{GS}
(Driver)

$$D = \frac{\text{Gate Pulse Width}}{\text{Gate Pulse Period}}$$

10V

I_{SD}
(DUT)

Body Diode Reverse Current

I_{RM}

di/dt

I_{FM} , Body Diode Forward Current

V_{DS}
(DUT)

V_{SD}

Body Diode
Forward Voltage Drop

V_{DD}

Body Diode Recovery dv/dt

10.67
9.65

-A-

1.68
1.00

4

9.65
8.38

1.78 MAX

0.25 MAX
PLASTIC BODY
STUB

4

2

1   3

2

1   3

(2.12)

1.78
1.14

0.99
0.51

⊕ | 0.25 Ⓜ | B | AⓂ

5.08

FRONT VIEW - DIODE PRODUCTS VERSION
ALTERNATIVE SUPPLIER DETAIL

10.67

9.45

10.00

3.80

1.05

5.08
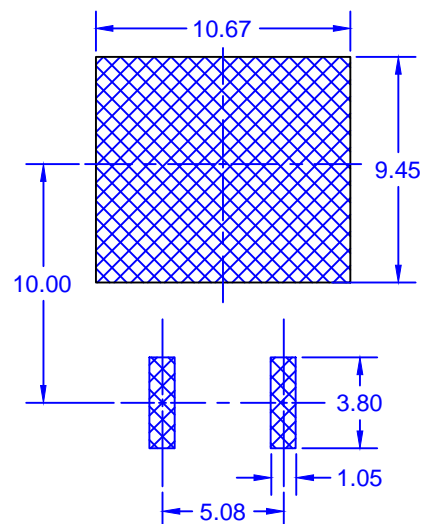
LAND PATTERN RECOMMENDATION
UNLESS NOTED, ALL DIMS TYPICAL

6.22 MIN

4

6.86 MIN

4

-B-

4.83
4.06

1.65
1.14

15.88
14.61

SEE
DETAIL A

2

3   1

2

3   1

BACK VIEW - DIODE PRODUCTS VERSION
ALTERNATIVE SUPPLIER DETAIL

GAGE PLANE

0.74
0.33

0.25

8°
0°

0.25 MAX

2.79
1.78

8°
0°

⌒ | 0.10 | B

(5.38)

SEATING
PLANE

DETAIL A, ROTATED 90°
SCALE: 2X
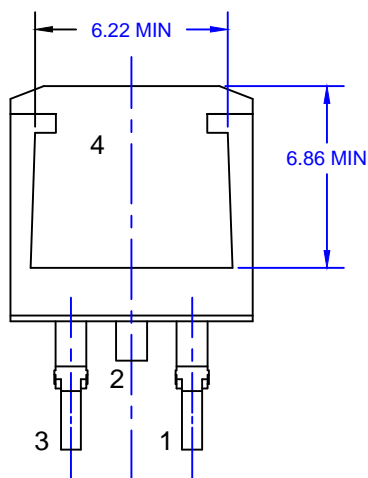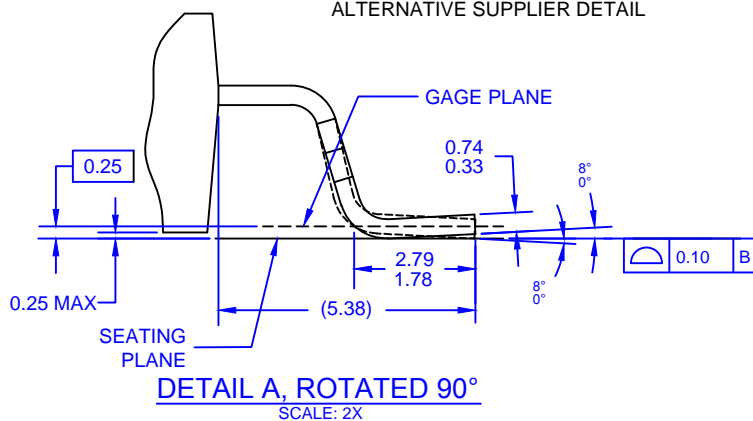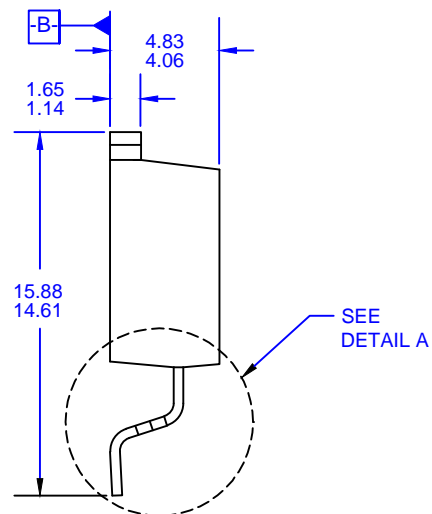
NOTES: UNLESS OTHERWISE SPECIFIED
  A) ALL DIMENSIONS ARE IN MILLIMETERS.
  B) REFERENCE JEDEC, TO-263, VARIATION AB.
  C) DIMENSIONING AND TOLERANCING PER
      DIMENSIONING AND TOLERANCING PER
      ASME Y14.5 - 2009.
  D) LOCATION OF THE PIN HOLE MAY VARY
      (LOWER LEFT CORNER, LOWER CENTER
      AND CENTER OF THE PACKAGE).
  E) LANDPATTERN RECOMMENDATION PER IPC
      TO254P1524X482-3N
  F) FILENAME: TO263A02REV8

FAIRCHILD.

PUBLICATION ORDERING INFORMATION

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