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Please note: As part of the Fairchild Semiconductor integration, some of the Fairchild orderable part numbers will need to change in order to meet ON Semiconductor's system requirements. Since the ON Semiconductor product management systems do not have the ability to manage part nomenclature that utilizes an underscore (_), the underscore (_) in the Fairchild part numbers will be changed to a dash (-). This document may contain device numbers with an underscore (_). Please check the ON Semiconductor website to verify the updated device numbers. The most current and up-to-date ordering information can be found at www.onsemi.com. Please email any questions regarding the system integration to Fairchild_questions@onsemi.com.

FAIRCHILD

July 2016

BSS138_F085

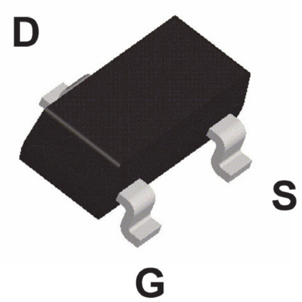
N-Channel Logic Level Enhancement Mode Field Effect Transistor

General Description

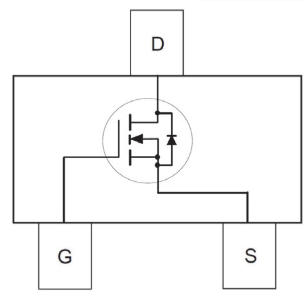
These N-Channel enhancement mode field effect transistors are produced using Fairchild's proprietary, high cell density, DMOS technology. These products have been designed to minimize on-state resistance while provide rugged, reliable, and fast switching performance.These products are particularly suited for low voltage, low current applications such as small servo motor control, power MOSFET gate drivers, and other switching applications.

Features

- Automotive Qualified
- 0.22 A, 50 V. RDS(ON) = 3.5Ω @ VGS = 10 V
  RDS(ON) = 6.0Ω @ VGS = 4.5 V
- High density cell design for extremely low RDS(ON)
- Rugged and Reliable
- Compact industry standard SOT-23 surface mount package



SOT-23



Absolute Maximum Rations

T_A = 25°C unless otherwise noted

Symbol	Parameter		Units	Symbol
V_{DSS}	Drain-Source Voltage		50	V
V_{GSS}	Gate-Source Voltage		±20	V
I_D	Drain Current – Continuous	(Note 1)	0.22	A
	– Pulsed		0.88	
P_D	Maximum Power Dissipation	(Note 1)	0.36	W
	Derate Above 25°C		2.8	mW/°C
T_J, T_{STG}	Operating and Storage Junction Temperature Range		–55 to +150	°C
T_L	Maximum Lead Temperature for Soldering Purposes, 1/16" from Case for 10 Seconds		300	°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1)	350	°C/W

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
SS	BSS138_F085	7"	8mm	3000 units

Electrical Characteristics

T_A = 25°C unless otherwise noted

Off Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
BV_{DSS}	Drain–Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 μA	50			V
ΔBV_{DSS} / ΔT_J	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, Referenced to 25°C		72		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 50V, V_{GS} = 0 V			0.5	μA
		V_{DS} = 50V, V_{GS} = 0 V, T_J = 125°C			5	μA
		V_{DS} = 30V, V_{GS} = 0 V			100	nA
I_{GSS}	Gate–Body Leakage	V_{GS} = ±20V, V_{DS} = 0 V			±100	nA

On Characteristics (Note2)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 1 mA	0.8	1.3	1.5	V
$\Delta V_{GS(th)}$ / ΔT_J	Gate Threshold Voltage Temperature Coefficient	I_D = 1 mA, Referenced to 25°C		-2		mV/°C
$R_{DS(on)}$	Static Drain–Source On–Resistance	V_{GS} = 10 V, I_D = 0.22 A		0.7	3.5	Ω
		V_{GS} = 4.5 V, I_D = 0.22 A		1.0	6.0	
		V_{GS} = 10 V, I_D = 0.22 A, T_J = 125°C		1.1	5.8	
$I_{D(on)}$	On–State Drain Current	V_{GS} = 10 V, V_{DS} = 5 V	0.2			A
g_{FS}	Forward Transconductance	V_{DS} = 10 V, I_D = 0.22 A	0.12	0.5		S

Dynamic Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
C_{iss}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1.0 MHz		27		pF
C_{oss}	Output Capacitance			13		pF
C_{rss}	Reverse Transfer Capacitance			6		pF
R_G	Gate Resistance	V_{GS} = 15 mV, f = 1.0 MHz		9		Ω

Switching Characteristics (Note2)

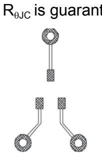
Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 30 V, I_D = 0.29 A, V_{GS} = 10 V, R_{GEN} = 6 Ω		2.8	5.8	ns
t_r	Turn-On Rise Time			2.1	4.4	ns
$t_{d(off)}$	Turn-Off Delay Time			9.6	19.2	ns
t_f	Turn-Off Fall Time			8.4	16.8	ns
Q_g	Total Gate Charge	V_{DS} = 25 V, I_D = 0.22 A, V_{GS} = 10 V		1.7	2.4	nC
Q_{gs}	Gate-Source Charge			0.1		nC
Q_{gd}	Gate-Drain Charge			0.4		nC

Drain–Source Diode Characteristics and Maximum Ratings

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
I_S	Maximum Continuous Drain–Source Diode Forward Current				0.22	A
V_{SD}	Drain–Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 0.44 A (Note 2)		0.8	1.4	V

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta JA}$ is determined by the user's board design.



a) 350°C/W when mounted on a minimum pad.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

Typical Performance Characteristics

Figure 1. On-Region Characteristics

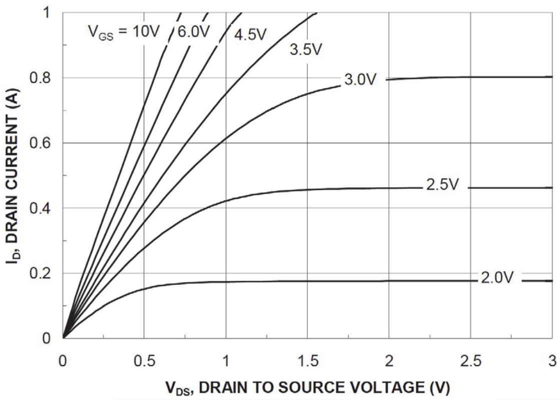


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage

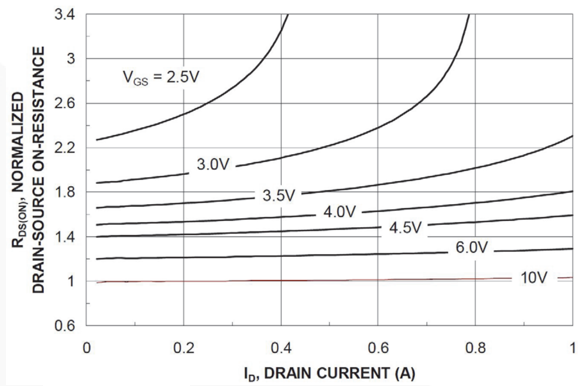


Figure 3. On-Resistance Variation with Temperature

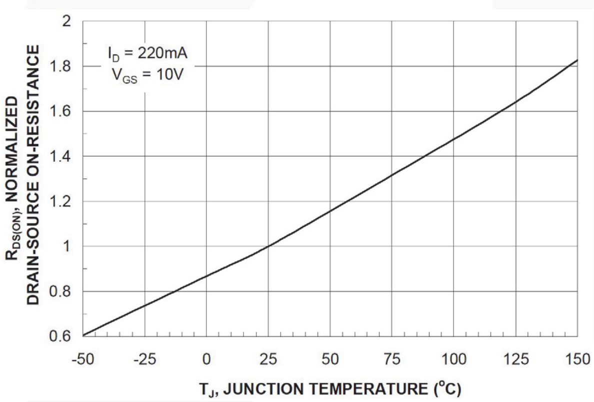


Figure 4. On-Resistance Variation with Gate-to-Source Voltage

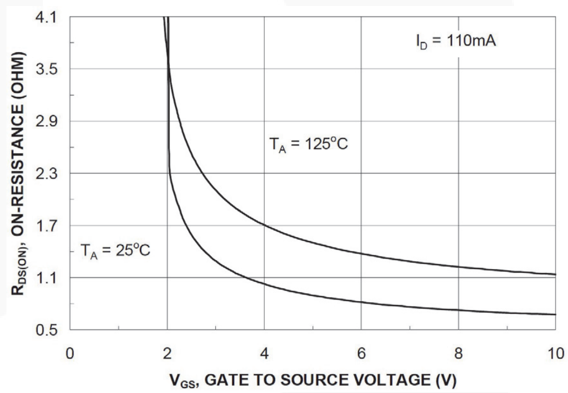


Figure 5. Transfer Characteristics

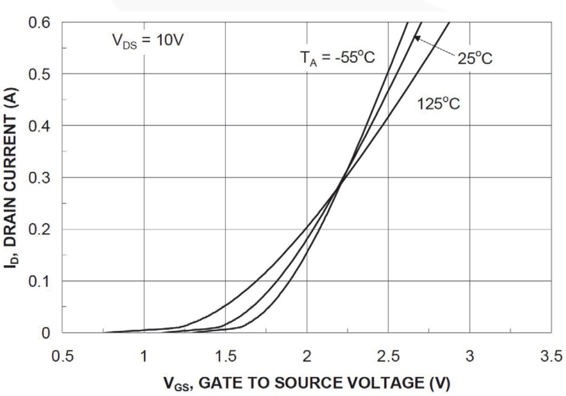
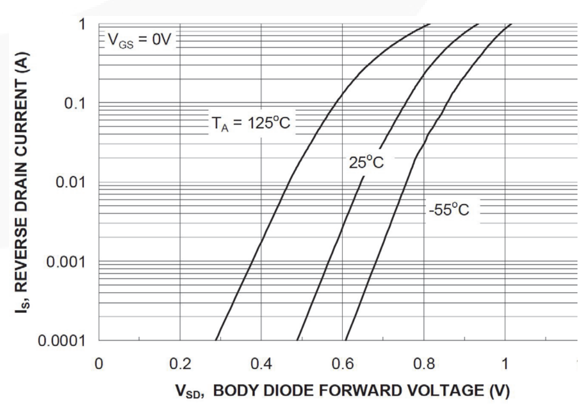


Figure 5. Body Diode Forward Voltage Variation with Source Current and Temperature



Typical Performance Characteristics

Figure 7. Gate Charge Characteristics

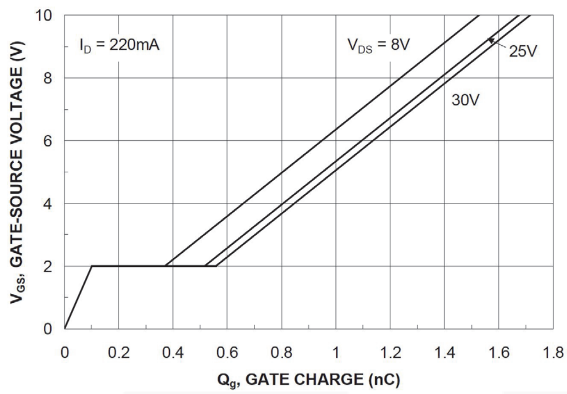


Figure 8. Capacitance Characteristics

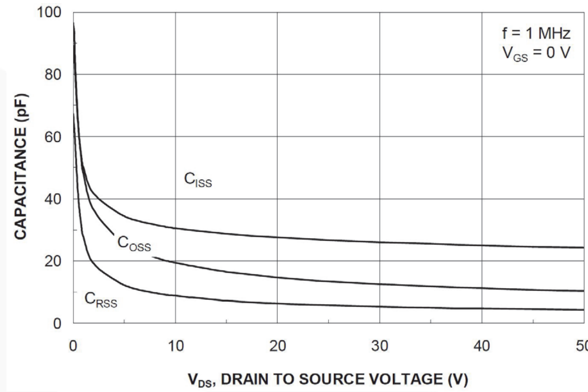


Figure 9. Maximum Safe Operating Area

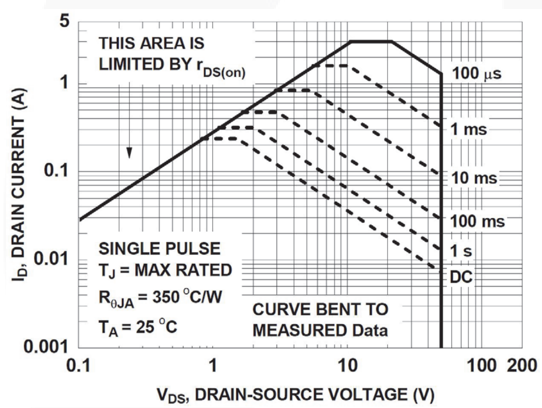


Figure 10. Single Pulse Maximum Power Dissipation

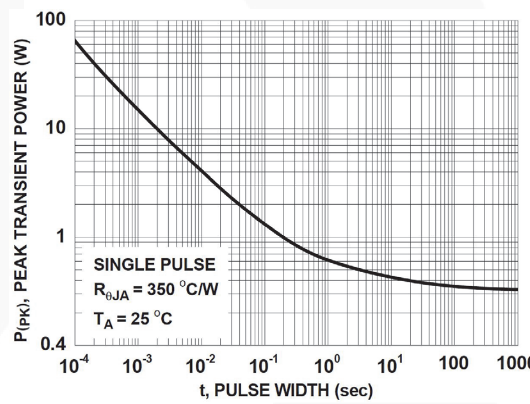
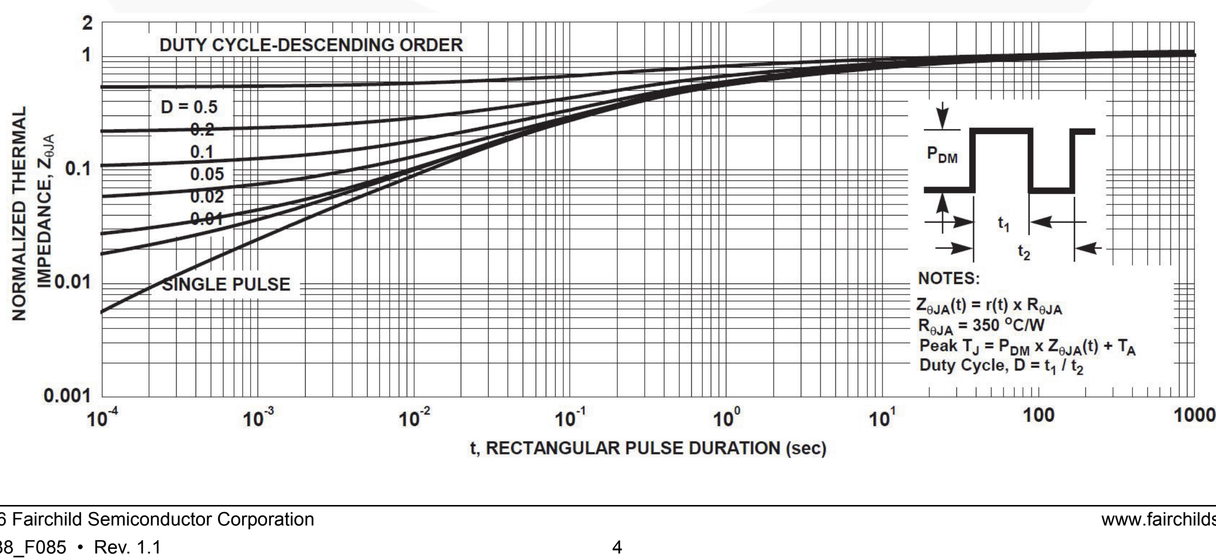
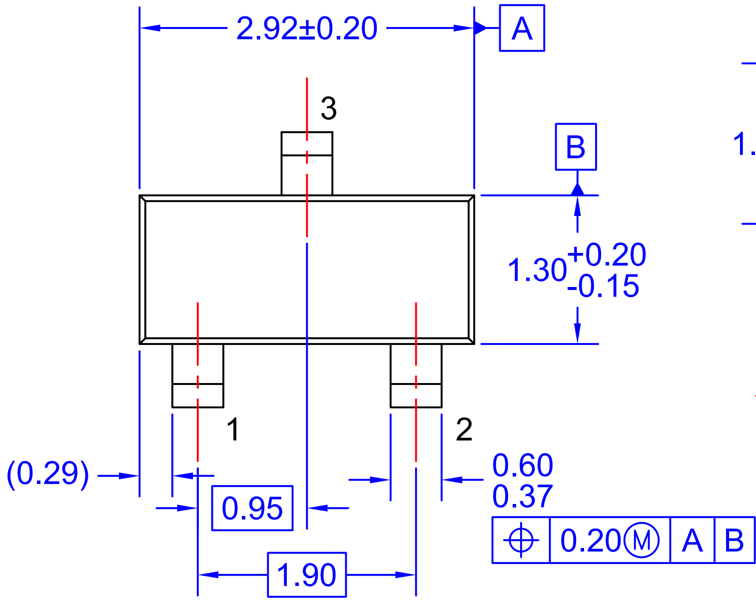


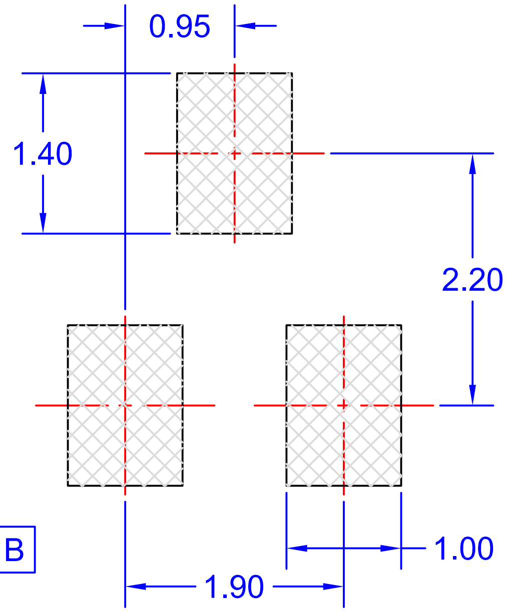
Figure 11. Transient Thermal Response Curve

Thermal characterization performed using the conditions described in Note 1a

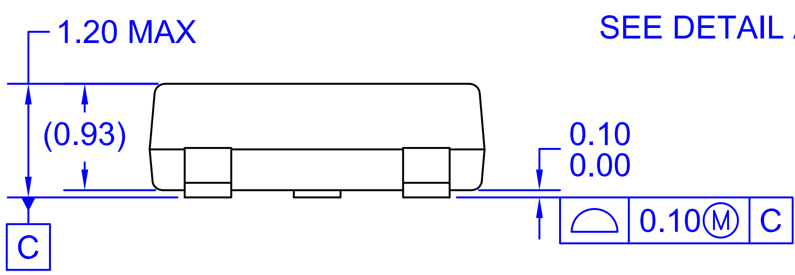
Transient thermal response will change depending on the circuit board design

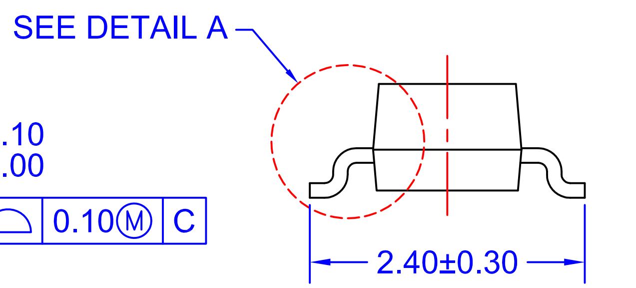


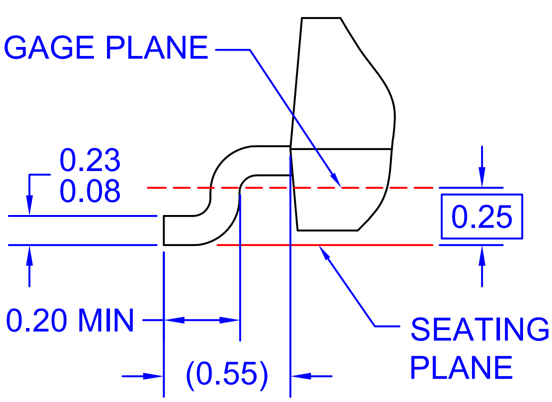




LAND PATTERN RECOMMENDATION







DETAIL A
SCALE: 2X

NOTES: UNLESS OTHERWISE SPECIFIED

A) REFERENCE JEDEC REGISTRATION TO-236, VARIATION AB, ISSUE H.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS ARE INCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR EXTRUSIONS.
D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M - 2009.
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