

### Features

- CDR/Reclocker with 4:1 input multiplexer
- Integrated loop filter and terminations
- Serial control or hardwired control, JTAG boundary scan
- Low power consumption of 405 mW (all channels active)
- Built-in pattern generator and receiver for module and system testing (PRBS, 8b/10b, Fibre Channel, User Programmable patterns)
- User Selectable Input Equalization and Pre-Emphasis for backplane ISI reduction

### Applications

- HD/SD-SDI Routing Switchers, Distribution amplifiers, and transport systems
- SONET systems and modules
- 10 GBASE-CX4 systems
- Gigabit Ethernet systems
- PCI-Express
- SAS/S-ATA/S-ATA2 systems

### Standards Compliance

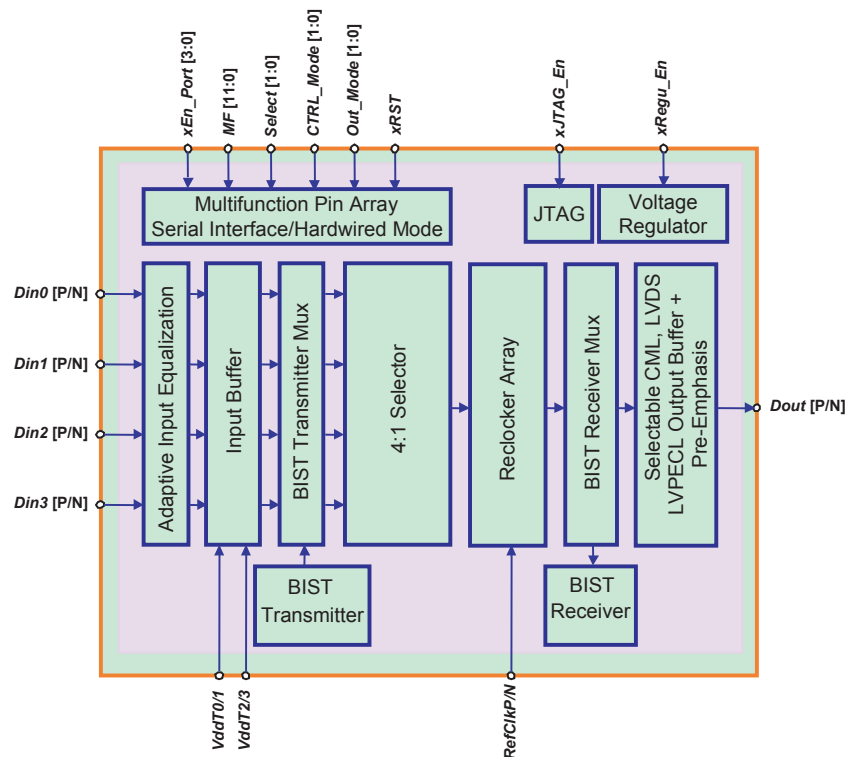
- SMPTE 292M
- SMPTE 259M
- SMPTE 344M
- SMPTE 424M

The M21262 is a CDR/reclocker with 4:1 input multiplexer for telecom, datacom, and HD/SD video applications. Each output channel has an independent multi-rate CDR capable of operating at data rates between 42 Mbps and 3.2 Gbps.

The M21262 can be controlled either through hardwired pins or through a serial programming interface. The hardwired mode eliminates the need for an external microcontroller to configure the device. The serial programming interface allows complete control of the device and is available as a two-wire or a four-wire interface.

The M21262 device supports JTAG external boundary scan, which includes all of the high-speed I/O as well as the traditional digital I/O.

Functional Block Diagram



### Ordering Information

| Part Number | Package                | Operating Temperature |
|-------------|------------------------|-----------------------|
| M21262-12   | 72-terminal, 10mm, MLF | -40 °C to 85 °C       |
| M21262G-12* | 72-terminal, 10mm, MLF | -40 °C to 85 °C       |

\* The letter "G" designator after the part number indicates that the device is RoHS compliant. The RoHS compliant devices are backwards compatible with 225 °C reflow profiles.

### Revision History

| Revision | Level       | Date       | Description                                                                                                                                                                                                   |
|----------|-------------|------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| V3       | Release     | May 2015   | Updated logos and page layout. No content changes.                                                                                                                                                            |
| C (V2)   | Release     | April 2008 | Added SMPTE 424M in standards compliance list.<br>Revised <a href="#">Section 2.8</a> .<br>Added 2 x HD-SDI data in <a href="#">Table 1-6</a> , <a href="#">Table 1-15</a> , and <a href="#">Table 2-14</a> . |
| B (V1)   | Release     | April 2007 | Removed M21261 from data sheet.<br>Added support for datacom/telecom rates up to 3.2 Gbps.<br>Updated specification tables.<br>Updated register tables.                                                       |
| A (V1P)  | Preliminary | April 2004 | Initial release.<br>Original Document Number 21261-DSH-001-A.                                                                                                                                                 |

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# 1.0 Functional Description

## 1.1 Detailed Feature Descriptions

### 1.1.1 Conventions

Throughout this data sheet, physical pins will be denoted in ***bold italic*** print. An array of pins can be called by each individual pin name (e.g. ***MF0***, ***MF1***, ***MF2***, ***MF3***, and ***MF6***) or as an array (e.g. ***MF*** [6, 3:0]). The M21262 control is accessed through registers that employ an 8-bit address and an 8-bit data scheme. Registers are denoted in italic print, (e.g. *TestRegister*) and individual bits within the register will be called out as *TestRegister* [4:3] to denote the 4<sup>th</sup> and 3<sup>rd</sup> bit where bit 0 is the LSB and bit 7 is the MSB. Many features of the device are bit mapped within a register; if the status of the other bits are uncertain, it is recommended that the user reads the value from the register before writing, to assure only the desired bits change. Writing in the same value to the bits within a register does not cause glitches to the unchanged features. The addresses for the registers as well as their functions can be found in detail in [Chapter 3](#). The purpose of the text description is to highlight the features of the registers. For redundant items, such as the channel number, the registers will have a nomenclature of *TestReg\_0* for channel 0, *TestReg\_1* for channel 1, *TestReg\_2* for channel 2, *TestReg\_3* for channel 3.

### 1.1.2 Reset

Upon application of power, the M21262 automatically generates a master reset. At any time, forcing ***xRST*** = L causes the M21262 to enter the master reset state. A master reset can also be initiated through the registers in the serial interface control mode by writing AAh to *Mastreset*. Once a master reset is initiated, all registers are returned to the default values, the internal state machines cleared, and all CDR/RCLK/BIST reset to the out-of-lock condition. After a reset, the register *Mastreset* will automatically return to the default value of 00h.

The CDR/RCLK can be soft reset by setting CDR *RCLK\_ctrlA* [7] = 1. The bit should be returned to 0b for normal operation. After a soft reset, the registers that determine the CDR/RCLK operation options such as data rate, window sizes, etc., remain unchanged and only the CDR/RCLK state machine is reset, resulting in an out-of-lock condition.

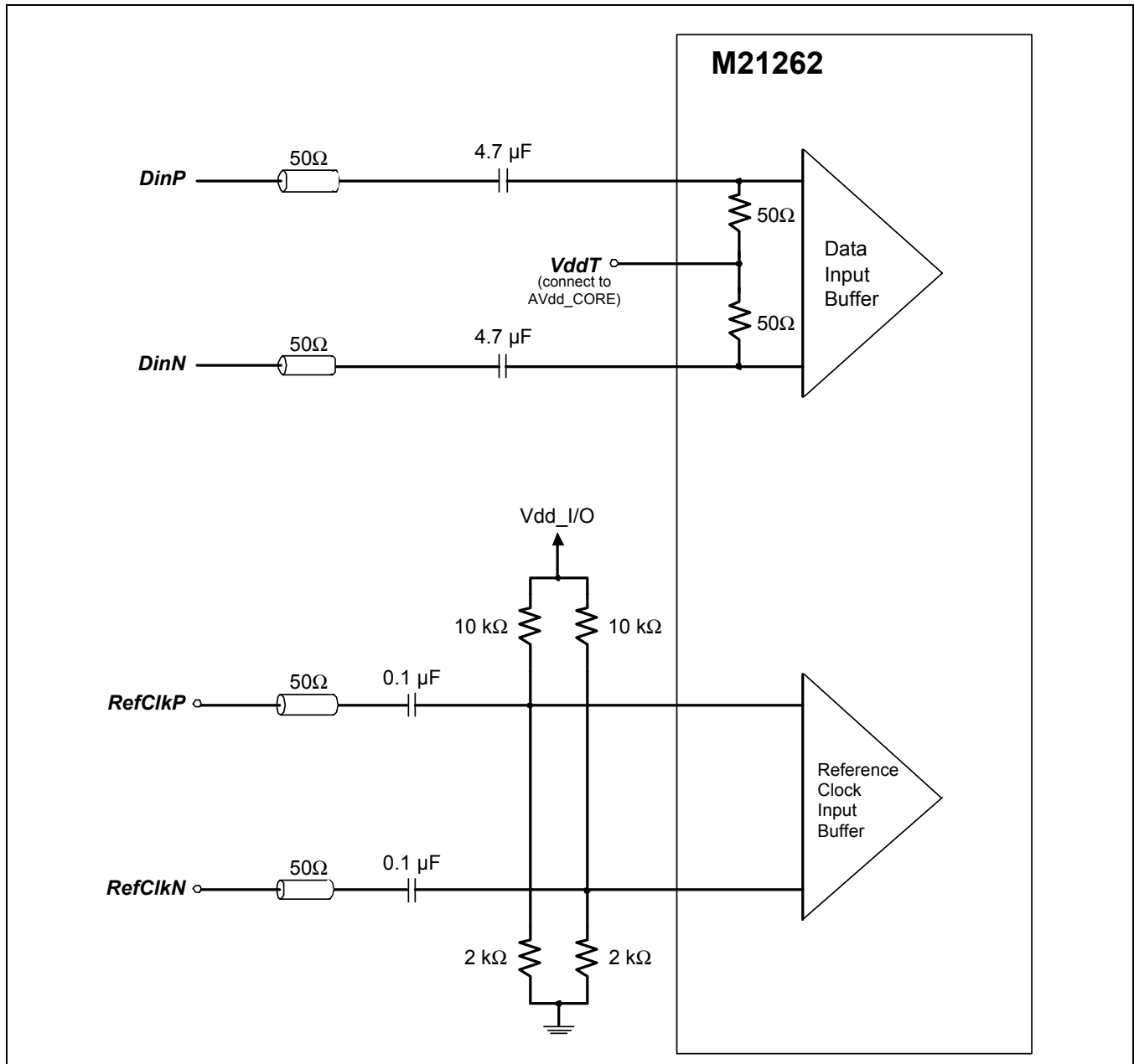
### 1.1.3 Internal Voltage Regulator

The digital and analog core are designed to run at 1.2V, however, for operation from 1.8V to 3.3V, an internal linear regulator is provided. ***xRegu\_En*** = L enables the voltage regulator which uses ***AVdd\_I/O*** and ***DVdd\_I/O*** to generate the required 1.2V for ***AVdd\_Core*** and ***DVdd\_Core***. In this mode, the ***AVdd\_Core*** and ***DVdd\_Core*** pins should be connected to a floating DC low inductance PCB plane and AC bypassed to ***Vss*** using standard decoupling techniques. If desired, ***AVdd\_Core*** and ***DVdd\_Core*** can be separated into individual planes. If 1.2V is available, it can be connected directly to ***AVdd\_Core*** and ***DVdd\_Core***, to save power, by bypassing the internal linear regulator with ***xRegu\_En*** = H. In this case, it is recommended that the ***AVdd\_Core*** and ***DVdd\_Core*** pins be tied together to a common PCB plane, and bypassed to ***Vss*** with standard decoupling techniques.

### 1.1.4 High-Speed Input/Output Pins

The high-speed input data interface is a differential input buffer, similar to a PCML design that is referenced to  $V_{dd\_CORE}$  (1.2V). The high-speed serial differential data (42 Mbps to 3200 Mbps) enters the device via **Din** [3:0, P/N]. Inputs 0 and 1 are internally terminated with  $50\Omega$  to  $V_{ddT0/1}$  and inputs 2 and 3 are terminated with  $50\Omega$  to  $V_{ddT2/3}$ . The  $V_{ddT}$  pins should be connected to **AVDD\_Core** for a proper termination of the inputs. See [Figure 1-1](#) for recommended data and reference clock input coupling circuits.

**Figure 1-1. Recommended Data and Reference Clock Input Coupling Circuitry**



The M21262 supports multiple high-speed output modes. The output modes are selectable with hardwired pins only. The I/O interface is set with **Out\_Mode** [1:0] and the output level with **MF** [9:8] as shown in Table 1-1. In the serial interface mode, the **Out\_ctrl\_N** [7:6] register is used to set the data level, and **Out\_Mode** [1:0] is used to set the interface type. In the serial interface mode, the data output can be enabled with **Out\_ctrl\_N** [2] = 1b (default) and the output data polarity can be flipped by setting **Out\_ctrl\_N** [3] = 1b (default: no inversion). Output data polarity flip is an internal function that would have the same effect as switching the P and N terminals. The recommended **AVdd\_I/O** for the different output interfaces is shown in Table 1-2. The nonstandard lower swing modes for PECL and InfiniBand are provided for lower power dissipation, when desired.

**Table 1-1. Output Interface and Level Mapping (For both hardwired and software modes)**

| Multifunction Pins & Register<br>MF [9:8]<br>Out_ctrl_N [7:6] | PCML Mode<br>Out_Mode [1:0] = 00b | LVDS Mode<br>Out_Mode [1:0] = 01b | PCML+ Mode<br>Out_Mode [1:0] = 11b |
|---------------------------------------------------------------|-----------------------------------|-----------------------------------|------------------------------------|
| 00b                                                           | Off                               | Off                               | Off                                |
| 01b                                                           | 550 mV                            | RRL at 450 mV                     | 900 mV                             |
| 10b                                                           | 900 mV                            | GPL at 650 mV                     | 1200 mV                            |
| 11b                                                           | 1200 mV                           | 1000 mV                           | 1500 mV                            |

**Table 1-2. Output Interface and Recommended AVdd\_I/O Range**

| Output Logic     | AVdd_I/O Range (V) |
|------------------|--------------------|
| Off              | 1.8–3.3            |
| PCML at 550 mV   | 1.8–3.3            |
| PCML at 900 mV   | 1.8–3.3            |
| PCML at 1200 mV  | 1.8–3.3            |
| PCML+ at 1500 mV | 1.8–3.3            |
| LVDS GPL         | 1.8–3.3            |
| LVDS RRL         | 1.8–3.3            |

### 1.1.5 Selector Settings

Table 1-3 details the selector configuration for each setting for the hardwired pins **Select\_Mode**[1:0].

The M21262 allows the user to route any of the four inputs to the output channel. The selector can be configured through the control register or through the hardwired pins **Select\_Mode**[1:0].

Table 1-3. Selector Configuration Settings

| Mode 0 | Mode 1 | Output  |
|--------|--------|---------|
| 0      | 0      | input 0 |
| 0      | 1      | input 1 |
| 1      | 0      | input 2 |
| 1      | 1      | input 3 |

### 1.1.6 Reclocker Reference Frequency

An external reference clock is applied to **RefClk**[P/N] to enable frequency acquisition in the Reclocker. PCML, LVTTTL, CMOS are examples of the wide variety of interfaces supported for the reference clock. The inputs contain a DC-coupled 100Ω differential termination between **RefClkP** and **RefClkN** along with a 100 kΩ pull-down on each terminal to **Vss**. After this termination/pull-down block, the inputs are AC coupled internally. The common-mode and allowable voltage swings are specified in Table 2-10. The **RefClk** common-mode must be above 250 mV, which may require external pull-ups, in the case of external AC coupling.

### 1.1.7 Multifunction Pins Overview

The M21262 is designed to be an extremely versatile device, with many user selectable options in the CDR/RCLK and I/O to optimize performance. All of these options can be accessed and controlled through the serial interface. The serial interface I/O pins and address pins are mapped to the multifunction pins **MF** [11:0]. A subset of the key features for most applications, such as standard data rates, I/O levels, etc., can be selected through **MF** [11:0] in the hardwired mode. The hardwired mode does not require the use of the serial interface. In this mode, upon power up (auto reset on power up), the M21262 function is determined by the status of the hardwired pins. During operation, the hardwired pins can change states, which would cause the device to follow with the appropriate action. Another feature of the multifunction pins is to support JTAG testing of this device during PCB manufacturing.

The various control and test modes of this device are selected with three pins: **CTRL\_Mode** [1:0], and **xJTAG\_En**. **xJTAG\_En** = L overrides **CTRL\_Mode** [1:0], and puts the device in JTAG test mode, while **xJTAG\_En** = H allows **CTRL\_Mode** [1:0] to determine the M21262 control mode, as summarized in Table 1-4.

Table 1-4. Mode Select Pins

| Pin                    | JTAG Test Mode | Hardwired Mode | 4-Wire Serial | I <sup>2</sup> C-Compatible 2-Wire Serial |
|------------------------|----------------|----------------|---------------|-------------------------------------------|
| <b>xJTAG_En</b>        | L              | H              | H             | H                                         |
| <b>CTRL_Mode</b> [1:0] | no impact      | 11b            | 00b           | 01b                                       |

### 1.1.8 Multifunction Pins Defined for Hardwired Mode

In the hardwired mode, a subset of options in the M21262 can be accessed with hardwired physical pins, as defined in [Table 1-5](#). The hardwired bit rates along with the default reference clock frequency are shown in [Table 1-5](#). [Table 1-6](#) provides the default reference clock frequency associated with each hardwired data rate.

**Table 1-5. Multifunction Pins for Hardwired Mode**

| Pin         | Name            | Function                | Description                                                                                                                                                      |
|-------------|-----------------|-------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>MF0</b>  | Rate_Sel_0      | Data rate selection     | CDR/Reclocker data rate select (see <a href="#">Table 1-6</a> for description)                                                                                   |
| <b>MF1</b>  | Rate_Sel_1      | Data rate selection     | CDR/Reclocker data rate select (see <a href="#">Table 1-6</a> for description)                                                                                   |
| <b>MF2</b>  | Rate_Sel_2      | Data rate selection     | CDR/Reclocker data rate select (see <a href="#">Table 1-6</a> for description)                                                                                   |
| <b>MF3</b>  | Rate_Sel_3      | Data rate selection     | CDR/Reclocker data rate select (see <a href="#">Table 1-6</a> for description)                                                                                   |
| <b>MF4</b>  | xPre_Emp_En     | Pre-emphasis control    | L = Pre-emphasis enable<br>H = Pre-emphasis disable                                                                                                              |
| <b>MF5</b>  | RSVD_Int_0      | MACOM internal          | Internal use only                                                                                                                                                |
| <b>MF6</b>  | RSVD_Int_1      | MACOM internal          | Internal use only                                                                                                                                                |
| <b>MF7</b>  | xPol_Flip_En    | Data polarity flip      | L = Data polarity flip<br>H = Standard data polarity                                                                                                             |
| <b>MF8</b>  | Out_Level_[1:0] | Output level selection  | 00b: All outputs disabled<br>01b: 500 mV (CML)<br>10b: 900 mV (CML)<br>11b: 1200 mV (CML)<br>See <a href="#">Table 1-1</a> for the other output interface modes. |
| <b>MF9</b>  |                 | Output level selection  |                                                                                                                                                                  |
| <b>MF10</b> | xEQ_En          | Equalization control    | L = Input equalization enabled<br>H = Input equalization disabled                                                                                                |
| <b>MF11</b> | xRCLK_BYP_En    | CDR/RCLK bypass control | L = CDR/Reclocker bypassed and powered down<br>H = CDR/Reclocker enabled                                                                                         |

**Table 1-6. Hardwired Bit Rates and Associated Reference Frequencies**

| Pins<br>MF[3:0] | Application            | Bit Rate (Mbps) | Reference Frequency (MHz) |
|-----------------|------------------------|-----------------|---------------------------|
| 0000            | 2 x HD-SDI             | 2967/2970       | 12.0                      |
| 0001            | HD-SDI                 | 1485 /1483.5    | 12.0                      |
| 0010            | 2 x SD-SDI             | 540             | 12.0                      |
| 0011            | Progressive Scan Video | 360             | 12.0                      |
| 0100            | SD-SDI                 | 270             | 12.0                      |
| 0101            | Legacy Comp Video      | 177             | 12.0                      |
| 0110            | Legacy Comp Video      | 143             | 12.0                      |

### 1.1.9 Multifunction Pins: Four-Wire Serial Interface

The second serial interface mode is a four-wire programming interface that has been traditionally used on MACOM earlier generation crosspoints and CDRs and is capable of higher speed operation than the two-wire interface. The interface consists of a unidirectional clock and a data input and data output line. For use with multiple ICs, a serial interface chip select pin is provided. Table 1-7 illustrates how the four-wire serial interface maps into the multifunction pins. This serial interface can operate with a maximum clock rate of 20 MHz.

**Table 1-7. Multifunction Pins for Four-Wire Interface**

| Pin  | Function | Description             |
|------|----------|-------------------------|
| MF4  | SDI      | Serial Data In          |
| MF5  | xCS      | Chip Select, active low |
| MF10 | SCLK     | Clock                   |
| MF11 | SDO      | Serial Data Out         |

The serial I/O shifts data in from the external controller on the rising edge of **SCLK**. The serial I/O operation is gated by **xCS**. Data is shifted in on **SDI** on the falling edge of **SCLK**, and shifted out on **SDO** on the rising edge of **SCLK**. To address a register, a 10-bit input consists of the first bit (Start Bit, SB = 1), the second bit (Operation Bit, OP = 1 for read, = 0 for write), followed by the 8-bit ADDR (MSB first) as shown in Figure 1-2.

**Figure 1-2. Serial Word Format**

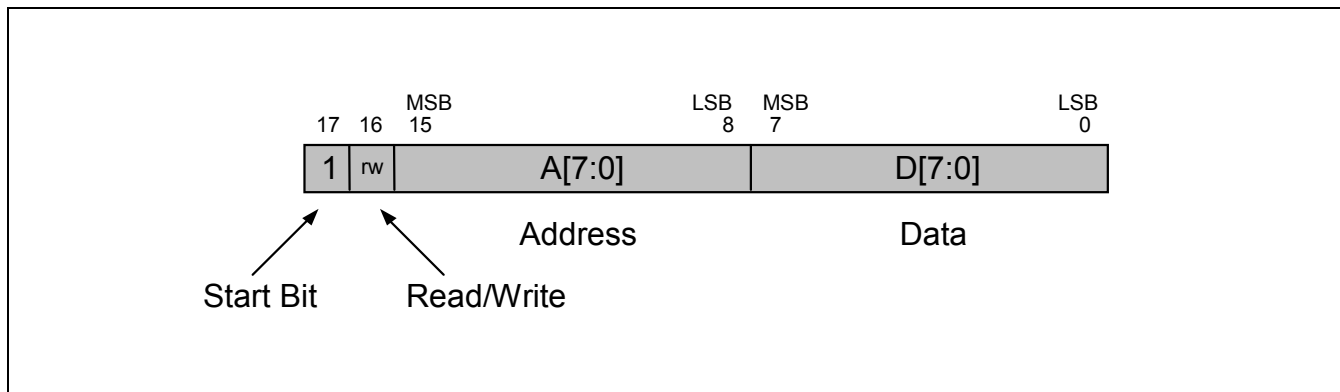


Figure 1-3 illustrates the Serial Write Mode. To initiate a Write sequence, **xCS** goes low before the falling edge of **SCLK**. On each falling edge of the clock, the 18-bits consisting of the SB = 1, OP = 0, ADDR, and DATA, are latched into the input shift register. The rising edge of **xCS** must occur before the falling edge of **SCLK** for the last bit. Upon receipt of the last bit, one additional cycle of **SCLK** is necessary before DATA transfers from the input shift register to the addressed register. If consecutive read/write cycles are being performed, it is not necessary to insert an extra clock cycle between read/write cycles, however one extra clock cycle is needed after the last data bit of the last read/write cycle.

**Figure 1-3. Serial WRITE Mode**

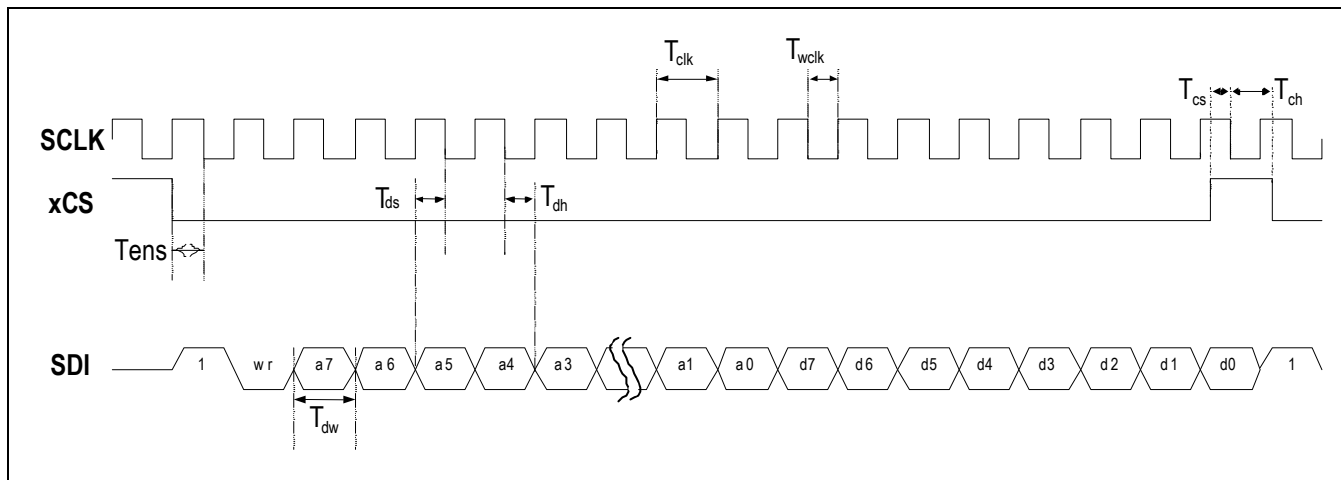
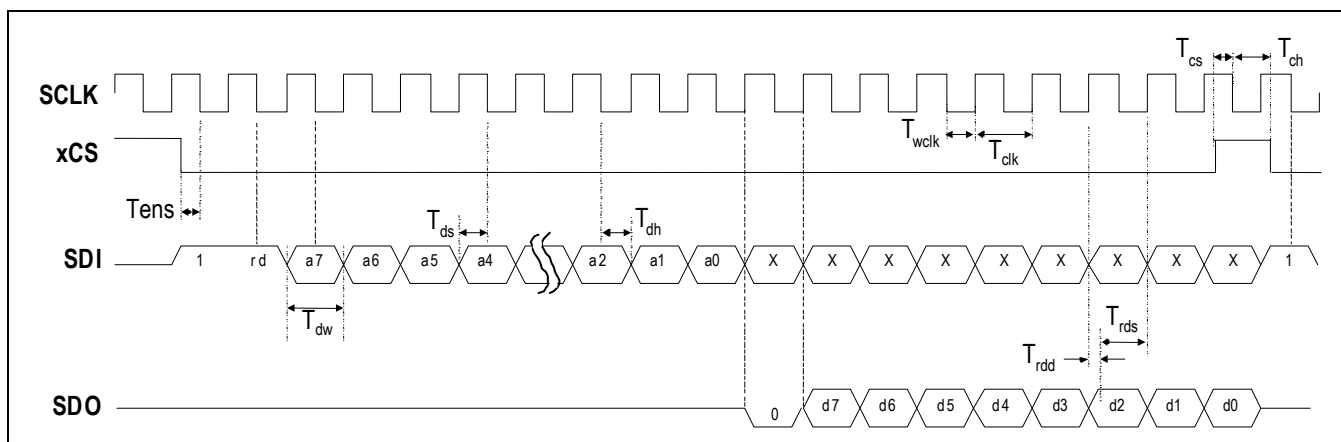


Figure 1-4 illustrates the Serial Read mode in where **xCS** goes low before the falling edge of **SCLK**. On each falling edge of **SCLK**, the 10-bits consisting of SB = 1, OP = 1, and the 8-bit ADDR are written to the serial input shift register and copied to the serial output shift register. On the next rising edge after the address LSB, the SB and 8-bits of the DATA are shifted out. The SB for a Read is always 0.

**Figure 1-4. Serial READ Mode**



On a Write cycle, any bits that follow the expected number of bits are ignored, and only the first 16-bits following SB and OP are used. On a Read cycle, any extra clock cycles will result in the repeat of the data LSB. An invalid SB or OP renders the operation undefined. The falling edge of **xCS** always resets the serial operation for a new Read or Write cycle.

The timing diagrams for the serial write and read operations are shown in Figure 1-3 and Figure 1-4, respectively. Table 1-8 contains the specifications for the various timing parameters for the serial programming interface.

Table 1-8. Serial Interface Timing—Specified at Recommended Operating Conditions

| Symbol     | Item                      | Notes | Minimum | Typical | Maximum  | Units |
|------------|---------------------------|-------|---------|---------|----------|-------|
| $t_{dw}$   | Data width                | —     | 14      | —       | —        | ns    |
| $t_{dh}$   | Data hold time            | —     | 5       | —       | —        | ns    |
| $t_{ds}$   | Data setup time           | —     | 5       | —       | —        | ns    |
| $t_{ens}$  | Enable setup time         | —     | 5       | —       | —        | ns    |
| $t_{cs}$   | Chip select setup time    | —     | 2       | —       | Tclk - 2 | ns    |
| $t_{ch}$   | Chip select hold time     | —     | 2       | —       | —        | ns    |
| $t_{rdd}$  | Read data output delay    | —     | 1       | —       | —        | ns    |
| $t_{rds}$  | Read data valid           | —     | 9       | —       | —        | ns    |
| $t_{clk}$  | SCLK period width         | —     | 14      | —       | —        | ns    |
| $t_{wclk}$ | SCLK minimum low duration | —     | 5       | —       | Tclk - 5 | ns    |
| $t_r$      | Output rise time          | 1     | 1       | —       | 4        | ns    |
| $t_f$      | Output fall time          | 1     | 1       | —       | 4        | ns    |

**NOTES:**

1. Edge rate in the high-edge rate mode.
2. Designed for max serial speed of 20 MHz read/write.

### 1.1.10 Two-Wire Serial Interface

The two-wire serial interface is compatible with the I<sup>2</sup>C standard. The M21262 supports the read/write slave-only mode, 7-bit device address field width, and supports the standard rate of 100 Kbps, fast mode of 400 Kbps, and high-speed mode of 3.4 Mbps. The 7-bit address for the device is determined with **MF** [6:0], which allows for a maximum of 124 unique addresses for this device. The four addresses 000001xx should not be used. SDA (**MF11**) and SCL (**MF10**) can drive a maximum of 500 pF each at the maximum rate. During the write mode from the master to the M21262, data is latched into the internal M21262 registers on the rising edge of SCL, during the acknowledge phase (ACK) of communication. Table 1-9 summarizes the multifunction pins for the two-wire serial interface mode. For further information on timing, please see the I<sup>2</sup>C bus specification standard.

Table 1-9. Multifunction Pins for Two-Wire Interface

| Pin  | Function      | Description                                                      |
|------|---------------|------------------------------------------------------------------|
| MF0  | Address bit 0 | 7-bit device address; address bit 0 is LSB, address bit 6 is MSB |
| MF1  | Address bit 1 |                                                                  |
| MF2  | Address bit 2 |                                                                  |
| MF3  | Address bit 3 |                                                                  |
| MF4  | Address bit 4 |                                                                  |
| MF5  | Address bit 5 |                                                                  |
| MF6  | Address bit 6 |                                                                  |
| MF10 | SCL           | Clock input                                                      |
| MF11 | SDA           | Data input/output                                                |

### 1.1.11 JTAG

The M21262 supports JTAG external boundary scan, which includes all of the high-speed I/O, as well as the traditional digital I/O. Table 1-10 shows the multifunction pins signal mapping for JTAG testing.

Table 1-10. Multifunction Pins for JTAG

| Pin  | Function | Description      |
|------|----------|------------------|
| MF8  | TMS      | Test select      |
| MF9  | TDI      | Test data input  |
| MF10 | TCK      | Test clock       |
| MF11 | TDO      | Test data output |

### 1.1.12 Input Deterministic Jitter Attenuators

Each of the four input channels contains an input equalizer to compensate for high-frequency loss. In the hardwired mode, there is the option to set input equalization on or off. In the two-wire serial interface control mode, the default state allows for configurable input equalization settings using *Ineq\_ctrl\_N* [2:0], for which the default setting of 100b is optimized for trace lengths between 10–46 inches.

The input equalization settings have been optimized for a variety of backplane PCB applications, such as board traces and cables. For board traces on FR4, the input equalizer can drive trace lengths of up to 72" at 1.6 Gbps and up to 60" at 3.1875 Gbps. The equalizer has similar high performance on Nelco-13, Arlon 25, Rogers 3003, 4003C, 4340, GeTek PCB materials, and twinaxial cables. The input equalizer was designed to compensate for the deterministic jitter accumulation effects of typical backplane interconnects, which have bandwidths of hundreds of MHz to a few GHz. The equalizers are not expected to make a significant difference in performance with signal data rates less than 1 Gbps.

Another component of input deterministic jitter is inter-symbol interference (ISI) due to DC offsets. By default, a DC servo-like circuit is enabled to correct for this type of deterministic jitter, and can be disabled by setting

*Ineq\_ctrl* [4] = 0b. The DC servo can also be used to track changes in the common mode, for single-ended operation. When the CDR, DC servo, and AIE are all enabled, the jitter tolerance should be greater than 1 UI.

**Figure 1-5. STS-48 waveform after transmission through 76" of PCB traces (input to M21262)**

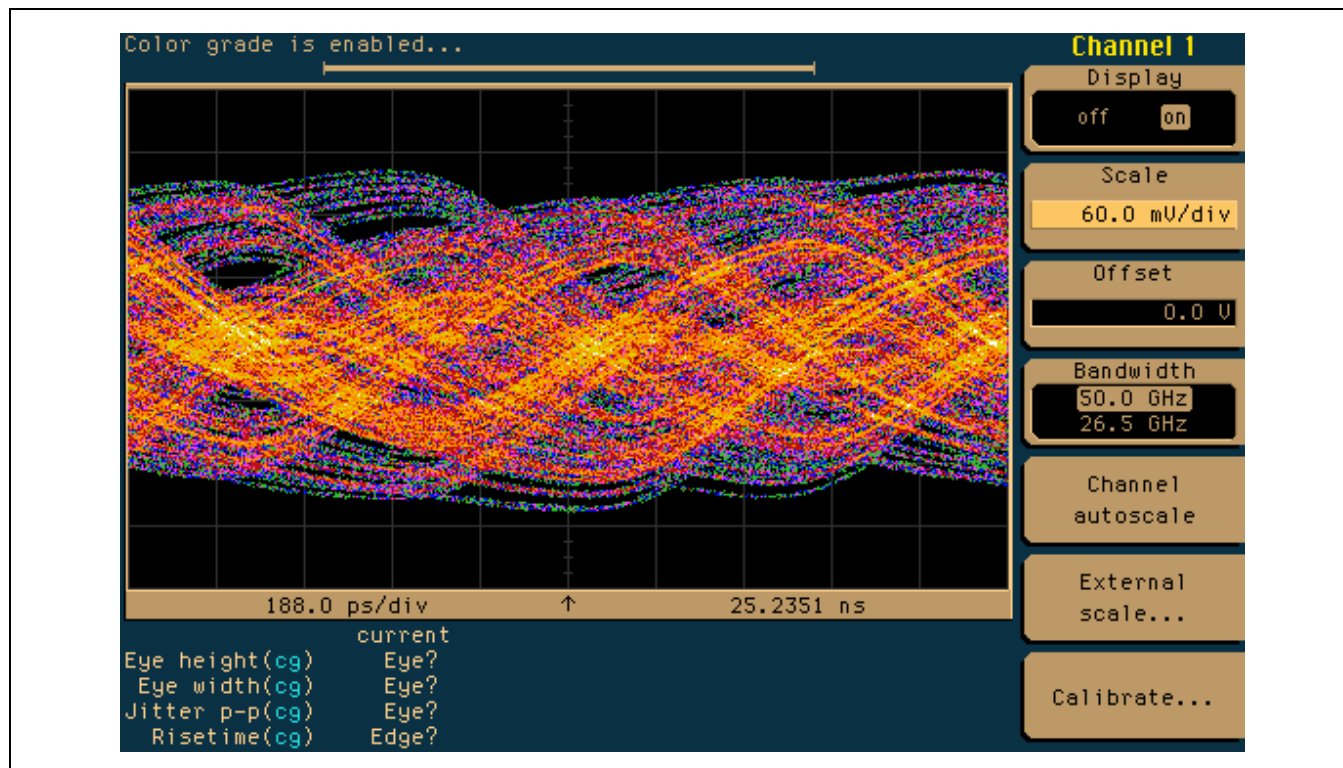
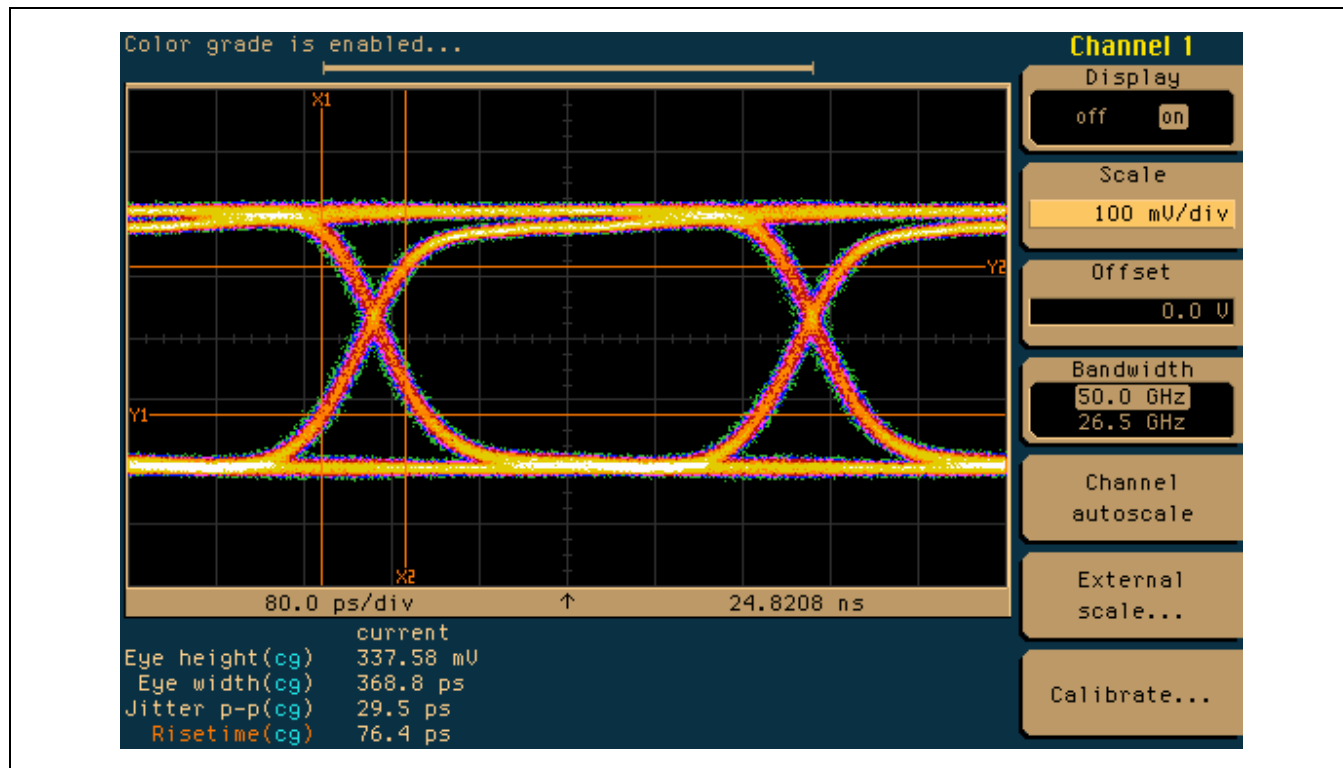


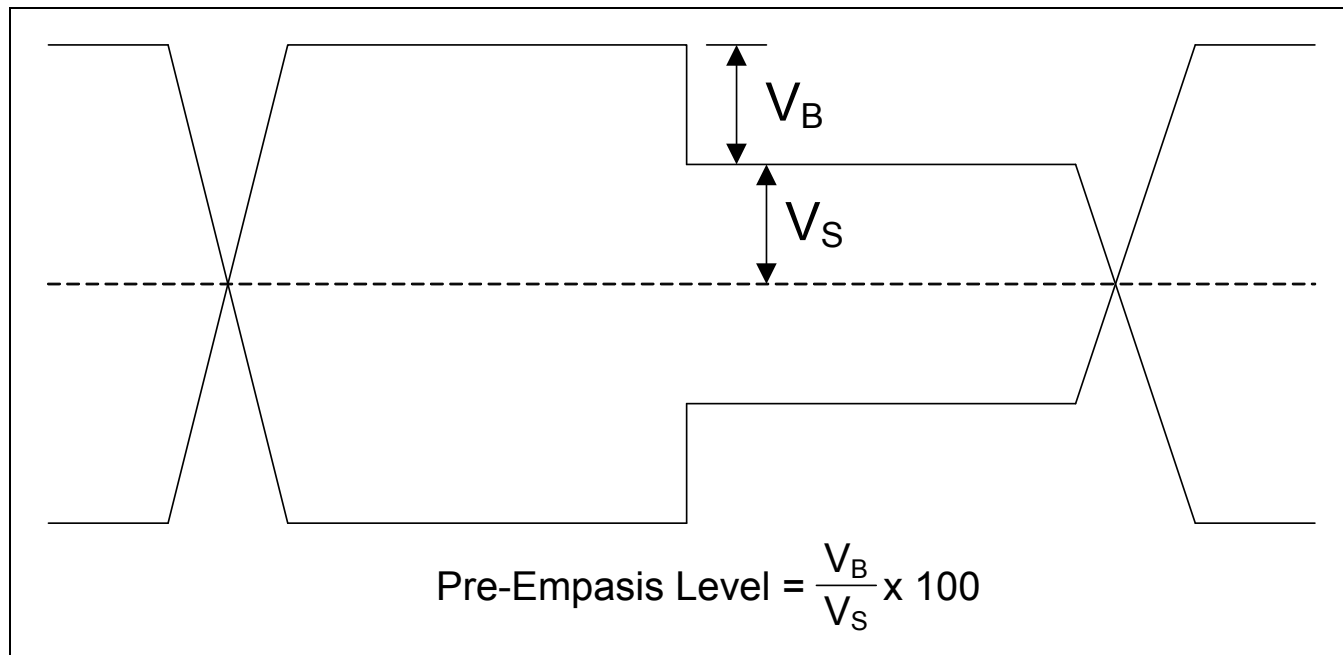
Figure 1-6. STS-48 waveform at M21260 output with input shown in Figure 1-4



### 1.1.13 Output Pre-Emphasis

The output channel contains an output pre-emphasis circuit that can be used to select the optimal pre-emphasis level. The pre-emphasis settings have been optimized for a variety of backplane PCB applications. For board traces on FR4, the pre-emphasis circuit can drive trace lengths up to 60" at 1.6 Gbps. Like the input equalizer settings, the output pre-emphasis circuit has similar high performance on Nelco-13, Arlon 25, Rogers 3003, 4003C, 4340, GeTek PCB materials, and twinaxial cables. The digital pre-emphasis level is selected, for each output channel, with *Preemp\_ctrl* [2:0], and the default value of 000b corresponds to pre-emphasis disabled. The pre-emphasis circuit tracks the signal data rate throughout the multirate range, however, like the input equalizer, it is designed to compensate for the bandwidth limitations of the interconnect, and may not have the desired effects at the low end of the multirate range. When the CDR/RCLK has been disabled or bypassed, analog pre-emphasis must be used in place of digital pre-emphasis. Writing the data value 1b to the register *Preemp\_ctrl* [3] enables analog pre-emphasis, whereas writing the data value 0b to the register *Preemp\_ctrl* [3] enables digital pre-emphasis. Once analog pre-emphasis has been enabled, the boost level may be chosen with *Preemp\_ctrl* [5:4], and the bandwidth may be chosen with *Preemp\_ctrl* [6]. The output pre-emphasis function is available for all data interfaces and levels.

Figure 1-7. Definition of Pre-Emphasis Levels



### 1.1.14 CDR/RCLK Overview

When the CDR/RCLK achieves phase lock onto the incoming data stream, it removes the incoming random jitter above its loop bandwidth. The M21262 output data has extremely low jitter, due to retiming with a very low jitter generation CDR/RCLK. Clock outputs are also provided, but are disabled by default.

Each CDR/RCLK is capable of multirate operation which is achieved by a combination of built in VCO frequency dividers (VCD), Data Rate Dividers (DRD), and a wide VCO tuning range ( $F_{\min} = 2.0$  GHz,  $F_{\max} = 3.2$  GHz). As a result, the allowed input data range is  $F_{\min} / \text{DRD}_{\max}$  to  $F_{\max} / \text{DRD}_{\min}$ . Although the ranges are not continuous, the ranges are deliberately chosen to cover all typical applications.

By default, the loop bandwidth is set to pass 2 x HD-SDI Video and SONET STS-48 specifications, with less than 0.1 dB of bandwidth peaking. Within a given VCO frequency range, the bandwidth will scale proportionately. For example, if the loop bandwidth (LBW) is 1.19 MHz at 1.485 GHz, then at 2.97 GHz the LBW will be 2.38 MHz, and peaking will be less than 0.1 dB. When DRD is not equal to 1, the bandwidth at  $\text{DRD} = 1$  scales by the DRD divide ratio. For example, if the LBW is 2.38 MHz at 2 x HD-SDI with  $\text{DRD} = 1$ , then if  $\text{DRD} = 2$  for HD operation, the LBW will be 1.19 MHz. In general, the default bandwidth will meet SMPTE specifications for all bit rates down to 143 MHz. Internal filter components assure that the peaking will not exceed 0.1 dB for all DRDs up to 16. In the hardwired mode, the LBW will be properly set for the hardwired bit rates. In the serial register mode, the default bandwidth scales automatically with the input bit rate, and the bandwidth can be tuned through registers.

The CDR/RCLK requires an external reference clock to be connected to the **RefClkP/N** pins. The CDR/RCLK contains an internal frequency prescaler that allows a single reference to be used for multiple bit rates and thereby ease the burden of having to route and switch multiple frequency references.

Frequency acquisition is accomplished with two key sections. The first section is a secondary phase/frequency lock loop (P/FLL) that drives the VCO towards the desired frequency. The second section is the loss-of-lock circuitry (LOLCir), that turns on or off the secondary P/FLL. In general LOL has register bits (*Alarm\_LOL*) which are active high, and pins (**xLOL**[3:0]) which are active low, for wired OR use to be wired OR externally. In the general context, they will be referred to as LOL which is active H. With both methods, frequency acquisition takes place when the LOLCir determines an out of lock condition (LOL = H) for each CDR/RCLK, when the VCO frequency exceeds a given range (window). LOLCir enables the secondary P/FLL to drive the VCO close to the desired frequency (the input data bit rate). When the VCO falls within a given frequency range where the CDR/RCLK loop can acquire phase lock, LOLCir turns off the secondary P/FLL and sets LOL = L, allowing the CDR/RCLK to achieve phase lock. During this time, LOLCir continues to monitor the frequency difference and will signal a LOL = H to start the acquisition routine again; if the frequency falls out of range. The LOLCir range is fixed in hardwired mode, and programmable in 2-wire or 4-wire serial interface mode. In general, the frequency threshold (window) for LOL = H-to-L and LOL = L-to-H are different to prevent LOL from toggling when the frequency is near one of the windows. These registers also control the frequency acquisition time. Suggested values are given in this document for general robust operation, and are used as register defaults, however, the programmability of the registers allow for optimization based on a given application (e.g. faster lock times).

### 1.1.15 General CDR/RCLK Features

The CDR/RCLK is reset upon **xRST** = L, *Mastreset* = AAh, or upon power up. A soft reset through *RCLK\_ctrlA* [3] = 1b resets the CDR/RCLK state machine, and presets the CDR/RCLK to an out-of-lock condition, however, the register contents that are related to CDR/RCLK setup are unchanged. It is required to force a soft reset if the bit rate is dynamically changed. The soft reset register bit needs to be cleared for proper operation. In general, a reset during operation will cause bit errors, until the CDR/RCLK achieves phase lock.

By default, the CDR/RCLK is active and powered up for normal operation. By setting *RCLK\_ctrlB* [7:6] = 11b, the CDR/RCLK can be bypassed and powered down, to allow for nonstandard bit rates, or to save power when the CDR/RCLK is not required at lower bit rates. When *RCLK\_ctrlB* [7:6] = 01b, the CDR/RCLK is bypassed so the output data is not retimed but active (VCO locked to the input data). In the last mode with *RCLK\_ctrlB* [7:6] = 10b, the CDR/RCLK is powered down, and all signals along the input and output paths are also powered down, to save power. In this case, the input data does not reach the output.

To prevent the propagation of noise in the case where there is a LOL condition, the CDR/RCLK contains an auto-inhibit feature, which is enabled by default. When LOL is active, the output of the CDR/RCLK is fixed at a logic high state (**DoutP** = H, **DoutN** = L). This feature can be disabled by setting *RCLK\_ctrlA* [3] = 0b, which allows *RCLK\_ctrlA* [5] to either force an inhibit (1b) or to never inhibit (0b).

In some applications, the optimal data sampling point is not in the middle of the data eye. By default, the CDR/RCLK achieves phase lock very near the center of the eye. For optimal performance (jitter tolerance), the actual sampling point can be adjusted with *Phadj\_ctrl* [3:0]. The adjustment range is from -122.5 mUI to +122.5 mUI with 17.5 mUI steps.

### 1.1.16 Multirate CDR Data Rate Selection

For multirate operation, the first step is to determine the desired data rate range. The input data range must be bracketed by  $DF_{\min} = F_{\text{vco, min}}/DRD_{\max}$  to  $DF_{\max} = F_{\text{vco, max}}/DRD_{\min}$ .  $DF_{\max/\min}$  are the maximum/minimum input data rate frequencies,  $DRD_{\max/\min}$  are the maximum/minimum data rate divider settings using *CDR\_ctrlB* [3:0], and  $F_{\text{vco, min}}/F_{\text{vco, max}}$  are the minimum/maximum VCO frequencies, which are 2.0 GHz and 3.2 GHz respectively. The valid data rates are shown in [Table 1-11](#).

Table 1-11. Valid Input Data Ranges

| Parameter                                             | DF <sub>min</sub> | DF <sub>max</sub> | Units |
|-------------------------------------------------------|-------------------|-------------------|-------|
| Data rate divider (DRD = 1): CDR_ctrlB [3:0] = 0000b  | 2.0               | 3.2               | GHz   |
| Data rate divider (DRD = 2): CDR_ctrlB [3:0] = 0001b  | 1.0               | 1.6               | GHz   |
| Data rate divider (DRD = 4): CDR_ctrlB [3:0] = 0010b  | 500               | 800               | MHz   |
| Data rate divider (DRD = 8): CDR_ctrlB [3:0] = 0011b  | 250               | 400               | MHz   |
| Data rate divider (DRD = 12): CDR_ctrlB [3:0] = 0100b | 166.7             | 266.66            | MHz   |
| Data rate divider (DRD = 16): CDR_ctrlB [3:0] = 0101b | 125               | 200               | MHz   |
| Data rate divider (DRD = 24): CDR_ctrlB [3:0] = 0110b | 83.33             | 133.33            | MHz   |
| Data rate divider (DRD = 32): CDR_ctrlB [3:0] = 0111b | 62.5              | 100               | MHz   |
| Data rate divider (DRD = 48): CDR_ctrlB [3:0] = 1000b | 42                | 66.66             | MHz   |

It is important to note the difference between the VCO frequency ( $F_{VCO}$ ), and the data rate frequency (DF).  $F_{VCO}$  is always between 2 GHz to 3.2 GHz, while DF is the divided down  $F_{VCO}$  that matches the input data rate.

### 1.1.17 Frequency Acquisition

Frequency acquisition is enabled by the LOLCir when LOL = H (*Alarm\_LOL* = H or *xLOL* = L). A secondary FLL attempts to lock the VCO to a frequency derived from the external reference. When the frequency is close to the desired frequency, LOLCir sets LOL = L and disables the secondary FLL, thus, the main CDR/RCLK PLL is free to phase lock to the incoming data. Although the main CDR/RCLK PLL can achieve frequency lock, the VCO frequency tuning range typically exceeds the CDR/RCLK PLL inherent acquisition range. This implies that the FLL needs to get the VCO within the CDR/RCLK PLL range. The loss of lock circuitry (LOLCir) is used to determine when the secondary FLL is active. The LOLCir consists of window detectors that constantly compare a scaled VCO frequency, to a frequency related to the external reference. When LOL = H the loop is out of lock, the FLL is activated until the frequency difference is within the narrow reference window (NRW). When LOL = L, the FLL is not engaged until the frequency exceeds the wide reference window (WRW). If a signal is not present, the FLL circuit will drive the VCO frequency to the NRW and turn off. Without data present, the VCO would then drift until the frequency difference exceeds the WRW, and repeat this cycle. To prevent this, by default, the FLL is activated with LOL = H and de-activated with LOL = L.

Figure 1-8. Block Diagram of Frequency Acquisition Circuits

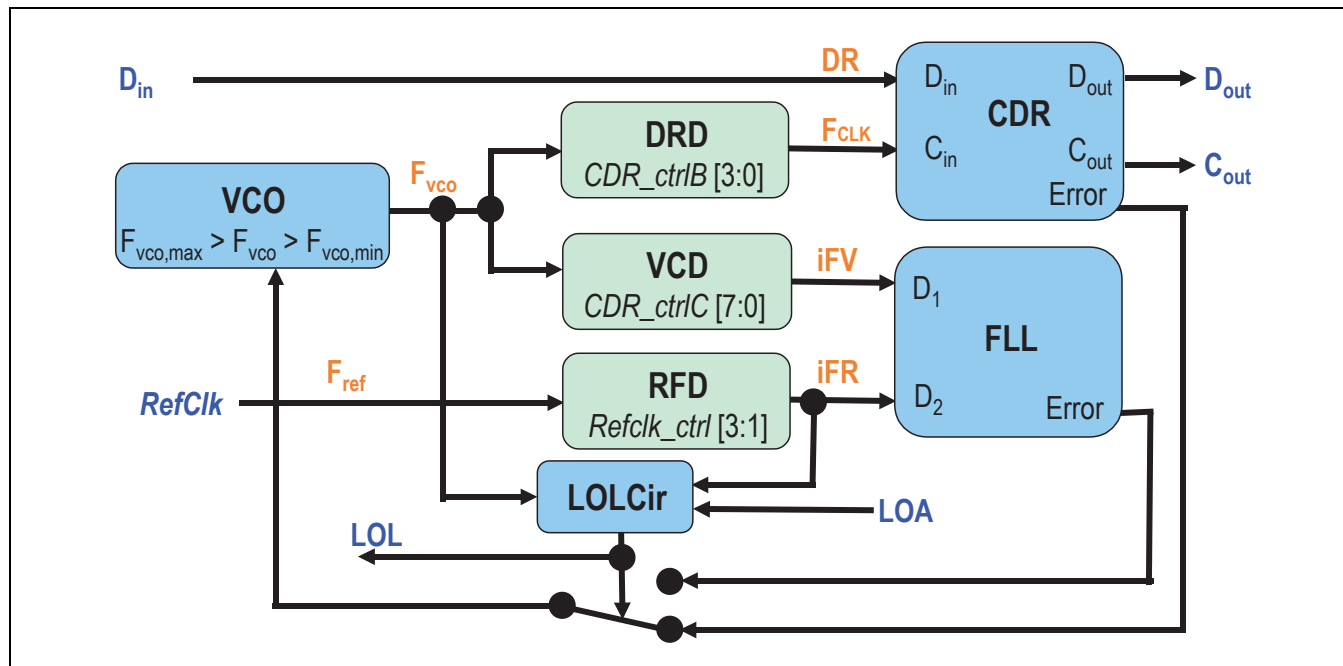


Figure 1-8 shows a block diagram of the frequency acquisition circuits. The secondary FLL compares a scaled version of the internal VCO frequency ( $iFV$ ) with a scaled version of the reference clock frequency ( $iFR$ );  $iFR$  and  $iFV$  are limited to between 10 MHz and 25 MHz. The external reference clock frequency ( $F_{ref}$ ) is applied to the **RefClk** [P/N] terminals. This reference frequency is scaled to the  $iFR$  by the reference frequency divider (RFD) [ $Refclk\_ctrl [3:1]$ ], which allows for an external reference clock in the range of 10 MHz to 800 MHz. The RFD level is a globally set value that applies to all CDR/RCLKs. Table 1-12 gives the divider ratio, along with the minimum and maximum  $F_{ref}$  values.

Table 1-12. Reference Clock Frequency Ranges

| RFD Value                                         | Minimum $F_{ref}$ (MHz) | Maximum $F_{ref}$ (MHz) |
|---------------------------------------------------|-------------------------|-------------------------|
| RFD ( $Refclk\_ctrl [3:1] = 000b$ ): divide by 1  | 10                      | 25                      |
| RFD ( $Refclk\_ctrl [3:1] = 001b$ ): divide by 2  | 20                      | 50                      |
| RFD ( $Refclk\_ctrl [3:1] = 010b$ ): divide by 4  | 40                      | 100                     |
| RFD ( $Refclk\_ctrl [3:1] = 011b$ ): divide by 8  | 80                      | 200                     |
| RFD ( $Refclk\_ctrl [3:1] = 100b$ ): divide by 12 | 120                     | 300                     |
| RFD ( $Refclk\_ctrl [3:1] = 101b$ ): divide by 16 | 160                     | 400                     |
| RFD ( $Refclk\_ctrl [3:1] = 110b$ ): divide by 32 | 320                     | 800                     |

The VCO frequency is scaled to the  $iFV$  by the VCO comparison divider (VCD) [ $RCLK\_ctrlC\_N [7:0]$ ]. Table 1-13 provides DRD, RFD, and VCD values for common applications. For applications that only deal with SONET/SDH data rates, a 19.44 MHz reference clock frequency must be used. For applications where a combination of

SONET/SDH and other data rates are used, a 25 MHz reference clock frequency must be used. If either of these reference clock frequencies is not available, please contact MACOM Technologies Applications Engineering for other options.

**Table 1-13. DRD/RFD/VCD Settings for Different Data Rates and Reference Frequencies (1 of 2)**

| Application  | DR (Mbps) | Fref (MHz) | DRD | RFD | VCD | Notes |
|--------------|-----------|------------|-----|-----|-----|-------|
| 10GE - XAUI  | 3125      | 156.25     | 1   | 8   | 160 | —     |
| 10GE - XAUI  | 3125      | 25         | 1   | 2   | 250 | —     |
| 10GFC - XAUI | 3187.5    | 159.375    | 1   | 8   | 160 | —     |
| 10GFC - XAUI | 3187.5    | 25         | 1   | 2   | 255 | 1     |
| STS-48+FEC   | 2666.06   | 19.44      | 1   | 1   | 137 | 1     |
| STS-48 + FEC | 2666.06   | 25         | 1   | 2   | 213 | 1     |
| STS-48       | 2488.32   | 155.52     | 1   | 8   | 128 | —     |
| STS-48       | 2488.32   | 19.44      | 1   | 1   | 128 | —     |
| STS-48       | 2488.32   | 25         | 1   | 2   | 199 | 1     |
| 2GFC         | 2125      | 106.25     | 1   | 8   | 160 | —     |
| 2GFC         | 2125      | 25         | 1   | 2   | 170 | —     |
| GE           | 1250      | 125        | 2   | 8   | 160 | —     |
| GE           | 1250      | 25         | 2   | 2   | 200 | —     |
| FC           | 1062.5    | 106.25     | 2   | 8   | 160 | —     |
| FC           | 1062.5    | 25         | 2   | 2   | 170 | 1     |
| STS-12       | 622.08    | 19.44      | 4   | 1   | 128 | —     |
| STS-12       | 622.08    | 25         | 4   | 2   | 199 | 1     |
| FC           | 531       | 25         | 4   | 2   | 170 | 1     |
| FC           | 266       | 25         | 12  | 2   | 255 | 1     |
| ESCON        | 200       | 10         | 12  | 1   | 240 | —     |
| ESCON        | 200       | 25         | 12  | 2   | 192 | —     |
| STS-3        | 155.52    | 19.44      | 16  | 1   | 128 | —     |
| STS-3        | 155.52    | 25         | 16  | 2   | 199 | 1     |
| FC           | 133       | 25         | 24  | 2   | 255 | 1     |
| FE           | 125       | 12.5       | 16  | 1   | 160 | —     |
| FE           | 125       | 25         | 24  | 2   | 240 | —     |
| STS-1        | 51.84     | 25         | 48  | 2   | 199 | 1     |

Table 1-13. DRD/RFD/VCD Settings for Different Data Rates and Reference Frequencies (2 of 2)

| Application | DR (Mbps) | Fref (MHz) | DRD | RFD | VCD | Notes |
|-------------|-----------|------------|-----|-----|-----|-------|
| STS-1       | 51.84     | 19.44      | 48  | 1   | 128 | 1     |
| DS3         | 44.736    | 25         | 48  | 2   | 172 | 1     |

**NOTES:**

- Set  $LOL\_ctrl\_N[0] = 1b$ , all other bits at default values.

The FLL drives the iFV to iFR, and it is the primary function of the LOLCir to determine when to turn off the FLL, so the CDR/RCLK can achieve phase lock. The LOLCir uses the frequency difference between iFV and iFR to switch LOL, which turns on and off the secondary FLL. The thresholds where LOL makes a transition are defined as windows. These windows are fixed in the hardwired mode, and programmable in the two-wire interface mode. To prevent LOL from toggling at the thresholds, two windows are used for hysteresis. When  $LOL = L$  and the frequency difference exceeds the larger window (WRW), LOL L-to-H occurs to signal an out of lock case. When  $LOL = H$  (and  $LOA = L$ ), the frequency difference is brought within the narrow reference window (NRW), after which LOL makes a H-to-L transition signaling in-lock. If  $LOA = H$  when  $LOL = L$ , the FLL remains on to keep the VCO locked to the reference, until a signal is present.  $N_{acq}$  is defined with  $LOL\_ctrl[7:5]$ ,  $N_{narrow}$  is defined with  $LOL\_ctrl[4:1]$ , and  $N_{wide}$  is defined with  $LOL\_ctrl[0]$ . The LOLCir averages a large number of transitions before making an LOL decision. This averaging time is referred to as the LOL decision time or  $DT_{LOL}$ .

Table 1-14 shows various window sizes for different applications, including the default value in both the hardwired and two-wire serial interface modes.

Table 1-14. LOL Window Size and Decision Time Examples

| Condition                              | $N_{acq}$ | $N_{narrow}$ | $N_{wide}$ | Narrow Window (ppm) | Wide Window (ppm) | Decision Time ( $\mu s$ ) |
|----------------------------------------|-----------|--------------|------------|---------------------|-------------------|---------------------------|
| Hardwired mode default                 | 101b      | 0100b        | 0b         | $\pm 1955$          | $\pm 2930$        | 420                       |
| Two-wire serial interface mode default | 101b      | 0100b        | 0b         | $\pm 1955$          | $\pm 2930$        | 420                       |
| iFV = iFR                              | 111b      | 0010b        | 1b         | $\pm 245$           | $\pm 975$         | 1685                      |
| Fast lock                              | 010b      | 0001b        | 0b         | $\pm 5860$          | $\pm 7800$        | 56                        |

**NOTES:**

- Decision time is calculated with iFR = 19.44 MHz; will scale proportionally with iFR range from 10 to 25 MHz.
- Above are examples showing ability to tailor windows for data rates, reference frequencies, and acquisition times.

### 1.1.18 CDR/Reclocker Data Rate Programming (HD/SD-SDI data rates only)

If the automatic rate detection (ARD) algorithm developed by MACOM is used, it is not necessary for the user to manually program the registers of the reclockers to configure the reclockers for operation at a specific data rate. In applications where the ARD is not implemented and the device is used with software control, there are a few parameters that must be configured for the reclocker to correctly lock to the input data. The parameters that need to be programmed are the data rate divider (DRD) and the VCO frequency divider (VCD). The DRD is programmed

using bits [3:0] of register address 41h. The VCD is programmed using bits [7:0] of register address 42h. The following table shows the recommended values of DRD and VCD for standard video data rates.

**Table 1-15. Recommended Values of DRD and VCD for Standard Video Data Rates**

| Data Rate (Mbps) | DRD Value | VCD Value | Fref (MHz) |
|------------------|-----------|-----------|------------|
| 143              | 05h       | BFh       | 12         |
| 177              | 04h       | B1h       | 12         |
| 270              | 03h       | B4h       | 12         |
| 360              | 03h       | F0h       | 12         |
| 540              | 02h       | B4h       | 12         |
| 1483.5/1485      | 01h       | F7h       | 12         |
| 2967/2970        | 00h       | F7h       | 12         |

### 1.1.19 Ambient Temperature Range Limitations

Table 1-16 summarizes the supported ambient temperature range as a function of data rate, and indicates when it is required to center the VCO.

**Table 1-16. Supported Ambient Temperature Range by Data Rate**

| F <sub>VCO</sub> (GHz) | DR (Gbps)         | T <sub>a</sub> (°C) | VCO Centering Requirement |
|------------------------|-------------------|---------------------|---------------------------|
| 2.0–2.666              | 2.0/DRD–2.666/DRD | –40–85              | N                         |
| 2.7–2.97               | 2.7/DRD–2.97/DRD  | 0–70                | N                         |
| 2.7–2.97               | 2.7/DRD–2.97/DRD  | –40–85              | Y                         |
| 3.0–3.2                | 3.0/DRD–3.2/DRD   | 0–70                | Y                         |

F<sub>VCO</sub> is the VCO frequency, which always lies in the range 2.0–3.2 GHz. DR is the data rate of the input signal, and DRD is the data rate divider (1, 2, 4, 8, 12, 16, 24, 32, 48) set with *rc1k\_ctrlB\_N*[3:0]. T<sub>a</sub> is the ambient temperature supported, which decreases for F<sub>VCO</sub> > 2.666 GHz. As an example, if the data rate is 800 Mbps DRD should be set to 4; to lock to this signal the VCO needs to operate at 3.2 GHz. Under these conditions the ambient temperature range supported is 0°C–70°C, and it is necessary to center the VCO in each of the four lanes.

The VCO tuning range is roughly the same bandwidth as the variation in VCO center frequency between the extremes of the operating temperature range. This issue can be resolved by centering the VCO frequency during the in-circuit testing (ICT) phase prior to shipment of the customer systems.

**NOTE:** The CDR/RCLK must be powered up and configured at 25°C–40°C ambient temperature during ICT.

1. Power up the device and configure the registers via the serial interface with the appropriate settings for the application of interest.
2. Read and store the VCO trim code from register MBh[4:0].
3. Every time the device is powered up, this trim code must be forced by setting M0h[0] = 0b then writing the code to MAh[4:0]. This can be done during the same write cycle as when the other registers are configured.

It should be noted that it is not possible to center the VCO in the hardwired mode, it is necessary to program the CDR/RCLK using the serial interface.

### 1.1.20 Loss of Activity

By default, the LOA detector is enabled and can be disabled by setting *CDR\_ctrlA\_N* [1] = 0b, where N is the channel number. Loss of activity measures the transition density of data to determine if the data is valid. With PRBS data, the transition density is typically 50%, averaged over long periods. During small time intervals, data transition density variations are due to data content, packet headers, stress patterns, etc. In some applications, when data is not present, noise produces rail-to-rail transitions that cause problems with level based detectors. These applications include cascaded reclockers, high-gain crosspoints, and other devices. The data transition density based LOA detector can separate data from random noise, determine false lock at the wrong integer and non-integer data rate, signal stuck high/low conditions, and determine false lock to retimed noise. Unlike level based detectors, it cannot determine false lock with low amplitude data.

### 1.1.21 Built-In Self Test (BIST) Overview

The M21262 contains a BIST test pattern generator as well as a test pattern receiver. Both the BIST transmitter (BIST Tx), and BIST receiver (BIST Rx) are designed to operate with fixed patterns. For PRBS evaluation, the PRBS  $2^7-1$ ,  $2^{15}-1$ ,  $2^{23}-1$ , and  $2^{31}-1$  test patterns are provided. For 8b/10b testing, the fibre channel CRPAT and CJTPAT standard patterns are supported. In addition, an 8b/10b countdown pattern is also provided; this is the 8b/10b representation of a binary count from 255 to 0, while maintaining 8b/10b running disparity requirements. User programmable 16 bit (PRBS) and 20 bit (8b/10b) patterns are also provided; they are typically used to generate short patterns for debug, such as 1100b, as well as 8b/10b idle or control characters. The BIST is designed to reduce system development time, as well as product test costs, and can be used by both the equipment provider as well as the equipment end user.

When enabled, the BIST Rx allows one input from the M21262 to enter the BIST receiver. The desired channel to monitor is selected through a control register. The BIST Rx uses the recovered clock and data from the selected CDR/RCLK to drive the pattern checker. Every time a bit error is received, the error register is incremented. The maximum number of errors is FFh, and all subsequent errors will not be counted. At any time, the error register can be cleared. By keeping track of the time between a clear and a read, a rough BER number can be obtained.

When enabled, the BIST Tx can output a test pattern to the M21262 output (the BIST Tx and Rx can be used at the same time). The BIST Tx contains an internal clock multiplier (PLL), that can take its input from either the external reference frequency, or from the same CDR/RCLK that is driving the BIST Rx (only in full-rate mode, DRD = 1).

### 1.1.22 BIST Test Patterns

The test pattern is selected with *BISTtx\_ctrl* [5:2] for the transmitter, and *BISTrx\_ctrl* [5:2] for the receiver.

The PRBS patterns generated by the unit are ITU-T 0.151 compliant, and summarized in the table below.

Table 1-17. BIST PRBS Patterns

| <i>BISTtx_ctrl</i> [5:2] / <i>BISTrx_ctrl</i> [5:2] | Pattern         | Polynomial        |
|-----------------------------------------------------|-----------------|-------------------|
| 0000b                                               | PRBS $2^7-1$    | $2^7+2^6+1$       |
| 0001b                                               | PRBS $2^{15}-1$ | $2^{15}+2^{14}+1$ |
| 0010b                                               | PRBS $2^{23}-1$ | $2^{23}+2^{18}+1$ |
| 0011b                                               | PRBS $2^{31}-1$ | $2^{31}+2^{28}+1$ |

For 8b/10b data, three patterns are available. The CJTPAT and CRPAT comply with the Fibre Channel T11.2/Project 1230/Rev10 specifications.

Table 1-18. BIST 8b/10b Patterns

| <i>BISTtx_ctrl</i> [5:2] / <i>BISTrx_ctrl</i> [5:2] | Pattern   |
|-----------------------------------------------------|-----------|
| 0100b                                               | CJTPAT    |
| 0101b                                               | CRPAT     |
| 0110b                                               | Countdown |

Two user programmable patterns that are 16 bits long (*BISTtx\_ctrl* [5:2] = *BISTrx\_ctrl* [5:2] = 0111b) and 20 bits long (*BISTtx\_ctrl* [5:2] = *BISTrx\_ctrl* [5:2] = 1000b) are determined with *BIST\_pattern0*, *BIST\_pattern1*, *BIST\_pattern2*. Note that the contents of these registers is used by both the BIST Tx and the BIST Rx, if they are setup in this mode.

### 1.1.23 BIST Receiver (BIST Rx) Operation

The BIST Rx is enabled and powered up by setting *BISTrx\_ctrl* [1] = 1b (off by default), resetting the BIST Rx block with *BISTrx\_ctrl* [0] = 1b (default), and selecting a pattern with *BISTrx\_ctrl* [5:2]. The signal to the BIST Rx is routed from the input of the device, and the BIST Rx can only check one channel at a time. The desired channel to monitor is selected with *BISTrx\_chsel* [2:0]. The BIST Rx uses the recovered clock from the CDR/RCLK to drive the BIST state machine, thus the CDR/RCLK must be enabled and locked to data for proper operation. When the data is valid, *BISTrx\_ctrl* [6] = 1b is used to clear the error register, and all subsequent errors can be read back through *BISTrx\_error*. The BIST Rx automatically synchronizes the input data with the pattern.

### 1.1.24 BIST Transmitter (BIST Tx) Operation

The BIST Tx is enabled and powered up by setting *BISTtx\_ctrl* [1] = 1b (off by default), resetting the BIST Tx block with *BISTtx\_ctrl* [0] = 1b (default), and selecting a pattern with *BISTtx\_ctrl* [5:2]. The high-speed clock of the BIST Tx is generated from its own frequency multiplier PLL, that uses a selectable frequency reference determined by *BISTtx\_ctrl* [6]. With *BISTtx\_ctrl* [6] = 0b (default), the external reference clock is used and typically gives the lowest jitter output. With *BISTtx\_ctrl* [6] = 1b the reference clock is derived from the same CDR/RCLK used to drive the BIST Rx (this feature only works with DRD = 1 for that CDR/RCLK). In this mode, the BIST Tx output is synchronous with the CDR/RCLK used in the BIST Rx, however, it contains the low-frequency jitter from the input data. In either case, the BIST Tx PLL needs to be configured for the proper data rate. When the PLL is properly

configured and locked to the reference, the LOL flag should be low (*BISTtx\_alarm* [7]). A bit error can be intentionally inserted into the BIST Tx output, by providing a 0b, 1b, 0b sequence to *BISTtx\_ctrl* [7].

The BIST Tx PLL setup is similar to the CDR/RCLK setup, thus, the description of similar registers for the CDR/RCLK also applies and will not be repeated here. The desired output data rate is set with the DRD register (*BISTtx\_PLL\_ctrlB* [3:0]) and with the VCD register (*BISTtx\_PLL\_ctrlC* [7:0]). The input reference frequency iFR is the same as for the main CDR/RCLKs, since the same external reference and reference dividers are used. In the internal CDR/RCLK case, iFR is  $F_{VCO, RCLK}/128$ , where  $F_{VCO, RCLK}$  is the VCO frequency of the CDR/RCLK selected by *BISTrx\_chsel* [2:0]. Unlike the CDR/RCLK, the Tx PLL always makes iFR equal to iFV, and *BISTtx\_alarm* [7] is used to determine if the Tx PLL is in lock. Like the CDR/RCLKs, if the output data rate of the BIST Tx needs to be changed, the BIST Tx requires a soft reset.

### 1.1.25 Junction Temperature Monitor

An internal junction temperature monitor with a range of -40°C to 130°C is integrated into the M21260. On the low end, the temperature monitor (Tmon) is set to measure -40°C to 10°C in six 10°C steps, and on the high end, 80°C to 130°C in six 10°C steps. The typical temperature resolution is 3°C. The temperature monitor is enabled with *Temp\_mon* [1] = 1b. When enabled, the temperature measurement cycle is achieved by providing a rising edge for *Temp\_mon* [0]. Afterwards, the correct temperature can be read from *Temp\_value* [3:0]. Table 1-19 shows the mapping of the temperature to *Temp\_value* [3:0]. Enabling and strobing the temperature in the same write cycle will not yield reliable results.

**Table 1-19. Junction Temperature Monitor**

| Junction Temperature                             | <i>Temp_value</i> [3:0] | Condition    |
|--------------------------------------------------|-------------------------|--------------|
| $T_c \geq 130^\circ\text{C}$                     | 1100b                   | High-alarm   |
| $130^\circ\text{C} > T_c \geq 120^\circ\text{C}$ | 1011b                   | High-alarm   |
| $120^\circ\text{C} > T_c \geq 110^\circ\text{C}$ | 1010b                   | High-warning |
| $110^\circ\text{C} > T_c \geq 100^\circ\text{C}$ | 1001b                   | Normal       |
| $100^\circ\text{C} > T_c \geq 90^\circ\text{C}$  | 1000b                   | Normal       |
| $90^\circ\text{C} > T_c \geq 80^\circ\text{C}$   | 0111b                   | Normal       |
| $80^\circ\text{C} > T_c \geq 70^\circ\text{C}$   | 0110b                   | Normal       |
| $70^\circ\text{C} > T_c \geq 60^\circ\text{C}$   | 0101b                   | Normal       |
| $60^\circ\text{C} > T_c \geq 50^\circ\text{C}$   | 0100b                   | Normal       |
| $50^\circ\text{C} > T_c \geq 40^\circ\text{C}$   | 0011b                   | Normal       |
| $40^\circ\text{C} > T_c \geq 30^\circ\text{C}$   | 0010b                   | Warning      |
| $30^\circ\text{C} > T_c \geq 20^\circ\text{C}$   | 0001b                   | Low-alarm    |
| $20^\circ\text{C} > T_c \geq 10^\circ\text{C}$   | 0000b                   | Low-alarm    |

### 1.1.26 IC Identification / Revision Code

The IC identification can be read back from *Chipcode*, and the revision of the device can be read back from *Revcode*.

## 1.2 Pin Definitions

**Table 1-20. Power Pins**

| Pin Number                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | Pin Name         | Function                     | Type  |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------|------------------------------|-------|
| Exposed pad                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    | <b>Vss</b>       | IC ground                    | Power |
| 1, 31, 54, 63, 64                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | <b>AVdd_I/O</b>  | Analog I/O positive supply   | Power |
| 21, 27, 28, 34, 57, 60, 67, 70                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | <b>AVdd_Core</b> | Analog core positive supply  | Power |
| 10                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             | <b>DVdd_I/O</b>  | Digital I/O positive supply  | Power |
| 11, 22, 33                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | <b>DVdd_Core</b> | Digital core positive supply | Power |
| <b>NOTES:</b> <ol style="list-style-type: none"> <li>If internal regulator is enabled, connect all of the <b>AVdd_Core</b> and/or <b>DVdd_Core</b> pins together to a common floating plane and bypass to <b>Vss</b>.</li> <li>If internal regulator is NOT enabled, it is recommended that all <b>AVdd_Core</b> pins be tied to a plane at 1.2V, that is bypassed to ground. <b>DVdd_Core</b> can be tied to this plane or separately decoupled.</li> <li>IC ground (<b>Vss</b>) is established by contact with exposed pad on underside of package; there are no <b>Vss</b> pins.</li> </ol> |                  |                              |       |

**Table 1-21. High-Speed Signal Pins**

| Pin Number | Pin Name       | Function                                 | Termination                    | Type                                |
|------------|----------------|------------------------------------------|--------------------------------|-------------------------------------|
| 19         | <b>Din0P</b>   | Serial positive data input for channel 0 | 50Ω pull up to <b>VddT0/1</b>  | PCML referenced to <b>Avdd_Core</b> |
| 20         | <b>Din0N</b>   | Serial negative data input for channel 0 | 50Ω pull up to <b>VddT0/1</b>  | PCML referenced to <b>Avdd_Core</b> |
| 25         | <b>Din1P</b>   | Serial positive data input for channel 1 | 50Ω pull up to <b>VddT0/1</b>  | PCML referenced to <b>Avdd_Core</b> |
| 26         | <b>Din1N</b>   | Serial negative data input for channel 1 | 50Ω pull up to <b>VddT0/1</b>  | PCML referenced to <b>Avdd_Core</b> |
| 29         | <b>Din2P</b>   | Serial positive data input for channel 2 | 50Ω pull up to <b>VddT2/3</b>  | PCML referenced to <b>Avdd_Core</b> |
| 30         | <b>Din2N</b>   | Serial negative data input for channel 2 | 50Ω pull up to <b>VddT2/3</b>  | PCML referenced to <b>Avdd_Core</b> |
| 35         | <b>Din3P</b>   | Serial positive data input for channel 3 | 50Ω pull up to <b>VddT2/3</b>  | PCML referenced to <b>Avdd_Core</b> |
| 36         | <b>Din3N</b>   | Serial negative data input for channel 3 | 50Ω pull up to <b>VddT2/3</b>  | PCML referenced to <b>Avdd_Core</b> |
| 23         | <b>VddT0/1</b> | Termination pin for <b>Din</b> [1:0]     | Terminate to <b>AVdd_Core</b>  | Termination                         |
| 32         | <b>VddT2/3</b> | Termination pin for <b>Din</b> [3:2]     | Terminate to <b>AVdd_Core</b>  | Termination                         |
| 72         | <b>DoutP</b>   | Serial positive data output              | 50Ω pull up to <b>AVdd_I/O</b> | O—CML/LVDS                          |
| 71         | <b>DoutN</b>   | Serial negative data output              | 50Ω pull up to <b>AVdd_I/O</b> | O—CML/LVDS                          |

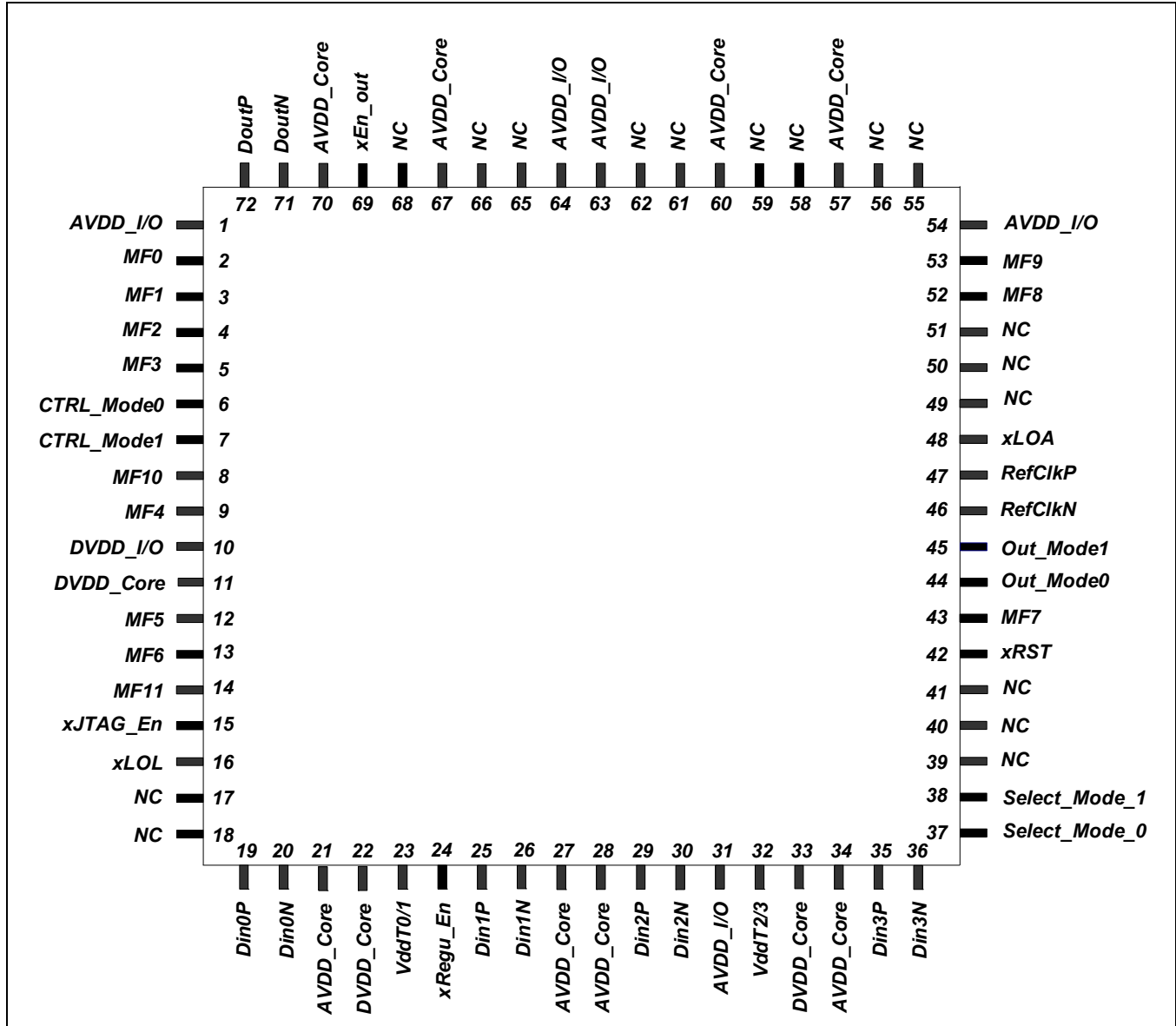
**Table 1-22. Control, Interface, and Alarm Pins (1 of 2)**

| Pin Number | Pin Name   | Function                                                   | Default          | Type   |
|------------|------------|------------------------------------------------------------|------------------|--------|
| 2          | <b>MF0</b> | Multifunction pin for hardwired mode, and serial interface | Internal pull up | I—CMOS |
| 3          | <b>MF1</b> | Multifunction pin for hardwired mode, and serial interface | Internal pull up | I—CMOS |
| 4          | <b>MF2</b> | Multifunction pin for hardwired mode, and serial interface | Internal pull up | I—CMOS |

Table 1-22. Control, Interface, and Alarm Pins (2 of 2)

| Pin Number | Pin Name             | Function                                                         | Default                          | Type         |
|------------|----------------------|------------------------------------------------------------------|----------------------------------|--------------|
| 5          | <b>MF3</b>           | Multifunction pin for hardwired mode, and serial interface       | Internal pull up                 | I—CMOS       |
| 9          | <b>MF4</b>           | Multifunction pin for hardwired mode, and serial interface       | Internal pull up                 | I—CMOS       |
| 12         | <b>MF5</b>           | Multifunction pin for hardwired mode, and serial interface       | Internal pull up                 | I—CMOS       |
| 13         | <b>MF6</b>           | Multifunction pin for hardwired mode, and serial interface       | Internal pull up                 | I—CMOS       |
| 43         | <b>MF7</b>           | Multifunction pin for hardwired mode                             | Internal pull up                 | I—CMOS       |
| 52         | <b>MF8</b>           | Multifunction pin for hardwired mode, and JTAG                   | Internal pull up                 | I—CMOS       |
| 53         | <b>MF9</b>           | Multifunction pin for hardwired mode, and JTAG                   | Internal pull up                 | I—CMOS       |
| 8          | <b>MF10</b>          | Multifunction pin for hardwired mode, serial interface, and JTAG | Internal pull up                 | I—CMOS       |
| 14         | <b>MF11</b>          | Multifunction pin for hardwired mode, serial interface, and JTAG | Internal pull up                 | I—CMOS       |
| 6          | <b>CTRL_Mode0</b>    | Hardwired or serial interface mode control pin                   | Internal pull up                 | I—CMOS       |
| 7          | <b>CTRL_Mode1</b>    | Hardwired or serial interface mode control pin                   | Internal pull up                 | I—CMOS       |
| 44         | <b>Out_Mode0</b>     | Output data interface control pin                                | Internal pull down               | I—CMOS       |
| 45         | <b>Out_Mode1</b>     | Output data interface control pin                                | Internal pull down               | I—CMOS       |
| 42         | <b>xRST</b>          | Reset pin (L = reset)                                            | Internal pull up                 | I—CMOS       |
| 15         | <b>xJTAG_En</b>      | JTAG testing control pin (L = enable)                            | Internal pull up                 | I—CMOS       |
| 24         | <b>xRegu_En</b>      | Internal voltage regulator control pin (L = enable)              | Internal pull down               | I—CMOS       |
| 47         | <b>RefClkP</b>       | Reference clock positive input                                   | Internal pull down               | I—AC coupled |
| 46         | <b>RefClkN</b>       | Reference clock negative input                                   | Internal pull down               | I—AC coupled |
| 37         | <b>Select_Mode_0</b> | Selector configuration pin                                       | Internal pull down               | I—CMOS       |
| 38         | <b>Select_Mode_1</b> | Selector configuration pin                                       | Internal pull down               | I—CMOS       |
| 69         | <b>xEn_Port0</b>     | Control pin to enable/disable output for (L = enable)            | Internal pull up                 | I—CMOS       |
| 16         | <b>xLOL</b>          | CDR/RCLK loss of lock alarm                                      | No internal pull up or pull down | O—Open Drain |
| 48         | <b>xLOA</b>          | CDR/RCLK loss of activity alarm                                  | No internal pull up or pull down | O—Open Drain |

Figure 1-9. M21262 Pinout Diagram (Top View)



## 2.0 Product Specifications

### 2.1 Absolute Maximum Ratings

These are the absolute maximum ratings at or beyond which the device can be expected to fail or be damaged. Reliable operation at these extremes for any length of time is not implied.

**Table 2-1. Absolute Maximum Ratings**

| Symbol          | Parameter                          | Notes | Minimum        | Typical     | Maximum               | Units |
|-----------------|------------------------------------|-------|----------------|-------------|-----------------------|-------|
| DVdd_I/O        | Digital I/O power                  | —     | 0              | 1.8/2.5/3.3 | 3.6                   | V     |
| AVdd_I/O        | Analog I/O power                   | —     | 0              | 1.8/2.5/3.3 | 3.6                   | V     |
| AVdd_Core       | Analog core power                  | 2     | 0              | 1.2         | 1.5                   | V     |
| DVdd_Core       | Digital core power                 | 2     | 0              | 1.2         | 1.5                   | V     |
| —               | High-speed signal pins             | 1, 4  | $V_{SS} - 0.5$ | —           | $AV_{DD} - I/O + 0.5$ | —     |
| —               | Control, interface, and alarm pins | 1, 5  | $V_{SS} - 0.5$ | —           | $AV_{DD} - I/O + 0.5$ | —     |
| T <sub>st</sub> | Storage temperature                | —     | -65            | —           | +150                  | °C    |
| ESD             | Human body model (low-speed)       | —     | 2000           | —           | —                     | V     |
| ESD             | Human body model (high-speed)      | —     | 350            | —           | —                     | V     |
| ESD             | Charged device model               | —     | 100            | —           | —                     | V     |
| —               | Maximum DC input current           | 1, 3  | —              | —           | 25                    | mA    |

**NOTES:**

1. No damage under these conditions.
2. Apply voltage to core pin if internal regulator is disabled. If enabled, pins should be floating with bypass to V<sub>SS</sub>.
3. Computed as the current through 50Ω from the voltage difference between the input voltage common mode and V<sub>DDT</sub>.
4. High-speed signal pins are shown in [Table 1-17](#).
5. Control, interface, and alarm pins are shown in [Table 1-18](#).

## 2.2 Recommended Operating Conditions

**Table 2-2. Recommended Operating Conditions**

| Symbol           | Parameter                              | Notes | Minimum | Typical     | Maximum | Units |
|------------------|----------------------------------------|-------|---------|-------------|---------|-------|
| <i>DVdd_I/O</i>  | Digital I/O power                      | 2     | —       | 1.8/2.5/3.3 | —       | V     |
| <i>AVdd_I/O</i>  | Analog I/O power                       | 2     | —       | 1.8/2.5/3.3 | —       | V     |
| <i>AVdd_Core</i> | Analog core power                      | 1, 2  | —       | 1.2         | —       | V     |
| <i>DVdd_Core</i> | Digital core power                     | 1, 2  | —       | 1.2         | —       | V     |
| $T_a$            | Ambient temperature                    | —     | -40     | —           | 85      | °C    |
| $\theta_{ja}$    | Junction to ambient thermal resistance | 3     | —       | 24          | —       | °C/W  |

**NOTES:**

1. Needed only if *AVdd\_Core* or *DVdd\_Core* are provided from external source (internal regulator disabled *xRegu\_En* = H).
2. Typical value  $\pm 5\%$  is acceptable.
3. With forced convection of 1 m/s and 2.5 m/s,  $\theta_{ja}$  is decreased to 18 °C/W and 16 °C/W respectively.

## 2.3 Power Dissipation

**Table 2-3. DC Power Electrical Specifications (1 of 2)**

| Symbol               | Parameter                                                                           | Notes | Minimum | Typical | Maximum | Units |
|----------------------|-------------------------------------------------------------------------------------|-------|---------|---------|---------|-------|
| I <sub>dd</sub>      | Case 1: current consumption for output swing = 550 mV CML, internal regulator = on  | 1     | —       | 310     | 365     | mA    |
| P <sub>diss</sub>    | Power dissipation at 1.8V                                                           | —     | —       | 560     | 660     | mW    |
| P <sub>diss</sub>    | Power dissipation at 3.3V                                                           | 2     | —       | 1.02    | 1.2     | W     |
| I <sub>dd</sub>      | Case 2: current consumption for output swing = 900 mV CML, internal regulator = on  | 1     | —       | 340     | 400     | mA    |
| P <sub>diss</sub>    | Power dissipation at 1.8V                                                           | —     | —       | 610     | 720     | mW    |
| P <sub>diss</sub>    | Power dissipation at 3.3V                                                           | 2     | —       | 1.12    | 1.32    | W     |
| —                    | Case 3: output swing = 550 mV CML, internal regulator = off                         | 1     | —       | —       | —       | —     |
| I <sub>dd_core</sub> | Core current consumption                                                            | —     | —       | 260     | 300     | mA    |
| I <sub>dd_io</sub>   | Input/Output buffers current consumption                                            | —     | —       | 50      | 70      | mA    |
| P <sub>diss</sub>    | Power dissipation at 1.2V core, 1.8V I/O                                            | —     | —       | 400     | 490     | mW    |
| P <sub>diss</sub>    | Power dissipation at 1.2V core, 3.3V I/O                                            | —     | —       | 480     | 590     | mW    |
| I <sub>dd</sub>      | Case 4: current consumption for output swing = 450 mV LVDS, internal regulator = on | 1     | —       | 320     | 380     | mA    |
| P <sub>diss</sub>    | Power dissipation at 1.8V                                                           | —     | —       | 580     | 680     | mW    |
| P <sub>diss</sub>    | Power dissipation at 3.3V                                                           | 2     | —       | 1.06    | 1.25    | W     |

Table 2-3. DC Power Electrical Specifications (2 of 2)

| Symbol            | Parameter                                                                          | Notes | Minimum | Typical | Maximum | Units |
|-------------------|------------------------------------------------------------------------------------|-------|---------|---------|---------|-------|
| I <sub>dd</sub>   | Case 5: current consumption for output swing = 1.5V PCML+, internal regulator = on | 1     | —       | 410     | 470     | mA    |
| P <sub>diss</sub> | Power dissipation at 1.8V                                                          | —     | —       | 740     | 850     | mW    |
| P <sub>diss</sub> | Power dissipation at 3.3V                                                          | 2     | —       | 1.35    | 1.55    | W     |

**NOTES:**

- Specified at recommended operating conditions—see Table 2-2.
- Thermal design such as thermal pad vias on PCB must be considered for this case.

## 2.4 Input/Output Specifications

Table 2-4. Serial Interface (2-wire and 4-wire) CMOS I/O Electrical Specifications

| Symbol             | Parameter                                                           | Notes | Minimum                     | Typical              | Maximum                     | Units |
|--------------------|---------------------------------------------------------------------|-------|-----------------------------|----------------------|-----------------------------|-------|
| V <sub>OH</sub>    | Output logic high I <sub>OH</sub> = -3 mA                           | 2     | 0.8 x DV <sub>dd_I/O</sub>  | DV <sub>dd_I/O</sub> | —                           | V     |
| V <sub>OL</sub>    | Output logic low I <sub>OL</sub> = 24 mA                            | 2     | —                           | 0.0                  | 0.2 x DV <sub>dd_I/O</sub>  | V     |
| I <sub>OH</sub>    | Output current (logic high)                                         | —     | -10                         | —                    | 0                           | mA    |
| I <sub>OL</sub>    | Output current (logic low)                                          | —     | 0                           | —                    | 10                          | mA    |
| V <sub>IH</sub>    | Input logic high                                                    | —     | 0.75 x DV <sub>dd_I/O</sub> | —                    | DV <sub>dd_I/O</sub> + 0.3  | V     |
| V <sub>IL</sub>    | Input logic low                                                     | —     | 0                           | —                    | 0.25 x DV <sub>dd_I/O</sub> | V     |
| I <sub>IH</sub>    | Input current (logic high)                                          | —     | -100                        | —                    | 100                         | μA    |
| I <sub>IL</sub>    | Input current (logic low)                                           | —     | -100                        | —                    | 100                         | μA    |
| t <sub>r</sub>     | Output rise time (20–80%)                                           | —     | —                           | —                    | 250                         | ns    |
| t <sub>f</sub>     | Output fall time (20–80%)                                           | —     | —                           | —                    | 250                         | ns    |
| C <sub>2wire</sub> | Input capacitance of MF10 and MF11 in 2-wire serial interface mode. | 3     | —                           | —                    | 10                          | pF    |

**NOTES:**

- Entire table specified at recommended operating conditions—see Table 2-2.
- DV<sub>dd\_I/O</sub> can be chosen independently from AV<sub>dd\_I/O</sub>.
- 2-wire serial output mode can drive 500 pF.

Table 2-5. Input Electrical Specifications

| Symbol           | Parameter                             | Notes | Minimum | Typical | Maximum         | Units |
|------------------|---------------------------------------|-------|---------|---------|-----------------|-------|
| DR <sub>IN</sub> | Input signal data rate                | —     | 42      | —       | 3200            | Mbps  |
| V <sub>ID</sub>  | Input differential voltage (P–P)      | 2, 3  | 100     | —       | 2000            | mV    |
| V <sub>ICM</sub> | Input common-mode voltage             | —     | 700     | —       | 1200            | mV    |
| V <sub>IH</sub>  | Maximum input high voltage            | —     | —       | —       | AVdd_Core + 400 | mV    |
| V <sub>IL</sub>  | Minimum input low voltage             | —     | 400     | —       | —               | mV    |
| R <sub>IN</sub>  | Input termination to VddT             | 4     | 45      | 50      | 65              | Ω     |
| S <sub>11</sub>  | Input return loss (40 MHz to 2.5 GHz) | —     | —       | -15.0   | —               | dB    |

**NOTES:**

- Entire table specified at recommended operating conditions—see Table 2-2.
- Example 1200 mV<sub>pp</sub> differential = 600 mV<sub>pp</sub> for each single-ended terminal.
- Minimum input level defined as error free operation at 10<sup>-12</sup> BER.
- See Figure 2-1 for input termination circuit.

Figure 2-1. Data Input Internal Circuitry

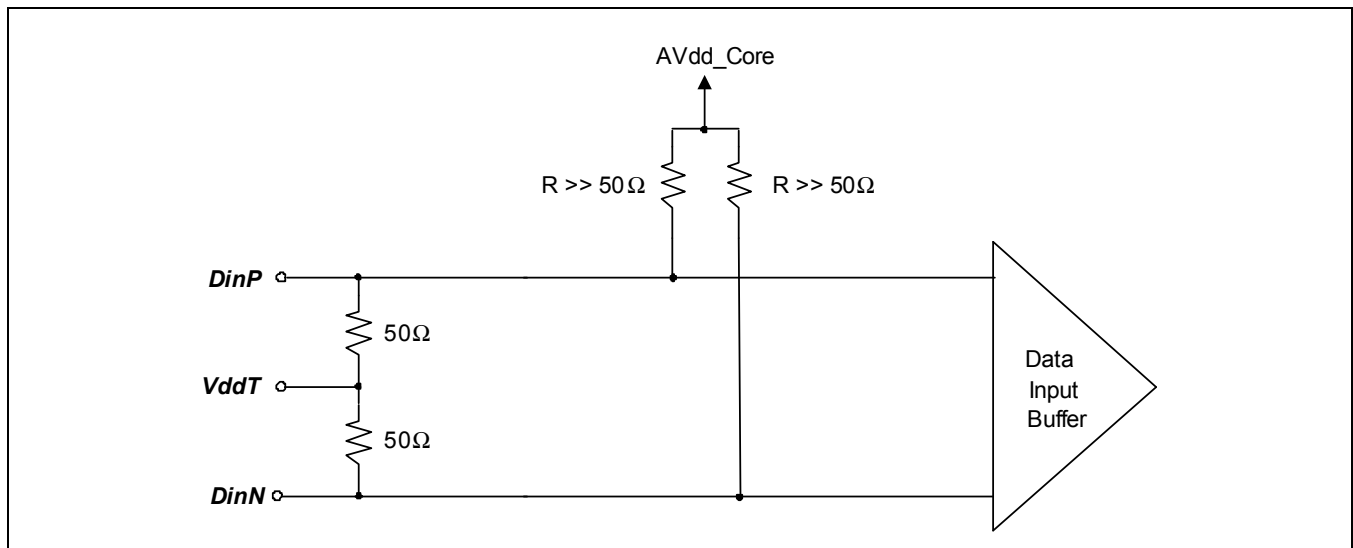


Table 2-6. PCML (Positive Current Mode Logic) Output Electrical Specifications

| Symbol                         | Parameter                                      | Notes | Minimum         | Typical | Maximum        | Units |
|--------------------------------|------------------------------------------------|-------|-----------------|---------|----------------|-------|
| DR <sub>OUT</sub>              | Output signal data rate (Reclockers enabled)   | —     | 42              | —       | 3200           | Mbps  |
| t <sub>r</sub> /t <sub>f</sub> | Rise/Fall time (20–80%) for all levels         | —     | —               | 75      | 130            | ps    |
| V <sub>OH</sub>                | Low swing: output logic high (single-ended)    | —     | AVdd_I/O - 25   | —       | AVdd_I/O       | mV    |
| V <sub>OL</sub>                | Low swing: output logic low (single-ended)     | —     | AVdd_I/O - 370  | —       | AVdd_I/O - 250 | mV    |
| V <sub>OD</sub>                | Low swing: differential swing                  | 2     | 400             | 550     | 750            | mV    |
| V <sub>OH</sub>                | Medium swing: output logic high (single-ended) | —     | AVdd_I/O - 80   | —       | AVdd_I/O       | mV    |
| V <sub>OL</sub>                | Medium swing: output logic low (single-ended)  | —     | AVdd_I/O - 600  | —       | AVdd_I/O - 420 | mV    |
| V <sub>OD</sub>                | Medium swing: differential swing               | 2     | 700             | 900     | 1150           | mV    |
| V <sub>OH</sub>                | High swing: output logic high (single-ended)   | —     | AVdd_I/O - 95   | —       | AVdd_I/O       | mV    |
| V <sub>OL</sub>                | High swing: output logic low (single-ended)    | —     | AVdd_I/O - 770  | —       | AVdd_I/O - 535 | mV    |
| V <sub>OD</sub>                | High swing: differential swing                 | 2     | 900             | 1200    | 1500           | mV    |
| V <sub>OH</sub>                | PCML+ swing: output logic high (single-ended)  | —     | AVdd_I/O - 115  | —       | AVdd_I/O       | mV    |
| V <sub>OL</sub>                | PCML+ swing: output logic low (single-ended)   | —     | AVdd_I/O - 1000 | —       | AVdd_I/O - 680 | mV    |
| V <sub>OD</sub>                | PCML+ swing: differential swing                | 2     | 1150            | 1500    | 1900           | mV    |
| R <sub>OUT</sub>               | Output termination to AVdd_Core                | —     | 45              | 50      | 65             | Ω     |
| S <sub>22</sub>                | Output return loss (40 MHz to 2.5 GHz)         | —     | —               | -15.0   | —              | dB    |

**NOTES:**

- Specified at recommended operating conditions—see Table 2-2.
- Example 1200 mV<sub>P-P</sub> differential = 600 mV<sub>P-P</sub> for each single-ended terminal.
- All output swings defined with pre-emphasis off.

Table 2-7. LVDS (Low Voltage Differential Signal) Output Electrical Specifications (1 of 2)

| Symbol                         | Parameter                                    | Notes | Minimum | Typical | Maximum | Units |
|--------------------------------|----------------------------------------------|-------|---------|---------|---------|-------|
| DR <sub>OUT</sub>              | Output Signal Data Rate (reclockers enabled) | —     | 42      | —       | 3200    | Mbps  |
| V <sub>OCM</sub>               | Output average common mode range             | 2     | —       | 1200    | —       | mV    |
| t <sub>r</sub> /t <sub>f</sub> | GPL: rise/fall time (20–80%)                 | —     | —       | 75      | 130     | ps    |
| V <sub>OD</sub>                | GPL: differential output (P–P)               | 3     | 500     | 650     | 800     | mV    |
| V <sub>OD</sub>                | RRL: differential output (P–P)               | —     | 300     | 450     | 550     | mV    |

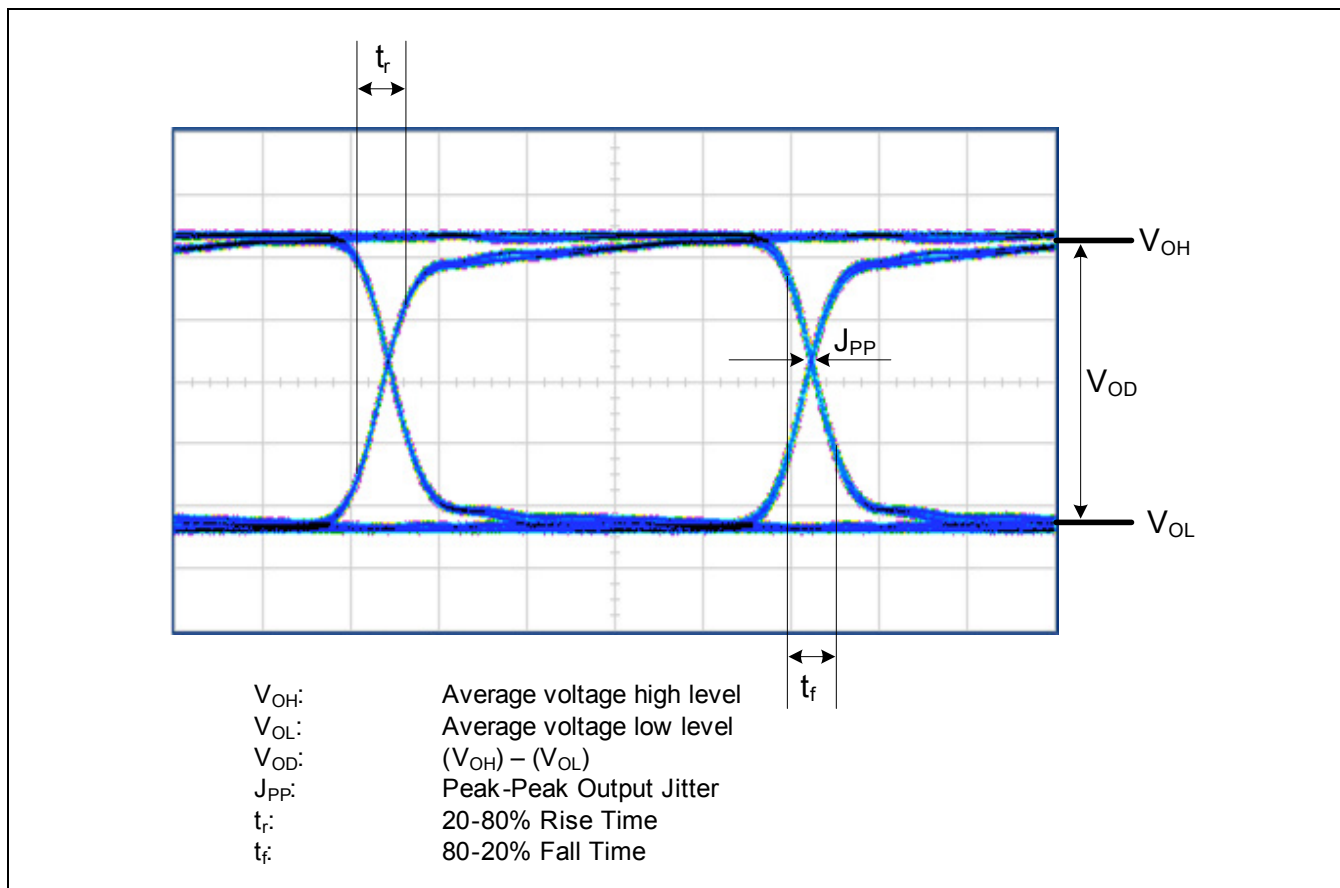
**Table 2-7. LVDS (Low Voltage Differential Signal) Output Electrical Specifications (2 of 2)**

| Symbol    | Parameter                              | Notes | Minimum | Typical | Maximum | Units    |
|-----------|----------------------------------------|-------|---------|---------|---------|----------|
| $R_{OUT}$ | Output termination (differential)      | —     | 90      | 100     | 130     | $\Omega$ |
| $S_{22}$  | Output return loss (40 MHz to 2.5 GHz) | —     | —       | -15.0   | —       | dB       |

**NOTES:**

1. Specified at recommended operating conditions—see Table 2-2.
2. Computed as average (average positive output and average negative output).
3. Conforms to IEEE Std 1596.3—1996 for GPL. All values specified for 50 $\Omega$  single-ended backmatch, 100 $\Omega$  differential load.
4. All output swings defined with pre-emphasis off.
5. See Figure 2-2 for definitions of eye parameters.

**Figure 2-2. Definitions of Eye Parameters**



**Table 2-8. Input Equalization Performance Specifications**

| Symbol           | Parameter                               | Notes      | Minimum | Typical | Maximum | Units |
|------------------|-----------------------------------------|------------|---------|---------|---------|-------|
| DR <sub>IN</sub> | Input signal data rate                  | —          | 42      | —       | 3200    | Mbps  |
| —                | Maximum error-free distance at 3.2 Gbps | 2, 3, 6, 7 | —       | —       | 60      | in    |
| —                | Maximum error-free distance at 1.6 Gbps | 2, 3, 6, 7 | —       | —       | 72      | in    |

**NOTES:**

1. Specified at recommended operating conditions—see [Table 2-2](#).
2. Performance measured on standard FR4 backplane such as standards provided by TYCO for 10GE XAUI.
3. Measured with PCML driver without output pre-emphasis at a minimum launch voltage of 900 mVpp output swing at beginning of line.
4. Combined input equalization + output pre-emphasis performance will be better than individual performance, but less than the sum of the two lengths.
5. Input equalization has greatest effect for data rates higher than 1 Gbps.
6. Default setting optimized for driving 10–46 in of PCB trace length. Equalizer can be configured for longer reach using serial interface.
7. Test setup: Pattern generator ⇒ test backplane ⇒ DUT ⇒ error detector

**Table 2-9. Output Pre-Emphasis Performance Specifications**

| Symbol            | Parameter                               | Notes   | Minimum | Typical | Maximum | Units |
|-------------------|-----------------------------------------|---------|---------|---------|---------|-------|
| DR <sub>OUT</sub> | Output signal data rate                 | —       | 42      | —       | 1600    | Mbps  |
| —                 | Maximum error-free distance at 3.2 Gbps | 2, 3, 6 | —       | —       | 40      | in    |
| —                 | Maximum error-free distance at 1.6 Gbps | 2, 3, 6 | —       | —       | 60      | in    |

**NOTES:**

1. Specified at recommended operating conditions—see [Table 2-2](#).
2. Performance measured on standard FR4 backplane such as standards provided by TYCO for 10GE XAUI.
3. Measured with PCML receiver without input equalization, using PCML output driver at 1200 mVpp output swing at beginning of line.
4. Combined adaptive equalization + output pre-emphasis performance will be better than individual performance, but less than the sum of the two lengths.
5. Output pre-emphasis has greatest effect for data-rates higher than 1 Gbps.
6. Test setup: Pattern generator ⇒ DUT ⇒ test backplane ⇒ error detector

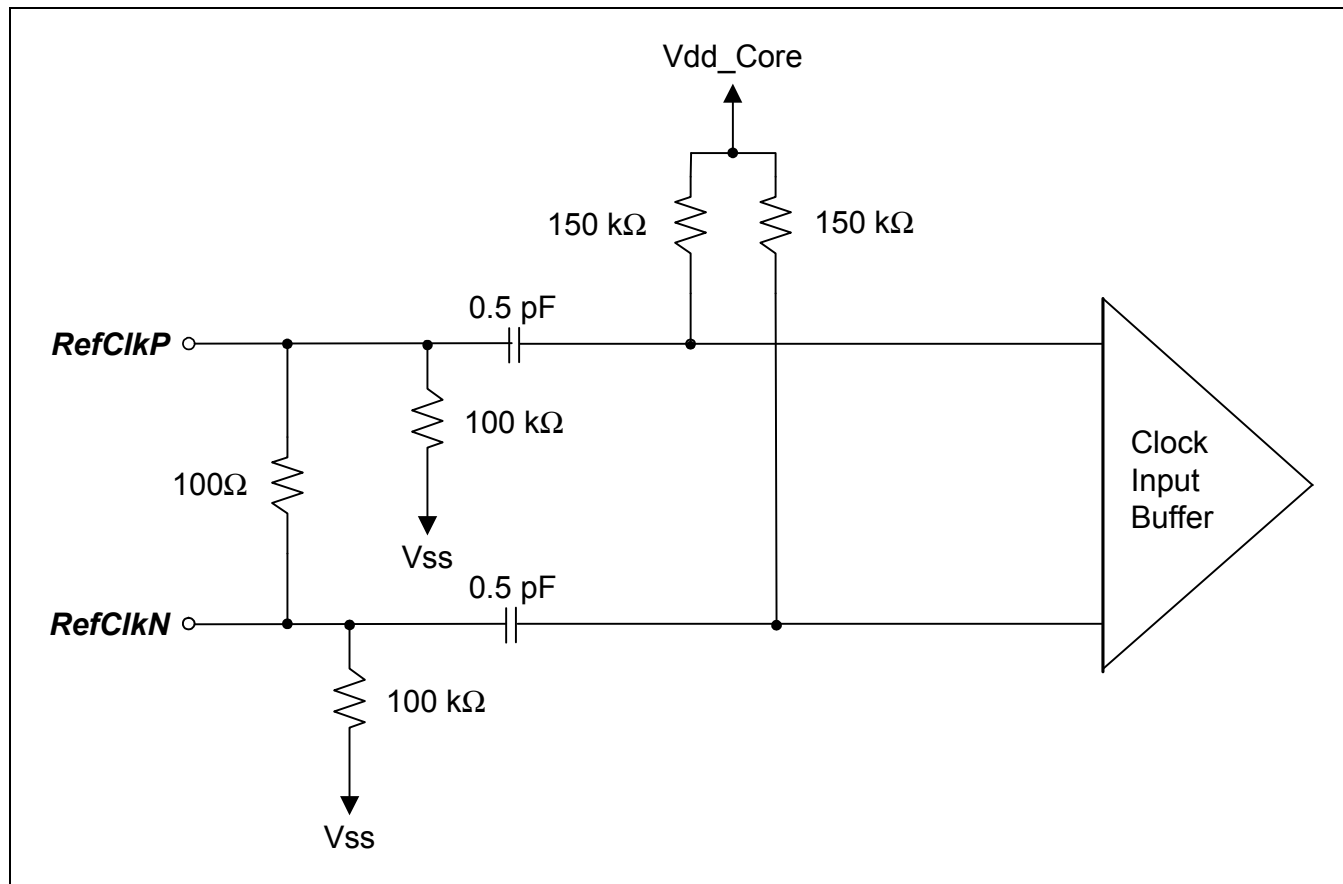
Table 2-10. Reference Clock Input

| Symbol    | Parameter                                          | Notes | Minimum | Typical | Maximum         | Units      |
|-----------|----------------------------------------------------|-------|---------|---------|-----------------|------------|
| $F_{ref}$ | Input frequency ( <i>Refclk_ctrl</i> [3:1] = 000b) | 2, 3  | 10      | 19.44   | 25              | MHz        |
| $F_{ref}$ | Input frequency ( <i>Refclk_ctrl</i> [3:1] = 001b) | 2, 3  | 20      | 38.88   | 50              | MHz        |
| $F_{ref}$ | Input frequency ( <i>Refclk_ctrl</i> [3:1] = 010b) | 2, 3  | 40      | 77.76   | 100             | MHz        |
| $F_{ref}$ | Input frequency ( <i>Refclk_ctrl</i> [3:1] = 011b) | 2, 3  | 80      | 155.52  | 200             | MHz        |
| $F_{ref}$ | Input frequency ( <i>Refclk_ctrl</i> [3:1] = 100b) | 2     | 120     | 250     | 300             | MHz        |
| $F_{ref}$ | Input frequency ( <i>Refclk_ctrl</i> [3:1] = 101b) | 2, 3  | 160     | 311.04  | 400             | MHz        |
| $F_{ref}$ | Input frequency ( <i>Refclk_ctrl</i> [3:1] = 110b) | 2, 3  | 320     | 622.08  | 800             | MHz        |
| $V_{ID}$  | Input differential voltage (P–P)                   | 4, 5  | 100     | —       | 1600            | mV         |
| $V_{ICM}$ | Input common-mode voltage                          | 2, 5  | 250     | —       | <i>AVdd_I/O</i> | mV         |
| —         | Input duty cycle                                   | —     | 40      | 50      | 60              | %          |
| —         | Frequency stability                                | 2     | —       | —       | 100             | ppm        |
| $R_{IN}$  | Differential termination                           | 5     | —       | 100     | —               | $\Omega$   |
| —         | Internal pull-down to <b>Vss</b>                   | —     | —       | 100     | —               | k $\Omega$ |
| —         | Maximum DC input current                           | —     | —       | —       | 15              | mA         |

**NOTES:**

- Specified at recommended operation conditions—see Table 2-2.
- Used for frequency acquisition.
- Typical values are exact integer ratios for SONET applications.
- Example 1200 mV<sub>pp</sub> differential = 600 mV<sub>pp</sub> for each single-ended terminal.
- Input can accept a CMOS single-ended clock on differential P terminal when differential N terminal is decoupled to ground with a large enough capacitor. CMOS input will then see an effective 100 $\Omega$  load.
- See Figure 2-3 for input termination circuit.

Figure 2-3. Reference Clock Input Internal Circuitry



## 2.5 High-Speed Performance Specifications

**Table 2-11. CDR/RCLK High-Speed Performance (1 of 2)**

| Symbol           | Parameter                                            | Notes    | Minimum | Typical | Maximum | Units |
|------------------|------------------------------------------------------|----------|---------|---------|---------|-------|
| DR <sub>IN</sub> | Input signal data rate (NRZ data) divider ratio = 1  | —        | 2       | —       | 3.2     | Gbps  |
| DR <sub>IN</sub> | Input signal data rate (NRZ data) divider ratio = 2  | —        | 1       | —       | 1.6     | Gbps  |
| DR <sub>IN</sub> | Input signal data rate (NRZ data) divider ratio = 4  | —        | 500     | —       | 800     | Mbps  |
| DR <sub>IN</sub> | Input signal data rate (NRZ data) divider ratio = 8  | —        | 250     | —       | 400     | Mbps  |
| DR <sub>IN</sub> | Input signal data rate (NRZ data) divider ratio = 12 | —        | 167     | —       | 267     | Mbps  |
| DR <sub>IN</sub> | Input signal data rate (NRZ data) divider ratio = 16 | —        | 125     | —       | 200     | Mbps  |
| DR <sub>IN</sub> | Input signal data rate (NRZ data) divider ratio = 24 | —        | 83      | —       | 133     | Mbps  |
| DR <sub>IN</sub> | Input signal data rate (NRZ data) divider ratio = 32 | —        | 62.5    | —       | 100     | Mbps  |
| DR <sub>IN</sub> | Input signal data rate (NRZ data) divider ratio = 48 | —        | 42      | —       | 67      | Mbps  |
| J <sub>TOL</sub> | Jitter tolerance (Figure 2-5)                        | 2        | —       | 0.625   | —       | UI    |
| J <sub>TRF</sub> | Jitter transfer (Figure 2-6)                         | 2, 16    | —       | —       | —       | —     |
| J <sub>GEN</sub> | Jitter generation (rms) at STS-N (N = 1, 3, 12, 48)  | 2, 12    | —       | 4.5     | 6.5     | mUI   |
| J <sub>GEN</sub> | Jitter generation (pp) at STS-N (N = 1, 3, 12, 48)   | 2, 12    | —       | 30      | 55      | mUI   |
| F <sub>LBW</sub> | Default loop bandwidth: divider ratio = 1            | 3, 4, 5  | —       | —       | 2       | MHz   |
| F <sub>LBW</sub> | Default loop bandwidth: divider ratio = 2            | 3, 4, 5  | —       | —       | 1       | MHz   |
| F <sub>LBW</sub> | Default loop bandwidth: divider ratio = 4            | 3, 4, 5  | —       | —       | 500     | KHz   |
| F <sub>LBW</sub> | Default loop bandwidth: divider ratio = 8            | 3, 4, 5  | —       | —       | 250     | KHz   |
| F <sub>LBW</sub> | Default loop bandwidth: divider ratio = 12           | 3, 4, 5  | —       | —       | 167     | KHz   |
| F <sub>LBW</sub> | Default loop bandwidth: divider ratio = 16           | 3, 4, 5  | —       | —       | 125     | KHz   |
| F <sub>LBW</sub> | Default loop bandwidth: divider ratio = 24           | 3, 4, 5  | —       | —       | 83      | KHz   |
| F <sub>LBW</sub> | Default loop bandwidth: divider ratio = 32           | 3, 4, 5  | —       | —       | 62.5    | KHz   |
| F <sub>LBW</sub> | Default loop bandwidth: divider ratio = 48           | 3, 4, 5  | —       | —       | 41.6    | KHz   |
| R <sub>j</sub>   | Output data random jitter (pp)                       | 13       | —       | —       | 100     | mUI   |
| D <sub>j</sub>   | Output data deterministic jitter (pp)                | 13       | —       | —       | 110     | mUI   |
| T <sub>j</sub>   | Output data total jitter (pp)                        | 13       | —       | —       | 210     | mUI   |
| J <sub>rms</sub> | Output data broadband jitter (rms)                   | 14, 15   | —       | 13      | 40      | mUI   |
| J <sub>pp</sub>  | Output data broadband jitter (pp)                    | 14, 15   | —       | 75      | 230     | mUI   |
| T <sub>LAT</sub> | Latency from input to output (utilizing CDR)         | —        | —       | 1.75    | 2       | ns    |
| CH <sub>SK</sub> | Channel to channel output data skew (utilizing CDR)  | —        | —       | 10      | 65      | ps    |
| —                | Initialization time                                  | 6, 7, 10 | —       | 2       | —       | ms    |
| T <sub>FRA</sub> | Frequency acquisition time                           | 6, 8     | —       | 0.4     | —       | ms    |

## CDR/Reclocker with 4:1 Input Multiplexer

Rev V3

Table 2-11. CDR/RCLK High-Speed Performance (2 of 2)

| Symbol           | Parameter                            | Notes | Minimum | Typical | Maximum | Units |
|------------------|--------------------------------------|-------|---------|---------|---------|-------|
| T <sub>PLL</sub> | Phase lock time with 100 ppm delta F | 9, 11 | —       | —       | 100     | ns    |
| T <sub>PLL</sub> | Phase lock time with 0 ppm delta F   | 9, 11 | —       | —       | 50      | ns    |

**NOTES:**

- Specified at recommended operating conditions—see Table 2-2.
- Jitter tolerance, jitter transfer, and jitter generation specified with input equalization and output pre-emphasis disabled, utilizing PRBS 2<sup>23</sup>-1, per GR-253 test methodologies.
- Nominal loop bandwidth for 2.48832 GHz/ DRD.
- Bandwidth is proportional to frequency.
- For SONET data rates, default meets SONET specifications.
- Assume that reference is within  $\pm 100$  ppm of desired data rate.
- Time after power up, reset, or data rate change.
- Time from application of valid data to lock within  $\pm 20\%$  of lock phase.
- Defined as when phase settles to within 20% of lock phase.
- After reset (master or soft), initialization takes place, then frequency acquisition.
- Based on nominal SONET bandwidth (bandwidth can be increased for lower phase lock time).
- Jitter generation specified per GR-253, utilizing bandpass filter with passband 12 KHz to 20 MHz for STS-48.
- R<sub>j</sub>, D<sub>j</sub>, T<sub>j</sub> represent jitter measured to BER of 10<sup>-12</sup> per FC-PI-2 specifications.
- Broadband jitter defined as jitter measured on sampling oscilloscope without the use of filters.
- Maximum value specified incorporates asynchronous aggressors.
- Jitter transfer of CDR meets the SONET STS-48 mask if loop bandwidth is set to 80% of nominal by writing *Phadj\_ctrl\_N*[5:4] = 00b. Jitter transfer at STS-12 (STS-3) exceeds mask by 0.1 dB in frequency range 10 - 25.1 KHz (1.5 - 10 KHz).

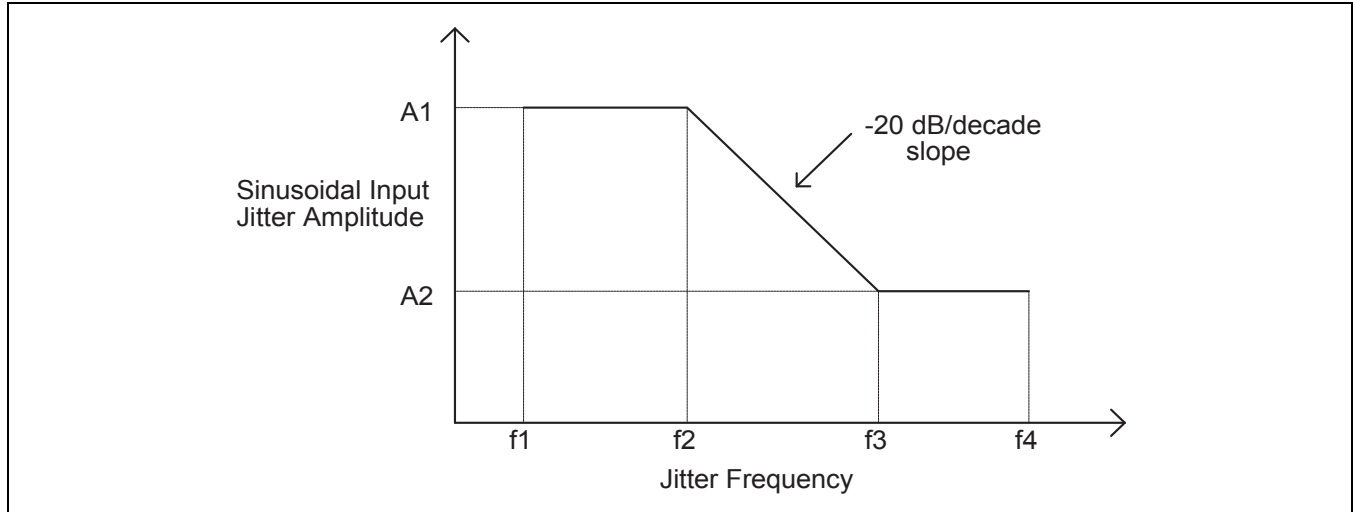
Table 2-12. CDR/RCLK Alarm Performance

| Symbol            | Parameter                                                                     | Notes | Minimum   | Typical    | Maximum      | Units |
|-------------------|-------------------------------------------------------------------------------|-------|-----------|------------|--------------|-------|
| DT <sub>LOA</sub> | <b>xLOA</b> decision time                                                     | 5     | —         | 26         | —            | μs    |
| —                 | <b>xLOA</b> assertion transition density threshold ( <b>xLOA</b> = H to L)    | 5, 6  | —         | 12.5       | —            | %     |
| —                 | <b>xLOA</b> de-assertion transition density threshold ( <b>xLOA</b> = L to H) | 5, 6  | —         | 12.5       | —            | %     |
| DT <sub>LOL</sub> | <b>xLOL</b> decision time (measurement time)                                  | 2     | 10        | 420        | 3275         | μs    |
| WRW               | <b>xLOL</b> assertion frequency threshold ( <b>xLOL</b> = H to L)             | 2, 3  | $\pm 185$ | $\pm 2930$ | $\pm 250000$ | ppm   |
| NRW               | <b>xLOL</b> de-assertion frequency threshold ( <b>xLOL</b> = L to H)          | 2, 3  | $\pm 120$ | $\pm 1955$ | $\pm 250000$ | ppm   |

**NOTES:**

- Specified at recommended operating conditions—see Table 2-2.
- Actual time is set with LOL window. Typical is the default value. Minimum and maximum indicate dynamic range.
- Assume that reference is  $\pm 50$  ppm of operating frequency.
- Computed for 1.4835 Gbps data rate. Will scale with data rate.
- Fixed values.
- Specification shown represents deviation from 50% transition density.

**Figure 2-4. Jitter Tolerance Specification Mask**



**Table 2-13. SMPTE Jitter Tolerance Mask**

| Jitter Parameter | SMPTE 259M | SMPTE 292M |
|------------------|------------|------------|
| f1               | 10 Hz      | 10 Hz      |
| f3               | 1 kHz      | 100 kHz    |
| f4               | >27 MHz    | >148.5 Mhz |
| A1               | 1.0 UI     | 1.0 UI     |
| A2               | 0.2 UI     | 0.2 UI     |

**Figure 2-5. SONET Jitter Tolerance Specification Mask**

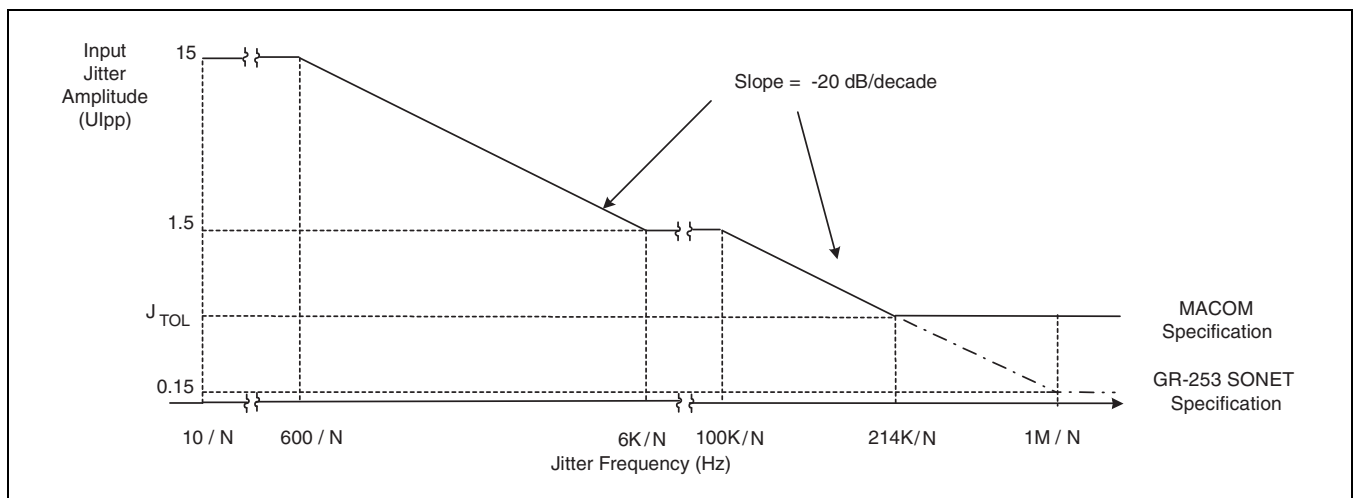


Figure 2-6. Jitter Transfer Specification Mask

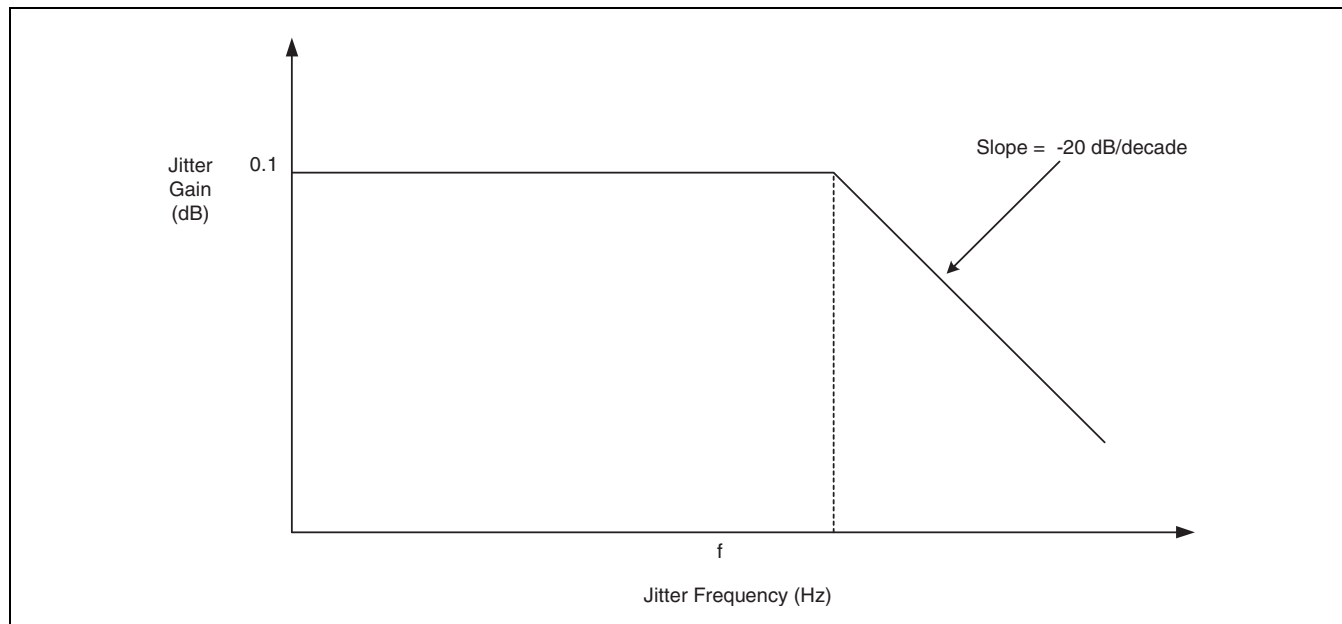


Table 2-14. Loop Bandwidths for Typical Video Data Rates

| Application       | Bit Rate (Mbps) | Value of N | Approximate Loop BW (f) |
|-------------------|-----------------|------------|-------------------------|
| 2xHD-SDI          | 2967/2970       | 0.84       | 2.38 MHz                |
| HD-SDI            | 1485/1483.5     | 1.68       | 1.19 MHz                |
| 2xSD-SDI          | 540             | 4.6        | 435 MHz                 |
| Progressive Scan  | 360             | 6.9        | 290 KHz                 |
| SD-SDI            | 270             | 9.2        | 217 KHz                 |
| Legacy Comp Video | 177             | 14.1       | 142 KHz                 |
| Legacy Comp Video | 143             | 17.4       | 115 KHz                 |

## 2.6 Package Drawings and Surface Mount Assembly Details

The M21262 is assembled in 72-pin 10 mm x 10 mm MicroLeadFrame (MLF) packages. This is a plastic encapsulated package with a copper leadframe. The MLF is a leadless package with lands on the bottom surface of the package.

The exposed die paddle serves as the IC ground (**V<sub>ss</sub>**), and the primary means of thermal dissipation. This die paddle should be soldered to the PCB. A cross-section of the MLF package can be found in [Figure 2-7](#).

**Figure 2-7. Cross-Section of MLF Package**

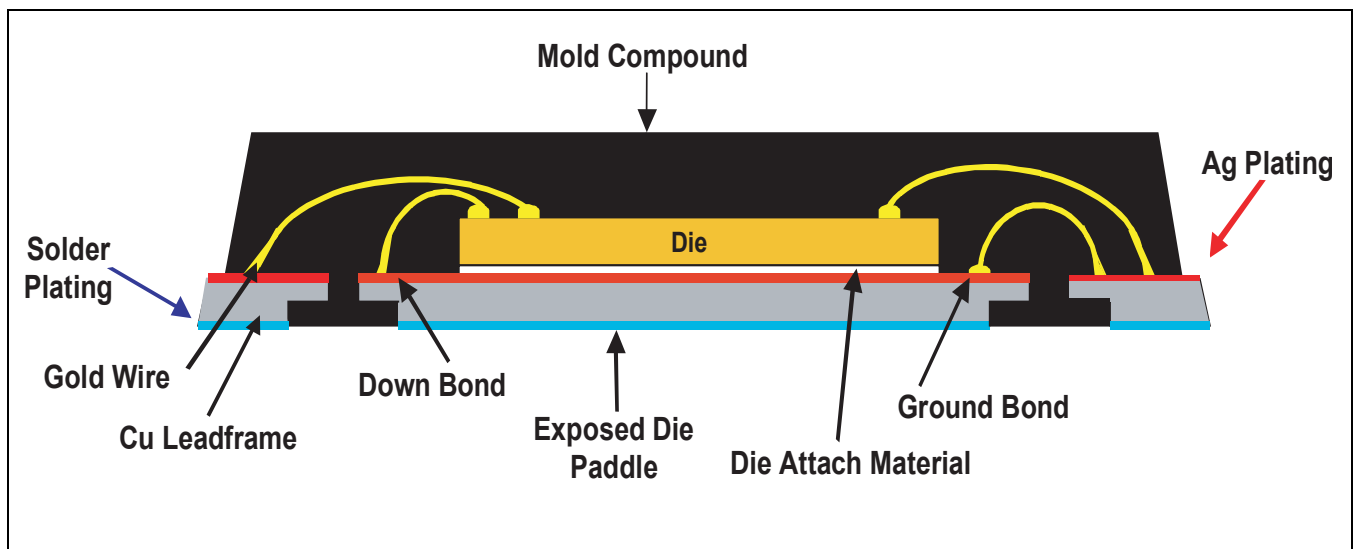


Figure 2-8 and Figure 2-9 shows the package outline drawing for the 10 mm x 10 mm MLF package.

**Figure 2-8. Package Drawing (1 of 2)**

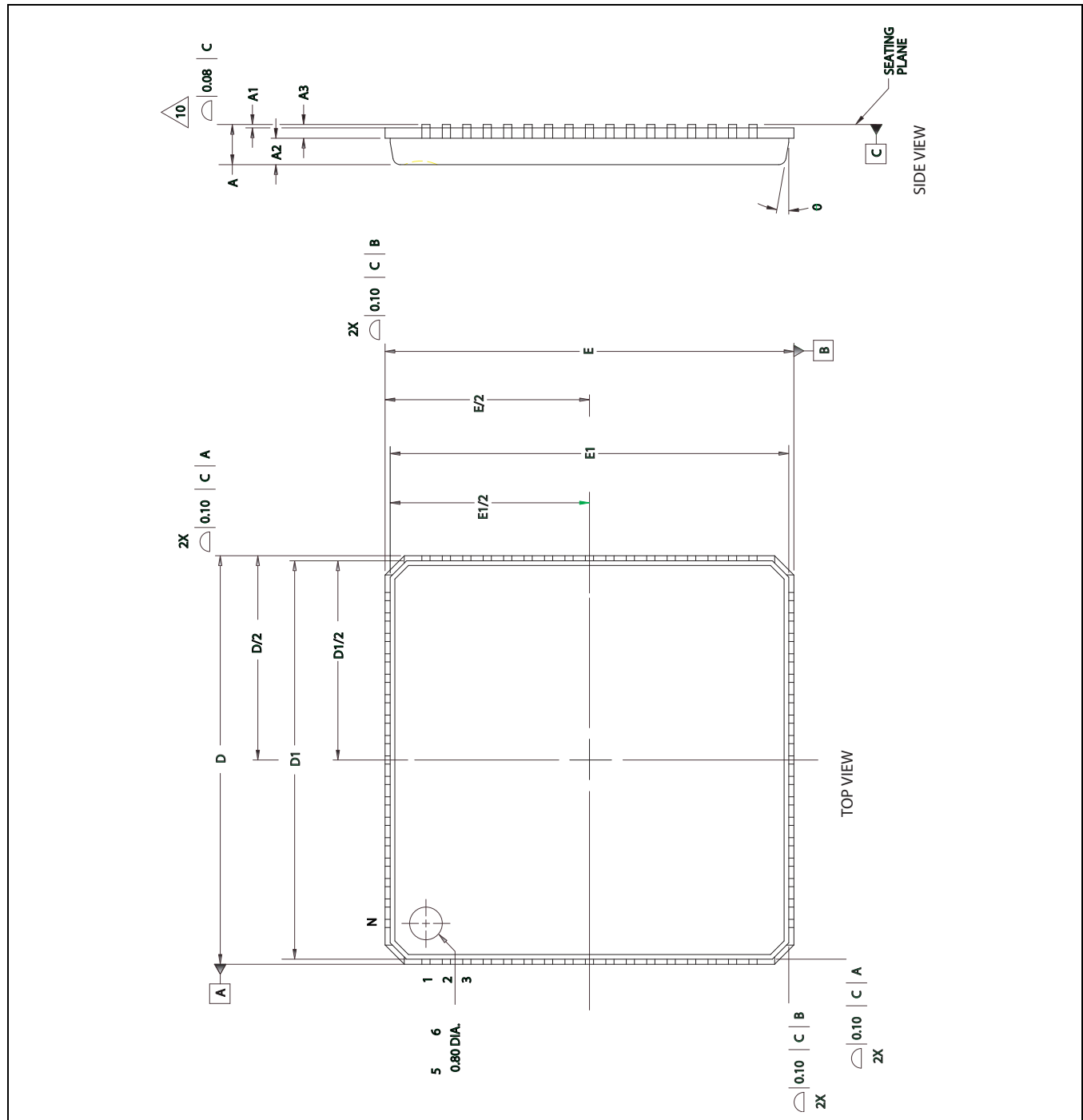
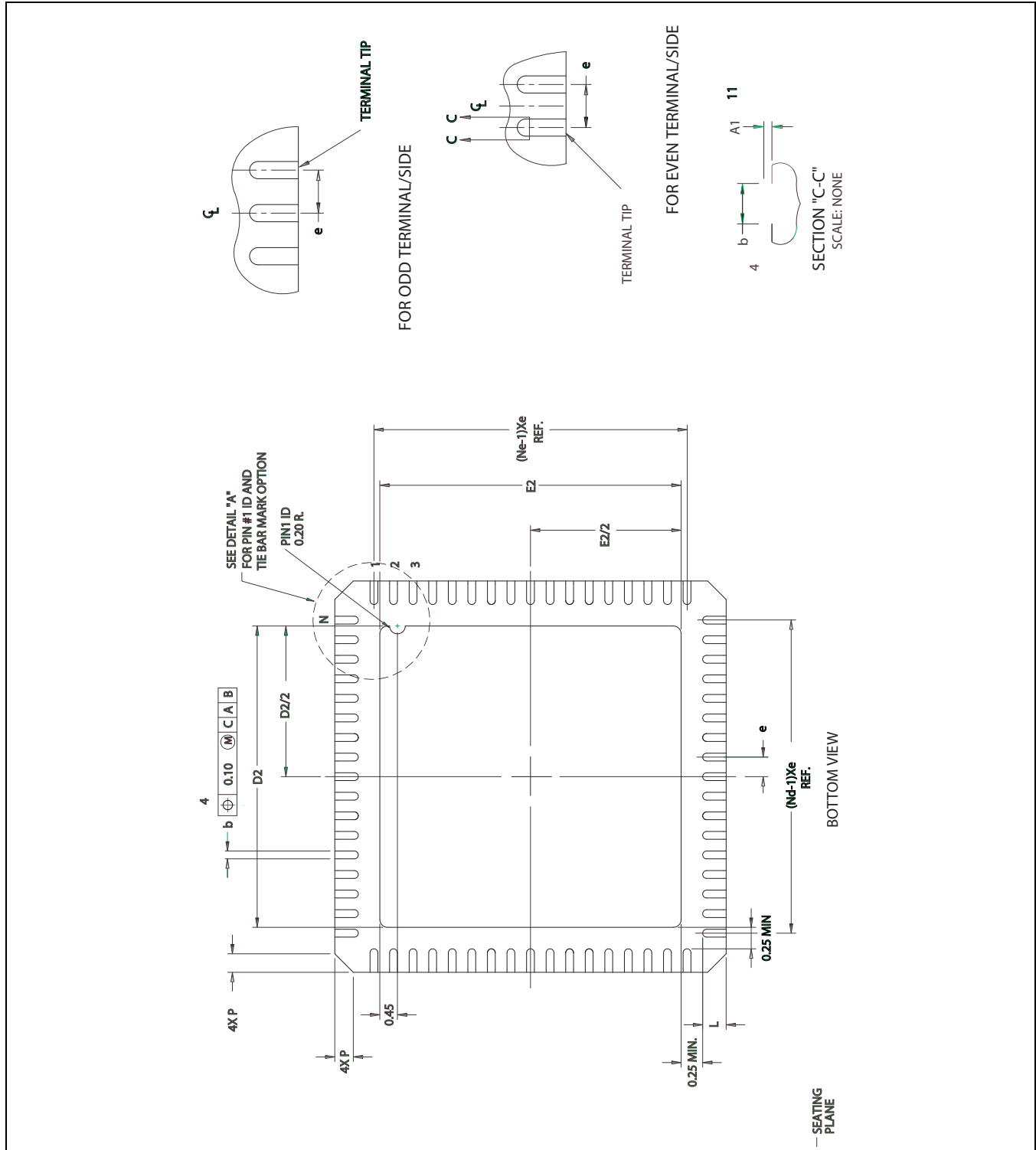
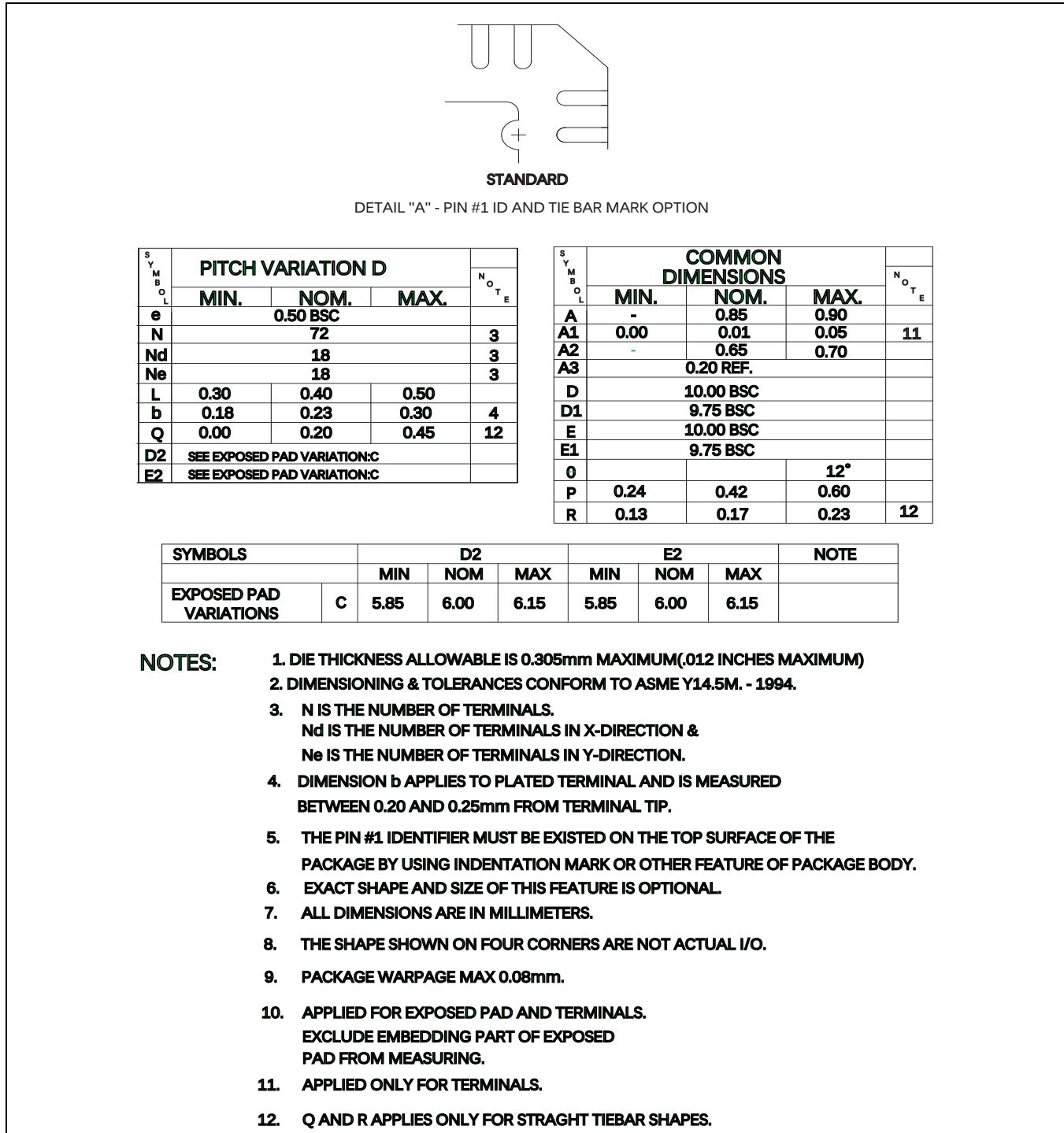


Figure 2-9. Package Drawing (2 of 2)



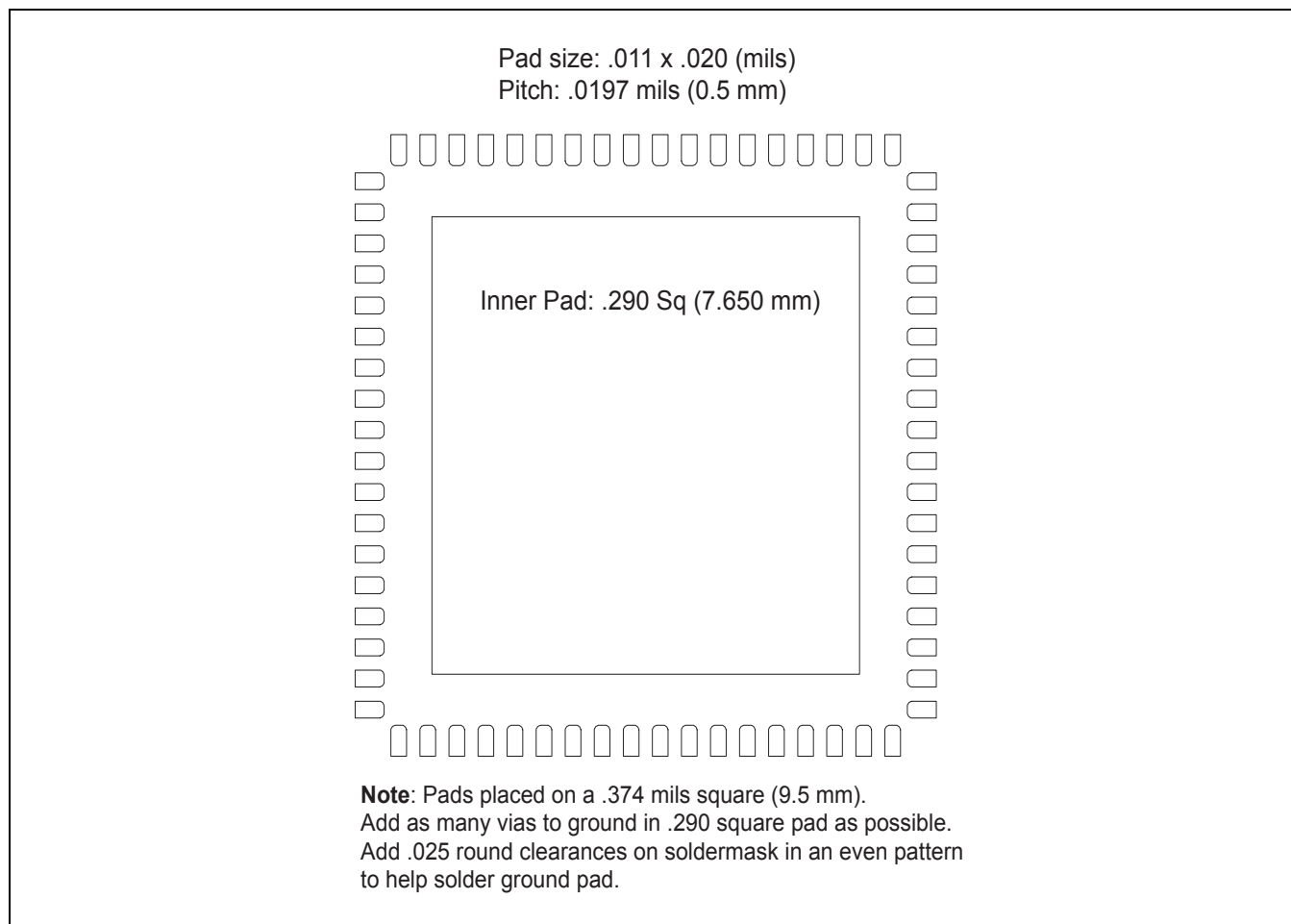
The relevant dimensions for the 72-pin version of the package can be found in [Figure 2-10](#).

**Figure 2-10. 72-Pin Package Dimensions**



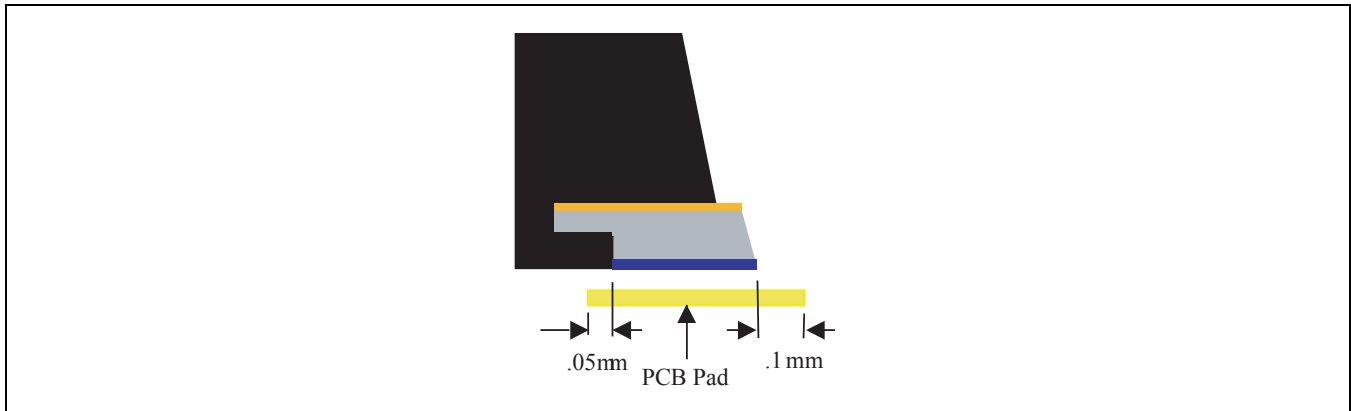
The M21262 evaluation module (EVM) uses the PCB footprint shown in [Figure 2-11](#).

**Figure 2-11. PCB Footprint for 72-Pin 10 mm MLF Package**



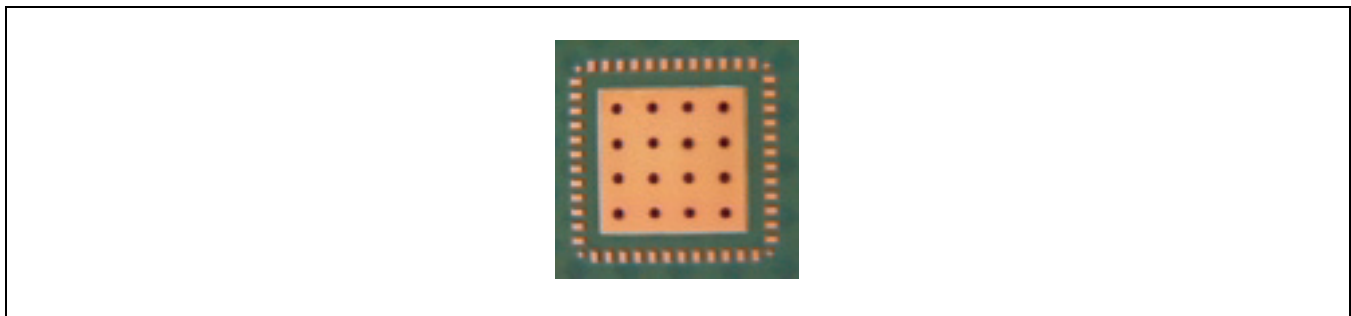
The pad length dimensions should account for component tolerances, PCB tolerances, and placement tolerances. At a minimum, the pad should extend at least 0.1 mm on the outside and 0.05 mm on the inside, as shown in Figure 2-12.

**Figure 2-12. PCB Pad Extensions**



To efficiently dissipate heat from the M21262, a thermal pad with thermal vias should be used on the PCB. An example of a thermal pad with a 4x4 via array is shown in Figure 2-13. The thermal vias provide a heat conduction path to inner and/or bottom layers of the PCB. The larger the via array, the lower the thermal resistance ( $\theta_{ja}$ ). It is recommended to use thermal vias with 1.0 to 1.2 mm pitch with 0.3 to 0.33 mm via diameter.

**Figure 2-13. Recommended Via Array for Thermal Pad**



For further details please refer to the relevant application note from package vendor Amkor (see list of references at the end of this document). Much of the material in this section has been adopted from the Amkor SMT application note.

## 2.7 PCB High-Speed Design and Layout Guidelines

A single power plane for the **AVdd\_IO** and **AVdd\_Core** power supplies with bulk capacitors (typically 10  $\mu$ F) distributed throughout the board will mitigate most power-rail related voltage transients. A bulk capacitor should also be placed where the power enters the board. It is recommended that decoupling capacitors only be routed directly to the power pin if they can be placed within 1/8 of an inch of the pin. Decoupling capacitors should be dispersed around the outside of the device on the top side and underneath the IC on the bottom side of the board. It is recommended that 0.1  $\mu$ F and 0.01  $\mu$ F decoupling capacitors be used. All three capacitor values are not required on each pin, but should be dispersed uniformly to filter different frequencies of noise.

A continuous ground plane is the best way to minimize ground impedance. Return currents and power supply transients produce most ground noise during switching. Reducing ground plane impedance minimizes this effect. There is a high frequency decoupling effect from the capacitive effect of power/ground planes and this can be used to help minimize the amount of high frequency decoupling capacitors.

High-speed PCML signals should be routed with 50 $\Omega$  equal length traces for P and N signals within each differential pair. Buried strip line is recommended for internal layers while microstrip line is used for signals routed on surface layers. There should be no discontinuity in the ground planes during the path of the signal traces.

Impedance discontinuities occur when a signal passes through vias and travels between layers. It is recommended to minimize the number of vias and layers that the transmit/receive signals travel through in the design. The system PCB should be designed so that high-speed signals pass through a minimal number of vias and remain on a single internal high-speed routing layer.

When vias need to be used, the via design should match the transmission line impedance by observing the following:

- Avoid through-hole vias; they cause stubs by extending the full cross-section of the PCB despite the fact that the layer change requires only a small length via (as in the case of adjacent layers). Use short blind vias.
- Avoid layer changes in general as the characteristic impedance of the transmission line changes as a result.

In general, some general rules for PCB design for high data rates are:

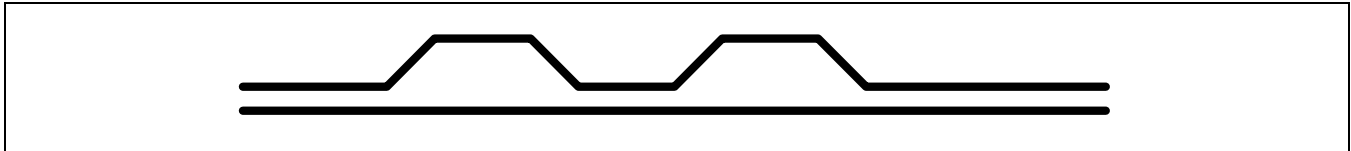
- PCB trace width for high-speed signals should closely match the SMT component width, so as to prevent stub effects from a sudden change in stripline width. A gradual increase in trace width is recommended as it meets the SMT pad.
- The PCB ground/power planes should be removed from under the I/O pins so as to reduce parasitic capacitance.
- High-speed traces should avoid sharp changes in direction. Using large radii will minimize impedance changes. Avoid bending traces by more than 45 degrees; otherwise, provide a circular bend so as to prevent the trace width from widening at the bend.
- Avoid trace stubs by minimizing components (resistors, capacitors) on the board. For instance, a termination resistor at the input of a receiver will inflict a stub effect at high frequency. Termination resistors integrated on chip will eliminate the stub. Components designed to DC couple to one another avoid the need for coupling capacitors and the inherent stubs created from them.

For high-speed differential signals, the trace lengths of each side of the differential pair should be matched to each other as much as possible. The skew between the P and N signals in a differential pair should be tightly controlled in order for the differential receiver to detect a valid data transition. When matching trace lengths within a

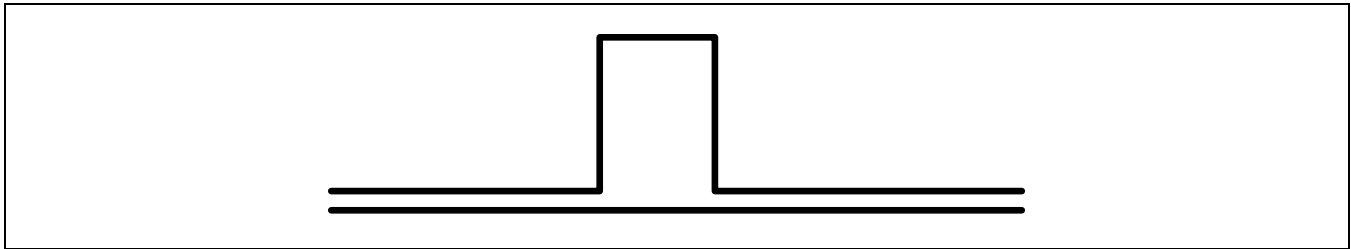
differential pair, care should be taken to avoid introducing large impedance discontinuities. The figures below show two methods of matching the trace lengths for a differential pair.

Typically, the preferred solution for trace length matching in differential pairs is to use a serpentine pattern for the shorter signal as shown in Figure 2-14. Using a serpentine pattern for length matching will minimize the differential impedance discontinuity while making both trace lengths equal.

**Figure 2-14. Trace Length Matching Using Serpentine Pattern**



**Figure 2-15. Loop Length Matching for Differential Traces**



The loop length matching method shown in Figure 2-15 will match the trace lengths of a differential pair, but will create a large impedance discontinuity in the transmission line, which could result in higher jitter on the signal and/or a greater sensitivity to noise for the differential pair.

When using capacitors to AC-couple the input, care should be taken to minimize the pattern-dependant jitter ( $PD_J$ ) associated with the low-frequency cutoff of the coupling network. When NRZ data containing long strings of 1s or 0s is applied to a high-pass filter, a voltage droop occurs. This voltage droop causes  $PD_J$  in much the same fashion as inter-symbol interference (ISI) is generated from dispersion effects of long trace lengths in backplane material.

If needed, use 0.1  $\mu$ F capacitors to AC-couple the high-speed output signals, and the reference clock inputs. The high-speed data input signals can be DC-coupled.

On the Evaluation Module (EVM), we have tied **DVdd\_I/O** and **AVdd\_I/O** together to minimize the number of power supply jacks. They are kept separate on-chip to give the flexibility to the system designers to supply a different voltage level for each. For instance, an FPGA can be used to supply power to **DVdd\_I/O**, while a lower voltage can be used to power **AVdd\_I/O** to minimize power dissipation. On the EVM, we have also tied **DVdd\_Core** and **AVdd\_Core** together to minimize the number of power supply jacks. They are kept separate on-chip to provide more isolation, however, if the system board plane is properly decoupled, they can be tied together.

No inductive filtering on the system board is necessary between different power supplies of the IC. It is up to the system designer to determine if this needs to be considered for supplies that are coming from other parts of the system board (such as switching regulators or ASICs).

An inductor should not be used at the **VddT** pins. These pins were made available to create a low AC impedance, such that the 50 $\Omega$  on-chip termination impedances see a common AC ground. This assures both common-mode and differential termination. If common-mode termination is not important (such as in LVDS applications), simply

leave the **VddT** pins floating. Note that a low AC impedance can also be created by tying the **VddT** pins to the **AVdd\_I/O** plane, thus saving on the number of external capacitors. This, however, implies a CML-like data interface (unless the data is AC-coupled). **VddT** is not really a supply plane on-chip, it is simply the point to which the 50Ω input impedances are tied.

Power planes should be decoupled to ground planes using thin dielectric layers, to increase capacitance (preferably 2–4 mils). Reference ground layers should be used on both sides of inner layer routing planes, with controlled impedance. The total board thickness should meet the standard drill holes to board thickness ratio of 1:12 or 1:14.

Use 1/2 ounce copper clad on all layers, which is approximately 0.7 mils. Avoid placing solder mask and silkscreen on top of transmission lines; solder mask will add 1–2Ω to the overall impedance of the transmission line. Dielectric core material should be used wherever possible, as it will maintain its thickness and geometry during processing, better than pliable prepreg.

The microwave ground should follow the transmission line from end to end, or from signal input to output. It is best to designate layers as dedicated microwave/circuit ground planes, and properly isolate them from other ground planes by providing adequate distance. All microwave ground planes should be tied together.

Uncoupled microstrip transmission lines should be placed at a distance from each other of at least three times the transmission line width. Coupled microstrip transmission lines, such as differential signal pairs, must be placed close to each other and maintain the same separation distance throughout the board (separation distance of at most twice the trace width). For buried stripline transmission lines, it is good design practice to maintain equal distance between the conductor and the ground plane on both sides.

During PCB manufacturing, over- and under-etching of traces used for transmission lines results in impedance discontinuities. Use of wide traces for transmission lines will reduce the impact of etching issues. Wide traces also help compensate for skin-effect losses in transmission lines. It should be noted, however, that the wider the traces in a differential pair, the thicker the underlying dielectric layer needs to be.

Surface mount connectors are preferred over through-mount connectors. Connectors should be selected that have controlled characteristic impedances that match the characteristic impedances of the transmission lines.

## 2.8 Auto Rate Detect (ARD)

For many video applications, CDR/reclockers are required to auto rate detect (ARD) the incoming data rate. MACOM has developed a reference design for an ARD implementation. The reference design includes binary files for the ARD software and a hardware reference design based on the ATMEL AT89C51Rx2 series of micro controllers. The ARD automatically configures the device for nine possible fixed data rates of 143, 177, 270, 360, 540, 1483.5, 1485, 2967, or 2970 Mbps for the M21262. If desired, customers can expand the ARD code to include operation at other data rates.

Please refer to the M2125x and M2126x ARD software description documents for details on MACOM's implementation of ARD for this device.

## 3.0 Registers

**Table 3-1. Register Table Summary**

| Addr                    | Register Name           | d7: MSB     | d6          | d5          | d4          | d3            | d2           | d1            | d0: LSB       |
|-------------------------|-------------------------|-------------|-------------|-------------|-------------|---------------|--------------|---------------|---------------|
| <b>Common Registers</b> |                         |             |             |             |             |               |              |               |               |
| 00h                     | <i>Globctrl</i>         | powerup     | RSVD int    | RSVD int    | RSVD int    | RSVD int      | RSVD int     | reserved      | clear_alm     |
| 01h                     | <i>mux_ctrl</i>         | port3[1]    | port3[0]    | port2[1]    | port2[0]    | port1[1]      | port1[0]     | port0[1]      | port0[0]      |
| 04h                     | <i>Refclk_ctrl</i>      | reserved    | reserved    | reserved    | reserved    | ref_divr[2]   | ref_divr[1]  | ref_divr[0]   | RSVD int      |
| 05h                     | <i>Mastreset</i>        | rst         | rst         | rst         | rst         | rst           | rst          | rst           | rst           |
| 06h                     | <i>Chipcode</i>         | chipcode[7] | chipcode[6] | chipcode[5] | chipcode[4] | chipcode[3]   | chipcode[2]  | chipcode[1]   | chipcode[0]   |
| 07h                     | <i>Revcode</i>          | revcode[7]  | revcode[6]  | revcode[5]  | revcode[4]  | revcode[3]    | revcode[2]   | revcode[1]    | revcode[0]    |
| 11h                     | <i>BISTrx_ctrl</i>      | RSVD int    | rx_ctrldr   | RSVD int    | RSVD int    | RSVD int      | rx_patt[0]   | en_rx         | rx_rst        |
| 12h                     | <i>BISTrx_error</i>     | err[7]      | err[6]      | err[5]      | err[4]      | err[3]        | err[2]       | err[1]        | err[0]        |
| 14h                     | <i>BISTtx_chsel</i>     | reserved    | reserved    | reserved    | reserved    | RSVD int      | RSVD int     | RSVD int      | tx_chan_0     |
| 15h                     | <i>BISTtx_ctrl</i>      | err_insert  | rx2txclk    | tx_patt[3]  | tx_patt[2]  | tx_patt[1]    | tx_patt[0]   | en_tx         | tx_rst        |
| 17h                     | <i>BISTtx_LOLctrl</i>   | RSVD int    | RSVD int    | tacq_LOL[0] | RSVD int    | RSVD int      | RSVD int     | narwin_LOL[0] | widwin_LOL[0] |
| 18h                     | <i>BISTtx_PLL_ctrlA</i> | softreset   | RSVD int    | reserved    | RSVD int    | reserved      | RSVD int     | reserved      | RSVD int      |
| 19h                     | <i>BISTtx_PLL_ctrlB</i> | PLLmode[1]  | PLLmode[0]  | RSVD int    | RSVD int    | data_rate[3]  | data_rate[2] | data_rate[1]  | data_rate[0]  |
| 1Ah                     | <i>BISTtx_PLL_ctrlC</i> | VCO_divr[7] | VCO_divr[6] | VCO_divr[5] | VCO_divr[4] | VCO_divr[3]   | VCO_divr[2]  | VCO_divr[1]   | VCO_divr[0]   |
| 1Bh                     | <i>BIST_pattern0</i>    | —           | —           | —           | —           | pattern[19]   | pattern[18]  | pattern[17]   | pattern[16]   |
| 1Ch                     | <i>BIST_pattern1</i>    | pattern[15] | pattern[14] | pattern[13] | pattern[12] | pattern[11]   | pattern[10]  | pattern[9]    | pattern[8]    |
| 1Dh                     | <i>BIST_pattern2</i>    | pattern[7]  | pattern[6]  | pattern[5]  | pattern[4]  | pattern[3]    | pattern[2]   | pattern[1]    | pattern[0]    |
| 1Fh                     | <i>BISTtx_alarm</i>     | tx_LOL      | reserved    | reserved    | RSVD int    | RSVD int      | RSVD int     | RSVD int      | RSVD int      |
| 20h                     | <i>Temp_mon</i>         | —           | —           | —           | —           | reserved      | reserved     | en_temp_mon   | strobe_temp   |
| 21h                     | <i>Temp_value</i>       | —           | —           | —           | —           | temp[3]       | temp[2]      | temp[1]       | temp[0]       |
| 30h                     | <i>Alarm_LOL</i>        | RSVD int    | RSVD int    | RSVD int    | RSVD int    | RSVD int      | RSVD int     | RSVD int      | LOL           |
| 31h                     | <i>Alarm_LOA</i>        | RSVD int    | RSVD int    | RSVD int    | RSVD int    | RSVD int      | RSVD int     | RSVD int      | LOA           |
| 40h                     | <i>RCLK_ctrlA</i>       | softreset   | RSVD int    | inh_force   | RSVD int    | autoinh_en    | RSVD int     | LOA_en        | RSVD int      |
| 41h                     | <i>RCLK_ctrlB</i>       | RCLKmode[1] | RCLKmode[0] | RSVD int    | reserved    | data_rate[3]  | data_rate[2] | data_rate[1]  | data_rate[0]  |
| 42h                     | <i>RCLK_ctrlC</i>       | VCO_divr[7] | VCO_divr[6] | VCO_divr[5] | VCO_divr[4] | VCO_divr[3]   | VCO_divr[2]  | VCO_divr[1]   | VCO_divr[0]   |
| 43h                     | <i>Out_ctrl</i>         | outlvl[1]   | outlvl[0]   | reserved    | reserved    | data_pol_flip | dataout_en   | RSVD int      | RSVD int      |
| 44h                     | <i>Preemp_ctrl</i>      | reserved    | RSVD int    | RSVD int    | RSVD int    | RSVD int      | preemph[2]   | preemph[1]    | preemph[0]    |
| 45h                     | <i>Ineq_ctrl</i>        | reserved    | RSVD int    | RSVD int    | en_DCservo  | RSVD int      | in_eq[2]     | in_eq[1]      | in_eq[0]      |
| 46h                     | <i>Phadj_ctrl</i>       | i_trim[1]   | i_trim[0]   | r_sel[1]    | r_sel[0]    | phase_adj[3]  | phase_adj[2] | phase_adj[1]  | phase_adj[0]  |
| 49h                     | <i>LOL_ctrl</i>         | RSVD int    | RSVD int    | tacq_LOL[0] | RSVD int    | RSVD int      | RSVD int     | narwin_LOL[0] | widwin_LOL[0] |
| 4Ah                     | <i>Jitter_red</i>       | RSVD int    | RSVD int    | RSVD int    | RSVD int    | RSVD int      | RSVD int     | RSVD int      | RSVD int      |

## 3.1 Global Control Registers

### Nomenclature:

1. Reserved bits: bits that exist and reserved for future use by MACOM.
2. Bits not defined and not reserved do not exist.
3. Do not write to reserved or undefined bits—operation not guaranteed.
4. MACOM internal: defines an internal function. Must always write the default value to MACOM internal bits.  
When in doubt, read back default value after reset.

### 3.1.1 Global Control

**Table 3-2. Global Control (Globctrl: Address 00h)**

| Bits | Type | Default | Label         | Description                                                                                                                                                                                                                                                               |
|------|------|---------|---------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7    | R/W  | 1b      | powerup       | Powers up the IC by enabling the current references.<br>0b: Power down the IC<br>1b: Power up the IC (chip powerup)                                                                                                                                                       |
| 6:2  | R/W  | 00000b  | RSVD internal | N/A                                                                                                                                                                                                                                                                       |
| 1    | R/W  | 0b      | Reserved      | N/A                                                                                                                                                                                                                                                                       |
| 0    | R/W  | 0b      | clear_alm     | Clears <i>Alarm_LOL</i> and <i>Alarm_LOL</i> alarm registers (write only) .<br>0b: Normal operation—latch alarm bits<br>1b: Clear alarms<br><b>NOTE:</b> Upon writing a 1b to this bit, it clears the registers, and user needs to write a 0b to enable the normal state. |

### 3.1.2 Input Multiplexer Settings

**Table 3-3. Input Multiplexer Setting (mux\_ctrl: Address 01h)**

| Bits | Type | Default | Label    | Description                                                                                                                          |
|------|------|---------|----------|--------------------------------------------------------------------------------------------------------------------------------------|
| 7:2  | R/W  | 111001  | Reserved | N/A                                                                                                                                  |
| 1:0  | R/W  | 00b     | output   | Determines input channel for output.<br>00b: Selects input 0<br>01b: Selects input 1<br>10b: Selects input 2<br>11b: Selects input 3 |

### 3.1.3 External Reference Frequency Divider Control (RFD)

**Table 3-4. External Reference Frequency Divider Control (RFD) (Refclk\_ctrl: Address 04h)**

| Bits | Type | Default | Label         | Description                                                                                                                                                                                                                    |
|------|------|---------|---------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:4  | R/W  | 0b      | Reserved      | N/A                                                                                                                                                                                                                            |
| 3:1  | R/W  |         | ref_divr      | Sets the divider ratio to scale down <b>RefClk</b> to the internal rate.<br>000b: Divide by 1<br>001b: Divide by 2<br>010b: Divide by 4<br>011b: Divide by 8<br>100b: Divide by 12<br>101b: Divide by 16<br>110b: Divide by 32 |
| 0    | R/W  | 0b      | RSVD internal | N/A                                                                                                                                                                                                                            |

### 3.1.4 Master IC Reset

**Table 3-5. Master IC Reset (Mastreset: Address 05h)**

| Bits | Type | Default | Label | Description                                                                                                                                                                                      |
|------|------|---------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:0  | R/W  | 0b      | rst   | Same feature as hardware <b>xRST</b> . Resets the entire IC.<br>00h: Normal operation [Default]<br>AAh: Reset upon write to this register with AAh<br><b>NOTE:</b> All other values are ignored. |

### 3.1.5 IC Electronic Identification

**Table 3-6. IC Electronic ID (Chipcode: Address 06h)**

| Bits | Type | Default | Label    | Description                                           |
|------|------|---------|----------|-------------------------------------------------------|
| 7:0  | R    | TBD     | chipcode | This register contains the identification of this IC. |

### 3.1.6 IC Revision Code

**Table 3-7. IC Revision Code (Revcode: Address 07h)**

| Bits | Type | Default | Label   | Description                                    |
|------|------|---------|---------|------------------------------------------------|
| 7:0  | R    | TBD     | revcode | This register contains the revision of the IC. |

### 3.1.7 Built In Self-Test (BIST) Receiver Main Control Register

**Table 3-8. Built In Self-Test (BIST) Receiver Main Control Register (BISTrx\_ctrl: Address 11h)**

| Bits | Type | Default | Label         | Description                                                                                                                                                                                                                                                                                                                                                                                             |
|------|------|---------|---------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7    | R/W  | 0b      | RSVD internal | N/A                                                                                                                                                                                                                                                                                                                                                                                                     |
| 6    | R/W  | 0b      | rx_ctrlr      | Clear the BIST Rx error count register, <i>BISTrx_error</i> (active when <i>BISTrx_ctrl</i> [1] = 1).<br>0b: Normal operation<br>1b: Clear register                                                                                                                                                                                                                                                     |
| 5:2  | R/W  | 0000b   | rx_patt       | Selects the BIST Rx test pattern (active when <i>BISTrx_ctrl</i> [1] = 1).<br>0000b: PRBS 2 <sup>7</sup> -1<br>0001b: PRBS 2 <sup>15</sup> -1<br>0010b: PRBS 2 <sup>23</sup> -1<br>0011b: PRBS 2 <sup>31</sup> -1<br>0100b: Fibre channel CJTPAT<br>0101b: Fibre channel CRPAT<br>0110b: 8b/10b countdown pattern<br>0111b: 16 bit user programmable pattern<br>1000b: 20 bit user programmable pattern |
| 1    | R/W  | 0b      | en_rx         | Powers up the BIST Rx.<br>0b: Power down<br>1b: Power up and enable                                                                                                                                                                                                                                                                                                                                     |
| 0    | R/W  | 1b      | rx_rst        | Resets the BIST Rx (recommended after powerup/enable, active when <i>BISTrx_ctrl</i> [1] = 1).<br>0b: Normal BIST Rx operation<br>1b: Reset of BIST Rx                                                                                                                                                                                                                                                  |

### 3.1.8 Built In Self-Test (BIST) Receiver Bit Error Counter

**Table 3-9. Built In Self-Test (BIST) Receiver Bit Error Counter (BISTrx\_error: Address 12h)**

| Bits | Type | Default | Label | Description                                                                                                                                                                                                                              |
|------|------|---------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:0  | R/W  | 00h     | err   | Bit error count (active when <i>BISTrx_ctrl</i> [1] = 1).<br>This register is set to 00h upon reset, and is incremented for every bit error the BIST Rx receives, up to FFh. At FFh, the register will stay at this level until cleared. |

### 3.1.9 Built In Self-Test (BIST) Transmitter Channel Select

**Table 3-10. Built In Self-Test (BIST) Transmitter Channel Select (BISTtx\_chsel: Address 14h)**

| Bits | Type | Default | Label    | Description                                                                                                                                                                                                                                                                                                                                                               |
|------|------|---------|----------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:4  | R/W  | 0000b   | Reserved | N/A                                                                                                                                                                                                                                                                                                                                                                       |
| 3:0  | R/W  | 0000b   | tx_chan  | <p>Selects which input channel the BIST Tx outputs the test pattern on (active when <i>BISTtx_ctrl</i> [1] = 1).</p> <p>Bit map: 1b = BIST Tx on, 0b = BIST Tx off</p> <p>[3]: N/A, set to '0'</p> <p>[2]: N/A, set to '0'</p> <p>[1]: Input channel 1</p> <p>[0]: Input channel 0</p> <p><b>NOTE:</b> Registers are set up to allow for multicasting BIST Tx output.</p> |

### 3.1.10 Built In Self-Test (BIST) Transmitter Main Control Register

**Table 3-11. Built In Self-Test (BIST) Transmitter Main Control Register (BISTtx\_ctrl: Address 15h)**

| Bits | Type | Default | Label      | Description                                                                                                                                                                                                                                                                                                                                                                                                               |
|------|------|---------|------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7    | R/W  | 0b      | err_insert | <p>Inserts a single bit error into the PRBS Tx.</p> <p>0b: Normal operation<br/>1b: Insert error</p> <p><b>NOTE:</b> Setting the register high allows one error to be inserted into the data stream. To insert another error, the user needs to clear, then set this register bit.</p>                                                                                                                                    |
| 6    | R/W  | 0b      | rx2txclk   | <p>Selects the source of the clock for the BIST Tx PLL (active when <i>BISTtx_ctrl</i> [1] = 1).</p> <p>0b: External reference frequency<br/>1b: Recovered clock from BIST Rx</p> <p><b>NOTE:</b> For the recovered clock option, the BIST Rx must be enabled with <i>BISTrx_ctrl</i> [1] = 1, and use the recovered clock from the same CDR/RCLK selected by BIST Rx. This option only works for the full-rate case.</p> |
| 5:2  | R/W  | 0000b   | tx_patt    | <p>Selects the BIST Tx test pattern (active when <i>BISTtx_ctrl</i> [1] = 1).</p> <p>0000b: PRBS 2<sup>7</sup>-1<br/>0001b: PRBS 2<sup>15</sup>-1<br/>0010b: PRBS 2<sup>23</sup>-1<br/>0011b: PRBS 2<sup>31</sup>-1<br/>0100b: Fibre channel CJTPAT<br/>0101b: Fibre channel CRPAT<br/>0110b: 8b/10b countdown pattern<br/>0111b: 16 bit user programmable pattern<br/>1000b: 20 bit user programmable pattern</p>        |
| 1    | R/W  | 0b      | en_tx      | <p>Powers up the BIST Tx and PLL.</p> <p>0b: Power down<br/>1b: Power up and enable</p>                                                                                                                                                                                                                                                                                                                                   |
| 0    | R/W  | 1b      | tx_rst     | <p>Resets the BIST Tx (recommended after powerup/enable; active when <i>BISTtx_ctrl</i> [1] = 1).</p> <p>0b: Normal BIST Tx operation<br/>1b: Reset of BIST Tx</p>                                                                                                                                                                                                                                                        |

### 3.1.11 Built In Self-Test (BIST) Transmitter PLL Loss of Lock Register

**Table 3-12. Built In Self-Test (BIST) Transmitter PLL Loss of Lock Register**  
(BISTtx\_LOLctrl: Address 17h) (1 of 2)

| Bits  | Type  | Default | Label      | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |      |       |       |     |       |     |       |     |       |      |       |      |       |      |       |      |       |       |       |   |       |    |       |    |       |    |       |    |       |    |       |    |       |    |
|-------|-------|---------|------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|-------|-------|-----|-------|-----|-------|-----|-------|------|-------|------|-------|------|-------|------|-------|-------|-------|---|-------|----|-------|----|-------|----|-------|----|-------|----|-------|----|-------|----|
| 7:5   | R/W   | 101b    | tacq_LOL   | <div>Sets the value for the LOL reference window.</div> <table><tr><th>Code</th><th>Value</th></tr><tr><td>000b</td><td>128</td></tr><tr><td>001b</td><td>256</td></tr><tr><td>010b</td><td>512</td></tr><tr><td>011b</td><td>1024</td></tr><tr><td>100b</td><td>2048</td></tr><tr><td>101b</td><td>4096</td></tr><tr><td>110b</td><td>8192</td></tr><tr><td>111b</td><td>16384</td></tr></table>                                                                                                                                                                                                                                                                                                                            | Code | Value | 000b  | 128 | 001b  | 256 | 010b  | 512 | 011b  | 1024 | 100b  | 2048 | 101b  | 4096 | 110b  | 8192 | 111b  | 16384 |       |   |       |    |       |    |       |    |       |    |       |    |       |    |       |    |
| Code  | Value |         |            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |      |       |       |     |       |     |       |     |       |      |       |      |       |      |       |      |       |       |       |   |       |    |       |    |       |    |       |    |       |    |       |    |       |    |
| 000b  | 128   |         |            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |      |       |       |     |       |     |       |     |       |      |       |      |       |      |       |      |       |       |       |   |       |    |       |    |       |    |       |    |       |    |       |    |       |    |
| 001b  | 256   |         |            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |      |       |       |     |       |     |       |     |       |      |       |      |       |      |       |      |       |       |       |   |       |    |       |    |       |    |       |    |       |    |       |    |       |    |
| 010b  | 512   |         |            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |      |       |       |     |       |     |       |     |       |      |       |      |       |      |       |      |       |       |       |   |       |    |       |    |       |    |       |    |       |    |       |    |       |    |
| 011b  | 1024  |         |            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |      |       |       |     |       |     |       |     |       |      |       |      |       |      |       |      |       |       |       |   |       |    |       |    |       |    |       |    |       |    |       |    |       |    |
| 100b  | 2048  |         |            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |      |       |       |     |       |     |       |     |       |      |       |      |       |      |       |      |       |       |       |   |       |    |       |    |       |    |       |    |       |    |       |    |       |    |
| 101b  | 4096  |         |            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |      |       |       |     |       |     |       |     |       |      |       |      |       |      |       |      |       |       |       |   |       |    |       |    |       |    |       |    |       |    |       |    |       |    |
| 110b  | 8192  |         |            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |      |       |       |     |       |     |       |     |       |      |       |      |       |      |       |      |       |       |       |   |       |    |       |    |       |    |       |    |       |    |       |    |       |    |
| 111b  | 16384 |         |            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |      |       |       |     |       |     |       |     |       |      |       |      |       |      |       |      |       |       |       |   |       |    |       |    |       |    |       |    |       |    |       |    |       |    |
| 4:1   | R/W   | 0011b   | narwin_LOL | <div>Sets the narrow LOL window for the LOL = H to LOL = L transition (transition to in lock threshold).</div> <table><tr><th>Code</th><th>Value</th></tr><tr><td>0000b</td><td>2</td></tr><tr><td>0001b</td><td>3</td></tr><tr><td>0010b</td><td>4</td></tr><tr><td>0011b</td><td>6</td></tr><tr><td>0100b</td><td>8</td></tr><tr><td>0101b</td><td>12</td></tr><tr><td>0110b</td><td>16</td></tr><tr><td>0111b</td><td>24</td></tr><tr><td>1000b</td><td>9</td></tr><tr><td>1001b</td><td>10</td></tr><tr><td>1010b</td><td>11</td></tr><tr><td>1011b</td><td>12</td></tr><tr><td>1100b</td><td>13</td></tr><tr><td>1101b</td><td>14</td></tr><tr><td>1110b</td><td>15</td></tr><tr><td>1111b</td><td>32</td></tr></table> | Code | Value | 0000b | 2   | 0001b | 3   | 0010b | 4   | 0011b | 6    | 0100b | 8    | 0101b | 12   | 0110b | 16   | 0111b | 24    | 1000b | 9 | 1001b | 10 | 1010b | 11 | 1011b | 12 | 1100b | 13 | 1101b | 14 | 1110b | 15 | 1111b | 32 |
| Code  | Value |         |            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |      |       |       |     |       |     |       |     |       |      |       |      |       |      |       |      |       |       |       |   |       |    |       |    |       |    |       |    |       |    |       |    |       |    |
| 0000b | 2     |         |            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |      |       |       |     |       |     |       |     |       |      |       |      |       |      |       |      |       |       |       |   |       |    |       |    |       |    |       |    |       |    |       |    |       |    |
| 0001b | 3     |         |            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |      |       |       |     |       |     |       |     |       |      |       |      |       |      |       |      |       |       |       |   |       |    |       |    |       |    |       |    |       |    |       |    |       |    |
| 0010b | 4     |         |            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |      |       |       |     |       |     |       |     |       |      |       |      |       |      |       |      |       |       |       |   |       |    |       |    |       |    |       |    |       |    |       |    |       |    |
| 0011b | 6     |         |            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |      |       |       |     |       |     |       |     |       |      |       |      |       |      |       |      |       |       |       |   |       |    |       |    |       |    |       |    |       |    |       |    |       |    |
| 0100b | 8     |         |            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |      |       |       |     |       |     |       |     |       |      |       |      |       |      |       |      |       |       |       |   |       |    |       |    |       |    |       |    |       |    |       |    |       |    |
| 0101b | 12    |         |            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |      |       |       |     |       |     |       |     |       |      |       |      |       |      |       |      |       |       |       |   |       |    |       |    |       |    |       |    |       |    |       |    |       |    |
| 0110b | 16    |         |            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |      |       |       |     |       |     |       |     |       |      |       |      |       |      |       |      |       |       |       |   |       |    |       |    |       |    |       |    |       |    |       |    |       |    |
| 0111b | 24    |         |            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |      |       |       |     |       |     |       |     |       |      |       |      |       |      |       |      |       |       |       |   |       |    |       |    |       |    |       |    |       |    |       |    |       |    |
| 1000b | 9     |         |            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |      |       |       |     |       |     |       |     |       |      |       |      |       |      |       |      |       |       |       |   |       |    |       |    |       |    |       |    |       |    |       |    |       |    |
| 1001b | 10    |         |            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |      |       |       |     |       |     |       |     |       |      |       |      |       |      |       |      |       |       |       |   |       |    |       |    |       |    |       |    |       |    |       |    |       |    |
| 1010b | 11    |         |            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |      |       |       |     |       |     |       |     |       |      |       |      |       |      |       |      |       |       |       |   |       |    |       |    |       |    |       |    |       |    |       |    |       |    |
| 1011b | 12    |         |            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |      |       |       |     |       |     |       |     |       |      |       |      |       |      |       |      |       |       |       |   |       |    |       |    |       |    |       |    |       |    |       |    |       |    |
| 1100b | 13    |         |            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |      |       |       |     |       |     |       |     |       |      |       |      |       |      |       |      |       |       |       |   |       |    |       |    |       |    |       |    |       |    |       |    |       |    |
| 1101b | 14    |         |            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |      |       |       |     |       |     |       |     |       |      |       |      |       |      |       |      |       |       |       |   |       |    |       |    |       |    |       |    |       |    |       |    |       |    |
| 1110b | 15    |         |            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |      |       |       |     |       |     |       |     |       |      |       |      |       |      |       |      |       |       |       |   |       |    |       |    |       |    |       |    |       |    |       |    |       |    |
| 1111b | 32    |         |            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |      |       |       |     |       |     |       |     |       |      |       |      |       |      |       |      |       |       |       |   |       |    |       |    |       |    |       |    |       |    |       |    |       |    |

**Table 3-12. Built In Self-Test (BIST) Transmitter PLL Loss of Lock Register**  
(BISTtx\_LOLctrl: Address 17h) (2 of 2)

| Bits                                                                            | Type         | Default      | Label      | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |             |              |              |       |   |   |       |   |    |       |   |    |       |   |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |
|---------------------------------------------------------------------------------|--------------|--------------|------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------|--------------|--------------|-------|---|---|-------|---|----|-------|---|----|-------|---|----|-------|----|----|-------|----|----|-------|----|----|-------|----|----|-------|----|----|-------|----|----|-------|----|----|-------|----|----|-------|----|----|-------|----|----|-------|----|----|-------|----|----|
| 0                                                                               | R/W          | 0b           | widwin_LOL | <p>Sets the wide LOL window for the LOL = L to LOL = H transition (transition to out of lock threshold).</p> <table><tr><th>Narrow Code</th><th>Wide Code 0b</th><th>Wide Code 1b</th></tr><tr><td>0000b</td><td>3</td><td>8</td></tr><tr><td>0001b</td><td>4</td><td>12</td></tr><tr><td>0010b</td><td>6</td><td>16</td></tr><tr><td>0011b</td><td>8</td><td>24</td></tr><tr><td>0100b</td><td>12</td><td>32</td></tr><tr><td>0101b</td><td>16</td><td>32</td></tr><tr><td>0110b</td><td>24</td><td>32</td></tr><tr><td>0111b</td><td>32</td><td>32</td></tr><tr><td>1000b</td><td>12</td><td>32</td></tr><tr><td>1001b</td><td>12</td><td>32</td></tr><tr><td>1010b</td><td>12</td><td>32</td></tr><tr><td>1011b</td><td>16</td><td>32</td></tr><tr><td>1100b</td><td>16</td><td>32</td></tr><tr><td>1101b</td><td>16</td><td>32</td></tr><tr><td>1110b</td><td>16</td><td>32</td></tr><tr><td>1111b</td><td>32</td><td>32</td></tr></table> | Narrow Code | Wide Code 0b | Wide Code 1b | 0000b | 3 | 8 | 0001b | 4 | 12 | 0010b | 6 | 16 | 0011b | 8 | 24 | 0100b | 12 | 32 | 0101b | 16 | 32 | 0110b | 24 | 32 | 0111b | 32 | 32 | 1000b | 12 | 32 | 1001b | 12 | 32 | 1010b | 12 | 32 | 1011b | 16 | 32 | 1100b | 16 | 32 | 1101b | 16 | 32 | 1110b | 16 | 32 | 1111b | 32 | 32 |
| Narrow Code                                                                     | Wide Code 0b | Wide Code 1b |            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |             |              |              |       |   |   |       |   |    |       |   |    |       |   |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |
| 0000b                                                                           | 3            | 8            |            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |             |              |              |       |   |   |       |   |    |       |   |    |       |   |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |
| 0001b                                                                           | 4            | 12           |            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |             |              |              |       |   |   |       |   |    |       |   |    |       |   |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |
| 0010b                                                                           | 6            | 16           |            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |             |              |              |       |   |   |       |   |    |       |   |    |       |   |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |
| 0011b                                                                           | 8            | 24           |            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |             |              |              |       |   |   |       |   |    |       |   |    |       |   |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |
| 0100b                                                                           | 12           | 32           |            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |             |              |              |       |   |   |       |   |    |       |   |    |       |   |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |
| 0101b                                                                           | 16           | 32           |            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |             |              |              |       |   |   |       |   |    |       |   |    |       |   |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |
| 0110b                                                                           | 24           | 32           |            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |             |              |              |       |   |   |       |   |    |       |   |    |       |   |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |
| 0111b                                                                           | 32           | 32           |            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |             |              |              |       |   |   |       |   |    |       |   |    |       |   |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |
| 1000b                                                                           | 12           | 32           |            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |             |              |              |       |   |   |       |   |    |       |   |    |       |   |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |
| 1001b                                                                           | 12           | 32           |            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |             |              |              |       |   |   |       |   |    |       |   |    |       |   |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |
| 1010b                                                                           | 12           | 32           |            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |             |              |              |       |   |   |       |   |    |       |   |    |       |   |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |
| 1011b                                                                           | 16           | 32           |            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |             |              |              |       |   |   |       |   |    |       |   |    |       |   |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |
| 1100b                                                                           | 16           | 32           |            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |             |              |              |       |   |   |       |   |    |       |   |    |       |   |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |
| 1101b                                                                           | 16           | 32           |            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |             |              |              |       |   |   |       |   |    |       |   |    |       |   |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |
| 1110b                                                                           | 16           | 32           |            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |             |              |              |       |   |   |       |   |    |       |   |    |       |   |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |
| 1111b                                                                           | 32           | 32           |            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |             |              |              |       |   |   |       |   |    |       |   |    |       |   |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |
| <b>NOTE:</b><br>Default value applies to reference based frequency acquisition. |              |              |            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |             |              |              |       |   |   |       |   |    |       |   |    |       |   |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |

### 3.1.12 Built In Self-Test (BIST) Transmitter PLL Control Register A

**Table 3-13. Built In Self-Test (BIST) Transmitter PLL Control Register A** (BISTtx\_PLL\_ctrlA: Address 18h)

| Bits | Type | Default | Label         | Description                                                                                                               |
|------|------|---------|---------------|---------------------------------------------------------------------------------------------------------------------------|
| 7    | R/W  | 0b      | softreset     | <p>Resets the BIST transmitter PLL (assuming BISTtx_ctrl[1] = 1b).</p> <p>0b: Normal operation<br/>1b: Reset PLL only</p> |
| 6    | R/W  | 0b      | RSVD internal | N/A                                                                                                                       |
| 5    | R/W  | 0b      | Reserved      | N/A                                                                                                                       |
| 4    | R/W  | 0b      | RSVD internal | N/A                                                                                                                       |
| 3    | R/W  | 0b      | Reserved      | N/A                                                                                                                       |
| 2    | R/W  | 1b      | RSVD internal | N/A                                                                                                                       |
| 1    | R/W  | 0b      | Reserved      | N/A                                                                                                                       |
| 0    | R/W  | 1b      | RSVD internal | N/A                                                                                                                       |

### 3.1.13 Built In Self-Test (BIST) Transmitter PLL Control Register B

**Table 3-14. Built In Self-Test (BIST) Transmitter PLL Control Register B (BISTtx\_PLL\_ctrlB: Address 19h)**

| Bits | Type | Default | Label         | Description                                                                                                                                                                                                                                                                                                                                                               |
|------|------|---------|---------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:6  | R/W  | 11b     | PLLmode       | Determines state of the PLL. Must be enabled in addition to the BIST Tx (BISTtx_ctrl[1] = 1b).<br>00b: Channel active, PLL powered up<br>11b: Channel active, PLL powered down                                                                                                                                                                                            |
| 5:4  | R/W  | 01b     | RSVD internal | N/A                                                                                                                                                                                                                                                                                                                                                                       |
| 3:0  | R/W  | 0000b   | data_rate     | Data rate divider (DRD): this divides down the VCO frequency to the desired data rate.<br>0000b = VCO/1<br>0001b = VCO/2<br>0010b = VCO/4<br>0011b = VCO/8<br>0100b = VCO/12<br>0101b = VCO/16<br>0110b = VCO/24<br>0111b = VCO/32<br>1000b = VCO/48<br><b>NOTE:</b> Please consult $F_{vco, max}$ and $F_{vco, min}$ to determine the frequency range of each DRD ratio. |

### 3.1.14 Built In Self-Test (BIST) Transmitter PLL Control Register C

**Table 3-15. Built In Self-Test (BIST) Transmitter PLL Control Register C (BISTtx\_PLL\_ctrlC: Address 1Ah)**

| Bits | Type | Default   | Label   | Description                                                                                                                                                                                                                               |
|------|------|-----------|---------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:0  | R/W  | 10000000b | VCO_div | VCO comparison divider (VCD): this divider divides down the VCO to compare it with the divided down reference.<br>Binary value reflects the divider ratio<br>01h: Minimum value (VCO /1)<br>.<br>.<br>.<br>FFh: Maximum value (VCO / 255) |

### 3.1.15 Built In Self-Test (BIST) Transmitter 20 bit User Programmable Pattern

**Table 3-16. Built In Self-Test (BIST) Transmitter 20 bit User Programmable Pattern**  
(BIST\_pattern0: Address 1Bh)

| Bits | Type | Default | Label   | Description                                                                                                                                                         |
|------|------|---------|---------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 3:0  | R/W  | 1100b   | pattern | Sets the 20 bit user programmable pattern used in the BIST.<br>[3] MSB : Pattern bit#19<br>[2] : Pattern bit#18<br>[1] : Pattern bit#17<br>[0] LSB : Pattern bit#16 |

### 3.1.16 Built In Self-Test (BIST) Transmitter 16/20 bit User Programmable Pattern

**Table 3-17. Built In Self-Test (BIST) Transmitter 16/20 bit User Programmable Pattern**  
(BIST\_pattern1: Address 1Ch)

| Bits | Type | Default   | Label   | Description                                                                                                                                                                                                                                                          |
|------|------|-----------|---------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:0  | R/W  | 11001100b | pattern | Sets the 16/20 bit user programmable pattern used in the BIST.<br>[7] MSB : Pattern bit#15<br>[6] : Pattern bit#14<br>[5] : Pattern bit#13<br>[4] : Pattern bit#12<br>[3] : Pattern bit#11<br>[2] : Pattern bit#10<br>[1] : Pattern bit#9<br>[0] LSB : Pattern bit#8 |

### 3.1.17 Built In Self-Test (BIST) Transmitter 16/20 bit User Programmable Pattern

**Table 3-18. Built In Self-Test (BIST) Transmitter 16/20 bit User Programmable Pattern**  
(BIST\_pattern2: Address 1Dh)

| Bits | Type | Default   | Label   | Description                                                                                                                                                                                                                                                    |
|------|------|-----------|---------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:0  | R/W  | 11001100b | pattern | Sets the 16/20 bit user programmable pattern used in the BIST.<br>[7] MSB : Pattern bit#7<br>[6] : Pattern bit#6<br>[5] : Pattern bit#5<br>[4] : Pattern bit#4<br>[3] : Pattern bit#3<br>[2] : Pattern bit#2<br>[1] : Pattern bit#1<br>[0] LSB : Pattern bit#0 |

### 3.1.18 Built In Self-Test (BIST) Transmitter Alarm

**Table 3-19. Built In Self-Test (BIST) Transmitter Alarm (BISTtx\_alarm: Address 1Fh)**

| Bits | Type | Default | Label         | Description                                                                                                            |
|------|------|---------|---------------|------------------------------------------------------------------------------------------------------------------------|
| 7    | R    | 0b      | tx_LOL        | Loss of lock for the BIST Tx PLL (active when <i>BISTtx_ctrl</i> [1] = 1).<br>0b: Normal operation<br>1b: Loss of lock |
| 6:5  | R/W  | 00b     | Reserved      | N/A                                                                                                                    |
| 4:0  | R/W  | 00000b  | RSVD internal | N/A                                                                                                                    |

### 3.1.19 Internal Junction Temperature Monitor

**Table 3-20. Internal Junction Temperature Monitor (Temp\_mon: Address 20h)**

| Bits | Type | Default | Label       | Description                                                                                                                                                                                                               |
|------|------|---------|-------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 3:2  | R/W  | 00b     | Reserved    | N/A                                                                                                                                                                                                                       |
| 1    | R/W  | 0b      | en_temp_mon | Power up and enable the temperature monitor.<br>0b: Disable temperature monitor<br>1b: Enable and power up temperature monitor                                                                                            |
| 0    | R/W  | 0b      | strobe_temp | Strobes ADC for temperature measurement.<br>0b: Ok to read temperature<br>1b: Read temperature<br><b>NOTE:</b> To strobe ADC, a rising edge should be provided by writing 1b, then writing 0b to return to default state. |

### 3.1.20 Internal Junction Temperature Value

**Table 3-21. Internal Junction Temperature Value (Temp\_value: Address 21h)**

| Bits               | Type  | Default      | Label | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |                  |      |           |            |       |            |                    |       |            |                    |       |              |                    |       |        |                   |       |        |                  |       |        |                  |       |        |                 |       |        |                  |       |        |                    |       |        |                    |       |             |                    |       |           |            |       |           |
|--------------------|-------|--------------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------|------|-----------|------------|-------|------------|--------------------|-------|------------|--------------------|-------|--------------|--------------------|-------|--------|-------------------|-------|--------|------------------|-------|--------|------------------|-------|--------|-----------------|-------|--------|------------------|-------|--------|--------------------|-------|--------|--------------------|-------|-------------|--------------------|-------|-----------|------------|-------|-----------|
| 3:0                | R     | N/A          | temp  | <div>A read of these bits returns the temperature from the last write cycle (to strobe_temp).</div> <table><tr><th>Case Temperature</th><th>Temp</th><th>Condition</th></tr><tr><td>Tc ≥ 130°C</td><td>1100b</td><td>High-alarm</td></tr><tr><td>130°C &gt; Tc ≥ 120°C</td><td>1011b</td><td>High-alarm</td></tr><tr><td>120°C &gt; Tc ≥ 110°C</td><td>1010b</td><td>High-warning</td></tr><tr><td>110°C &gt; Tc ≥ 100°C</td><td>1001b</td><td>Normal</td></tr><tr><td>100°C &gt; Tc ≥ 90°C</td><td>1000b</td><td>Normal</td></tr><tr><td>90°C &gt; Tc ≥ 80°C</td><td>0111b</td><td>Normal</td></tr><tr><td>80°C &gt; Tc ≥ 10°C</td><td>0110b</td><td>Normal</td></tr><tr><td>10°C &gt; Tc ≥ 0°C</td><td>0101b</td><td>Normal</td></tr><tr><td>0°C &gt; Tc ≥ -10°C</td><td>0100b</td><td>Normal</td></tr><tr><td>-10°C &gt; Tc ≥ -20°C</td><td>0011b</td><td>Normal</td></tr><tr><td>-20°C &gt; Tc ≥ -30°C</td><td>0010b</td><td>Low-warning</td></tr><tr><td>-30°C &gt; Tc ≥ -40°C</td><td>0001b</td><td>Low-alarm</td></tr><tr><td>-40°C &gt; Tc</td><td>0000b</td><td>Low-alarm</td></tr></table> | Case Temperature | Temp | Condition | Tc ≥ 130°C | 1100b | High-alarm | 130°C > Tc ≥ 120°C | 1011b | High-alarm | 120°C > Tc ≥ 110°C | 1010b | High-warning | 110°C > Tc ≥ 100°C | 1001b | Normal | 100°C > Tc ≥ 90°C | 1000b | Normal | 90°C > Tc ≥ 80°C | 0111b | Normal | 80°C > Tc ≥ 10°C | 0110b | Normal | 10°C > Tc ≥ 0°C | 0101b | Normal | 0°C > Tc ≥ -10°C | 0100b | Normal | -10°C > Tc ≥ -20°C | 0011b | Normal | -20°C > Tc ≥ -30°C | 0010b | Low-warning | -30°C > Tc ≥ -40°C | 0001b | Low-alarm | -40°C > Tc | 0000b | Low-alarm |
| Case Temperature   | Temp  | Condition    |       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |                  |      |           |            |       |            |                    |       |            |                    |       |              |                    |       |        |                   |       |        |                  |       |        |                  |       |        |                 |       |        |                  |       |        |                    |       |        |                    |       |             |                    |       |           |            |       |           |
| Tc ≥ 130°C         | 1100b | High-alarm   |       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |                  |      |           |            |       |            |                    |       |            |                    |       |              |                    |       |        |                   |       |        |                  |       |        |                  |       |        |                 |       |        |                  |       |        |                    |       |        |                    |       |             |                    |       |           |            |       |           |
| 130°C > Tc ≥ 120°C | 1011b | High-alarm   |       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |                  |      |           |            |       |            |                    |       |            |                    |       |              |                    |       |        |                   |       |        |                  |       |        |                  |       |        |                 |       |        |                  |       |        |                    |       |        |                    |       |             |                    |       |           |            |       |           |
| 120°C > Tc ≥ 110°C | 1010b | High-warning |       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |                  |      |           |            |       |            |                    |       |            |                    |       |              |                    |       |        |                   |       |        |                  |       |        |                  |       |        |                 |       |        |                  |       |        |                    |       |        |                    |       |             |                    |       |           |            |       |           |
| 110°C > Tc ≥ 100°C | 1001b | Normal       |       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |                  |      |           |            |       |            |                    |       |            |                    |       |              |                    |       |        |                   |       |        |                  |       |        |                  |       |        |                 |       |        |                  |       |        |                    |       |        |                    |       |             |                    |       |           |            |       |           |
| 100°C > Tc ≥ 90°C  | 1000b | Normal       |       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |                  |      |           |            |       |            |                    |       |            |                    |       |              |                    |       |        |                   |       |        |                  |       |        |                  |       |        |                 |       |        |                  |       |        |                    |       |        |                    |       |             |                    |       |           |            |       |           |
| 90°C > Tc ≥ 80°C   | 0111b | Normal       |       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |                  |      |           |            |       |            |                    |       |            |                    |       |              |                    |       |        |                   |       |        |                  |       |        |                  |       |        |                 |       |        |                  |       |        |                    |       |        |                    |       |             |                    |       |           |            |       |           |
| 80°C > Tc ≥ 10°C   | 0110b | Normal       |       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |                  |      |           |            |       |            |                    |       |            |                    |       |              |                    |       |        |                   |       |        |                  |       |        |                  |       |        |                 |       |        |                  |       |        |                    |       |        |                    |       |             |                    |       |           |            |       |           |
| 10°C > Tc ≥ 0°C    | 0101b | Normal       |       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |                  |      |           |            |       |            |                    |       |            |                    |       |              |                    |       |        |                   |       |        |                  |       |        |                  |       |        |                 |       |        |                  |       |        |                    |       |        |                    |       |             |                    |       |           |            |       |           |
| 0°C > Tc ≥ -10°C   | 0100b | Normal       |       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |                  |      |           |            |       |            |                    |       |            |                    |       |              |                    |       |        |                   |       |        |                  |       |        |                  |       |        |                 |       |        |                  |       |        |                    |       |        |                    |       |             |                    |       |           |            |       |           |
| -10°C > Tc ≥ -20°C | 0011b | Normal       |       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |                  |      |           |            |       |            |                    |       |            |                    |       |              |                    |       |        |                   |       |        |                  |       |        |                  |       |        |                 |       |        |                  |       |        |                    |       |        |                    |       |             |                    |       |           |            |       |           |
| -20°C > Tc ≥ -30°C | 0010b | Low-warning  |       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |                  |      |           |            |       |            |                    |       |            |                    |       |              |                    |       |        |                   |       |        |                  |       |        |                  |       |        |                 |       |        |                  |       |        |                    |       |        |                    |       |             |                    |       |           |            |       |           |
| -30°C > Tc ≥ -40°C | 0001b | Low-alarm    |       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |                  |      |           |            |       |            |                    |       |            |                    |       |              |                    |       |        |                   |       |        |                  |       |        |                  |       |        |                 |       |        |                  |       |        |                    |       |        |                    |       |             |                    |       |           |            |       |           |
| -40°C > Tc         | 0000b | Low-alarm    |       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |                  |      |           |            |       |            |                    |       |            |                    |       |              |                    |       |        |                   |       |        |                  |       |        |                  |       |        |                 |       |        |                  |       |        |                    |       |        |                    |       |             |                    |       |           |            |       |           |

### 3.1.21 CDR/RCLK Loss of Lock Register Alarm Status

**Table 3-22. CDR/RCLK Loss of Lock Register Alarm Status (Alarm\_LOL: Address 30h)**

| Bits | Type | Default  | Label         | Description                                                                                                                                                                                                                                                                                              |
|------|------|----------|---------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:1  | N/A  | 0000000b | RSVD internal | N/A                                                                                                                                                                                                                                                                                                      |
| 0    | R    | N/A      | LOL           | <p>Latched loss of lock alarm status.</p> <p>0b = normal operation<br/>1b = loss of CDR/RCLK lock</p> <p><b>NOTE:</b> After a clear (<i>Globctrl</i> [0] = 1), this register is cleared and will latch any new alarms that make a L to H transition, and set any pre-existing alarm conditions to H.</p> |

### 3.1.22 CDR/RCLK Loss of Activity Register Alarm Status

**Table 3-23. CDR/RCLK Loss of Activity Register Alarm Status (Alarm\_LOA: Address 31h)**

| Bits | Type | Default  | Label         | Description                                                                                                                                                                                                                                                      |
|------|------|----------|---------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:1  | N/A  | 0000000b | RSVD internal | N/A                                                                                                                                                                                                                                                              |
| 0    | R    | N/A      | LOL           | <p>0b = LOA alarm de-asserted<br/>1b = LOA alarm asserted</p> <p><b>NOTE:</b> After a clear (<i>Globctrl</i> [0] = 1), this register is cleared and will latch any new alarms that make a L to H transition, and set any pre-existing alarm conditions to H.</p> |

### 3.1.23 CDR/RCLK Control Register A

**Table 3-24. CDR/RCLK Control Register A (RCLK\_ctrlA: Address 40h)**

| Bits | Type | Default | Label         | Description                                                                                                                                                                                               |
|------|------|---------|---------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7    | R/W  | 0b      | softreset     | Resets individual CDR/RCLK (setup registers remain unchanged; need to softreset after rate change).<br>0b: Normal operation<br>1b: Reset single CDR/RCLK only                                             |
| 6    | R/W  | 0b      | RSVD internal | N/A                                                                                                                                                                                                       |
| 5    | R/W  | 0b      | inh_force     | Manual control of the output inhibit if RCLK_ctrlA [3] = 0.<br>0b: Normal operation<br>1b: Forced inhibit                                                                                                 |
| 4    | R/W  | 0b      | RSVD internal | N/A                                                                                                                                                                                                       |
| 3    | R/W  | 1b      | autoinh_en    | Auto inhibit of the output ( <b>DoutP</b> = H, <b>DoutN</b> = L) if CDR/RCLK has a LOL condition.<br>0b: Auto inhibit disabled, RCLK_ctrlA [5] determines inhibit force state<br>1b: Auto inhibit enabled |
| 2    | R/W  | 1b      | RSVD internal | N/A                                                                                                                                                                                                       |
| 1    | R/W  | 1b      | RSVD internal | N/A                                                                                                                                                                                                       |
| 0    | R/W  | 1b      | RSVD internal | N/A                                                                                                                                                                                                       |

### 3.1.24 CDR/RCLK Control Register B

**Table 3-25. CDR/RCLK Control Register B (RCLK\_ctrlB: Address 41h)**

| Bits | Type | Default | Label         | Description                                                                                                                                                                                                                                                                                                                                                                                            |
|------|------|---------|---------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:6  | R/W  | 00b     | RCLKmode      | Determines state of the PLL.<br>00b: CDR/RCLK powered up and active<br>01b: CDR/RCLK powered up and bypassed<br>10b: CDR/RCLK powered down (no signal through)<br>11b: CDR/RCLK powered down and bypassed                                                                                                                                                                                              |
| 5    | R/W  | 0b      | RSVD internal | N/A                                                                                                                                                                                                                                                                                                                                                                                                    |
| 4    | R/W  | 0b      | Reserved      | N/A                                                                                                                                                                                                                                                                                                                                                                                                    |
| 3:0  | R/W  | 0000b   | data_rate     | Data rate divider (DRD): this divides down the VCO frequency to the desired data rate to match input data rate.<br><br>0000b = VCO/1<br>0001b = VCO/2<br>0010b = VCO/4<br>0011b = VCO/8<br>0100b = VCO/12<br>0101b = VCO/16<br>0110b = VCO/24<br>0111b = VCO/32<br>1000b = VCO/48<br><br><b>NOTE:</b> Please consult $F_{vco, max}$ and $F_{vco, min}$ to determine frequency range of each DRD ratio. |

### 3.1.25 CDR/RCLK Control Register C

**Table 3-26. CDR/RCLK N Control Register C (RCLK\_ctrlC: Address 42h)**

| Bits | Type | Default   | Label    | Description                                                                                                                                                                                                                         |
|------|------|-----------|----------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:0  | R/W  | 10000000b | VCO_divr | VCO comparison divider (VCD): this divides down the VCO, to compare it with the scaled reference clock.<br>Binary value reflects the divider ratio.<br>1h: Minimum value (VCO / 1)<br>.<br>.<br>.<br>FFh: Maximum value (VCO / 255) |

### 3.1.26 Output Buffer Control for CDR/RCLK

**Table 3-27. Output Buffer Control for CDR/RCLK (Out\_ctrl: Address 43h)**

| Bits | Type | Default | Label         | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
|------|------|---------|---------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:6  | R/W  | 10b     | outlvl        | <p>Determines the output swing of a data buffer for CDR/RCLK.</p> <p>In PCML mode:</p> <p>00b: Power down<br/> 01b: 500 mV<br/> 10b: 900 mV<br/> 11b: 1200 mV</p> <p>For LVDS, the output swing is reduced to:</p> <p>00b: Power down<br/> 01b: RRL 390 mV<br/> 10b: GPL 700 mV<br/> 11b: 940 mV</p> <p>For LVPECL, the output swing is increased to:</p> <p>00b: Power down<br/> 01b: 900 mV<br/> 10b: Standard (low specification side) 1200 mV<br/> 11b: Standard (nominal) 1600 mV</p> <p>For InfiniBand, the output swing is increased to:</p> <p>00b: Power down<br/> 01b: 900 mV<br/> 10b: 1200 mV<br/> 11b: Standard (nominal) 1400 mV</p> |
| 5:4  | R/W  | 00b     | Reserved      | N/A                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| 3    | R/W  | 0b      | data_pol_flip | <p>Flips the polarity of the output data.</p> <p>0b: Normal<br/> 1b: Polarity flip</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| 2    | R/W  | 1b      | dataout_en    | <p>Enables the data output driver.</p> <p>0b: Data output disabled and powered down<br/> 1b: Data output enabled to level specified in Out_ctrl [7:6]</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| 1:0  | R/W  | 00b     | RSVD internal | N/A                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |

### 3.1.27 Output Buffer Pre-Emphasis Control for Output

**Table 3-28. Output Buffer Pre-Emphasis Control for Output (Preemp\_ctrl: Address 44h)**

| Bits | Type | Default | Label         | Description                                                                                                                                               |
|------|------|---------|---------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7    | R/W  | 0b      | Reserved      | Default = 0b                                                                                                                                              |
| 6:3  | R/W  | 1000b   | RSVD Internal | N/A                                                                                                                                                       |
| 2:0  | R/W  | 000b    | preemph       | Selects the pre-emphasis level.<br>000b: Pre-emphasis off<br>001b: 25%<br>010b: 37.5%<br>011b: 50%<br>100b: 75%<br>101b: 100%<br>110b: 150%<br>111b: 200% |

### 3.1.28 Input Equalization Control for Output

**Table 3-29. Input Equalization Control for Output (Ineq\_ctrl: Address 45h)**

| Bits | Type | Default | Label         | Description                                                                                                                                                                                                                                                                                                                                                                                    |
|------|------|---------|---------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7    | R/W  | 0b      | Reserved      | N/A                                                                                                                                                                                                                                                                                                                                                                                            |
| 6:5  | R/W  | 00b     | RSVD internal | N/A                                                                                                                                                                                                                                                                                                                                                                                            |
| 4    | R/W  | 0b      | en_DCservo    | Enables DC servo in the input channel to remove offset based deterministic jitter.<br>0b: DC servo $D_j$ attenuator off<br>1b: DC servo $D_j$ attenuator on                                                                                                                                                                                                                                    |
| 3    | R/W  | 0b      | RSVD internal | N/A                                                                                                                                                                                                                                                                                                                                                                                            |
| 2:0  | R/W  | 100b    | in_eq         | Selects the input equalization level.<br>000b: Input equalization disabled<br>001b: Minimum input equalization level<br>.<br>.<br>.<br>100b: Nominal input equalization level<br>.<br>.<br>.<br>111b: Maximum input equalization level<br><b>NOTE:</b> The 100b setting is optimized for PCB trace lengths between 10–46 inches, although other settings may be optimal for some applications. |

### 3.1.29 CDR/RCLK Loop Bandwidth and Data Sampling Point Adjust

**Table 3-30. CDR/RCLK Loop Bandwidth and Data Sampling Point Adjust (Phadj\_ctrl: Address 46h)**

| Bits | Type | Default | Label     | Description                                                                                                                                                                                                                                                                                                                                                                 |
|------|------|---------|-----------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:6  | R/W  | 10b     | i_trim    | Adjusts the charge-pump current; the loop bandwidth ( $F_{LBW}$ ) scales proportionately.<br>00b: 0.65x<br>01b: 0.8x<br>10b: Nominal<br>11b: 1.15x                                                                                                                                                                                                                          |
| 5:4  | R/W  | 01b     | r_sel     | Adjusts the resistor of the CDR/RCLK loop filter; the loop bandwidth ( $F_{LBW}$ ) scales proportionately.<br>00b: 80% of the nominal value<br>01b: Nominal<br>10b: 4x nominal value<br>11b: 6x nominal value                                                                                                                                                               |
| 3:0  | R/W  | 0000b   | phase_adj | Adjusts the static phase offset (sampling point) of the data.<br>1111b: -122.5 mUI<br>1110b: -105 mUI<br>1101b: 87.5 mUI<br>1100b: -70 mUI<br>1011b: -52.5 mUI<br>1010b: -35.0 mUI<br>1001b: -17.5 mUI<br>1000b: 0 mUI<br>0000b: 0 mUI<br>0001b: 17.5 mUI<br>0010b: 35.0 mUI<br>0011b: 52.5 mUI<br>0100b: 70.0 mUI<br>0101b: 87.5 mUI<br>0110b: 105 mUI<br>0111b: 122.5 mUI |

### 3.1.30 CDR/RCLK LOL Window Control

**Table 3-31. CDR/RCLK LOL Window Control (LOL\_ctrl: Address 49h) (1 of 2)**

| Bits  | Type  | Default | Label      | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |      |       |       |     |       |     |       |     |       |      |       |      |       |      |       |      |       |       |       |   |       |    |       |    |       |    |       |    |       |    |       |    |       |    |
|-------|-------|---------|------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|-------|-------|-----|-------|-----|-------|-----|-------|------|-------|------|-------|------|-------|------|-------|-------|-------|---|-------|----|-------|----|-------|----|-------|----|-------|----|-------|----|-------|----|
| 7:5   | R/W   | 101b    | tacq_LOL   | Sets the value for the LOL reference window.<br><table><tr><th>Code</th><th>Value</th></tr><tr><td>000b</td><td>128</td></tr><tr><td>001b</td><td>256</td></tr><tr><td>010b</td><td>512</td></tr><tr><td>011b</td><td>1024</td></tr><tr><td>100b</td><td>2048</td></tr><tr><td>101b</td><td>4096</td></tr><tr><td>110b</td><td>8192</td></tr><tr><td>111b</td><td>16384</td></tr></table>                                                                                                                                                                                                                                                                                                                            | Code | Value | 000b  | 128 | 001b  | 256 | 010b  | 512 | 011b  | 1024 | 100b  | 2048 | 101b  | 4096 | 110b  | 8192 | 111b  | 16384 |       |   |       |    |       |    |       |    |       |    |       |    |       |    |       |    |
| Code  | Value |         |            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |      |       |       |     |       |     |       |     |       |      |       |      |       |      |       |      |       |       |       |   |       |    |       |    |       |    |       |    |       |    |       |    |       |    |
| 000b  | 128   |         |            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |      |       |       |     |       |     |       |     |       |      |       |      |       |      |       |      |       |       |       |   |       |    |       |    |       |    |       |    |       |    |       |    |       |    |
| 001b  | 256   |         |            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |      |       |       |     |       |     |       |     |       |      |       |      |       |      |       |      |       |       |       |   |       |    |       |    |       |    |       |    |       |    |       |    |       |    |
| 010b  | 512   |         |            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |      |       |       |     |       |     |       |     |       |      |       |      |       |      |       |      |       |       |       |   |       |    |       |    |       |    |       |    |       |    |       |    |       |    |
| 011b  | 1024  |         |            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |      |       |       |     |       |     |       |     |       |      |       |      |       |      |       |      |       |       |       |   |       |    |       |    |       |    |       |    |       |    |       |    |       |    |
| 100b  | 2048  |         |            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |      |       |       |     |       |     |       |     |       |      |       |      |       |      |       |      |       |       |       |   |       |    |       |    |       |    |       |    |       |    |       |    |       |    |
| 101b  | 4096  |         |            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |      |       |       |     |       |     |       |     |       |      |       |      |       |      |       |      |       |       |       |   |       |    |       |    |       |    |       |    |       |    |       |    |       |    |
| 110b  | 8192  |         |            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |      |       |       |     |       |     |       |     |       |      |       |      |       |      |       |      |       |       |       |   |       |    |       |    |       |    |       |    |       |    |       |    |       |    |
| 111b  | 16384 |         |            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |      |       |       |     |       |     |       |     |       |      |       |      |       |      |       |      |       |       |       |   |       |    |       |    |       |    |       |    |       |    |       |    |       |    |
| 4:1   | R/W   | 0011b   | narwin_LOL | Sets the narrow LOL window for the LOL = H to LOL = L transition (transition to in lock threshold).<br><table><tr><th>Code</th><th>Value</th></tr><tr><td>0000b</td><td>2</td></tr><tr><td>0001b</td><td>3</td></tr><tr><td>0010b</td><td>4</td></tr><tr><td>0011b</td><td>6</td></tr><tr><td>0100b</td><td>8</td></tr><tr><td>0101b</td><td>12</td></tr><tr><td>0110b</td><td>16</td></tr><tr><td>0111b</td><td>24</td></tr><tr><td>1000b</td><td>9</td></tr><tr><td>1001b</td><td>10</td></tr><tr><td>1010b</td><td>11</td></tr><tr><td>1011b</td><td>12</td></tr><tr><td>1100b</td><td>13</td></tr><tr><td>1101b</td><td>14</td></tr><tr><td>1110b</td><td>15</td></tr><tr><td>1111b</td><td>32</td></tr></table> | Code | Value | 0000b | 2   | 0001b | 3   | 0010b | 4   | 0011b | 6    | 0100b | 8    | 0101b | 12   | 0110b | 16   | 0111b | 24    | 1000b | 9 | 1001b | 10 | 1010b | 11 | 1011b | 12 | 1100b | 13 | 1101b | 14 | 1110b | 15 | 1111b | 32 |
| Code  | Value |         |            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |      |       |       |     |       |     |       |     |       |      |       |      |       |      |       |      |       |       |       |   |       |    |       |    |       |    |       |    |       |    |       |    |       |    |
| 0000b | 2     |         |            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |      |       |       |     |       |     |       |     |       |      |       |      |       |      |       |      |       |       |       |   |       |    |       |    |       |    |       |    |       |    |       |    |       |    |
| 0001b | 3     |         |            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |      |       |       |     |       |     |       |     |       |      |       |      |       |      |       |      |       |       |       |   |       |    |       |    |       |    |       |    |       |    |       |    |       |    |
| 0010b | 4     |         |            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |      |       |       |     |       |     |       |     |       |      |       |      |       |      |       |      |       |       |       |   |       |    |       |    |       |    |       |    |       |    |       |    |       |    |
| 0011b | 6     |         |            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |      |       |       |     |       |     |       |     |       |      |       |      |       |      |       |      |       |       |       |   |       |    |       |    |       |    |       |    |       |    |       |    |       |    |
| 0100b | 8     |         |            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |      |       |       |     |       |     |       |     |       |      |       |      |       |      |       |      |       |       |       |   |       |    |       |    |       |    |       |    |       |    |       |    |       |    |
| 0101b | 12    |         |            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |      |       |       |     |       |     |       |     |       |      |       |      |       |      |       |      |       |       |       |   |       |    |       |    |       |    |       |    |       |    |       |    |       |    |
| 0110b | 16    |         |            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |      |       |       |     |       |     |       |     |       |      |       |      |       |      |       |      |       |       |       |   |       |    |       |    |       |    |       |    |       |    |       |    |       |    |
| 0111b | 24    |         |            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |      |       |       |     |       |     |       |     |       |      |       |      |       |      |       |      |       |       |       |   |       |    |       |    |       |    |       |    |       |    |       |    |       |    |
| 1000b | 9     |         |            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |      |       |       |     |       |     |       |     |       |      |       |      |       |      |       |      |       |       |       |   |       |    |       |    |       |    |       |    |       |    |       |    |       |    |
| 1001b | 10    |         |            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |      |       |       |     |       |     |       |     |       |      |       |      |       |      |       |      |       |       |       |   |       |    |       |    |       |    |       |    |       |    |       |    |       |    |
| 1010b | 11    |         |            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |      |       |       |     |       |     |       |     |       |      |       |      |       |      |       |      |       |       |       |   |       |    |       |    |       |    |       |    |       |    |       |    |       |    |
| 1011b | 12    |         |            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |      |       |       |     |       |     |       |     |       |      |       |      |       |      |       |      |       |       |       |   |       |    |       |    |       |    |       |    |       |    |       |    |       |    |
| 1100b | 13    |         |            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |      |       |       |     |       |     |       |     |       |      |       |      |       |      |       |      |       |       |       |   |       |    |       |    |       |    |       |    |       |    |       |    |       |    |
| 1101b | 14    |         |            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |      |       |       |     |       |     |       |     |       |      |       |      |       |      |       |      |       |       |       |   |       |    |       |    |       |    |       |    |       |    |       |    |       |    |
| 1110b | 15    |         |            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |      |       |       |     |       |     |       |     |       |      |       |      |       |      |       |      |       |       |       |   |       |    |       |    |       |    |       |    |       |    |       |    |       |    |
| 1111b | 32    |         |            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |      |       |       |     |       |     |       |     |       |      |       |      |       |      |       |      |       |       |       |   |       |    |       |    |       |    |       |    |       |    |       |    |       |    |

Table 3-31. CDR/RCLK LOL Window Control (LOL\_ctrl: Address 49h) (2 of 2)

| Bits        | Type         | Default      | Label      | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |             |              |              |       |   |   |       |   |    |       |   |    |       |   |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |
|-------------|--------------|--------------|------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------|--------------|--------------|-------|---|---|-------|---|----|-------|---|----|-------|---|----|-------|----|----|-------|----|----|-------|----|----|-------|----|----|-------|----|----|-------|----|----|-------|----|----|-------|----|----|-------|----|----|-------|----|----|-------|----|----|-------|----|----|
| 0           | R/W          | 0b           | widwin_LOL | Sets the wide LOL window for the LOL = L to LOL = H transition (transition to out of lock threshold).                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |             |              |              |       |   |   |       |   |    |       |   |    |       |   |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |
|             |              |              |            | <table><tr><th>Narrow Code</th><th>Wide Code 0b</th><th>Wide Code 1b</th></tr><tr><td>0000b</td><td>3</td><td>8</td></tr><tr><td>0001b</td><td>4</td><td>12</td></tr><tr><td>0010b</td><td>6</td><td>16</td></tr><tr><td>0011b</td><td>8</td><td>24</td></tr><tr><td>0100b</td><td>12</td><td>32</td></tr><tr><td>0101b</td><td>16</td><td>32</td></tr><tr><td>0110b</td><td>24</td><td>32</td></tr><tr><td>0111b</td><td>32</td><td>32</td></tr><tr><td>1000b</td><td>12</td><td>32</td></tr><tr><td>1001b</td><td>12</td><td>32</td></tr><tr><td>1010b</td><td>12</td><td>32</td></tr><tr><td>1011b</td><td>16</td><td>32</td></tr><tr><td>1100b</td><td>16</td><td>32</td></tr><tr><td>1101b</td><td>16</td><td>32</td></tr><tr><td>1110b</td><td>16</td><td>32</td></tr><tr><td>1111b</td><td>32</td><td>32</td></tr></table> | Narrow Code | Wide Code 0b | Wide Code 1b | 0000b | 3 | 8 | 0001b | 4 | 12 | 0010b | 6 | 16 | 0011b | 8 | 24 | 0100b | 12 | 32 | 0101b | 16 | 32 | 0110b | 24 | 32 | 0111b | 32 | 32 | 1000b | 12 | 32 | 1001b | 12 | 32 | 1010b | 12 | 32 | 1011b | 16 | 32 | 1100b | 16 | 32 | 1101b | 16 | 32 | 1110b | 16 | 32 | 1111b | 32 | 32 |
| Narrow Code | Wide Code 0b | Wide Code 1b |            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |             |              |              |       |   |   |       |   |    |       |   |    |       |   |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |
| 0000b       | 3            | 8            |            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |             |              |              |       |   |   |       |   |    |       |   |    |       |   |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |
| 0001b       | 4            | 12           |            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |             |              |              |       |   |   |       |   |    |       |   |    |       |   |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |
| 0010b       | 6            | 16           |            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |             |              |              |       |   |   |       |   |    |       |   |    |       |   |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |
| 0011b       | 8            | 24           |            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |             |              |              |       |   |   |       |   |    |       |   |    |       |   |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |
| 0100b       | 12           | 32           |            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |             |              |              |       |   |   |       |   |    |       |   |    |       |   |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |
| 0101b       | 16           | 32           |            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |             |              |              |       |   |   |       |   |    |       |   |    |       |   |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |
| 0110b       | 24           | 32           |            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |             |              |              |       |   |   |       |   |    |       |   |    |       |   |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |
| 0111b       | 32           | 32           |            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |             |              |              |       |   |   |       |   |    |       |   |    |       |   |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |
| 1000b       | 12           | 32           |            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |             |              |              |       |   |   |       |   |    |       |   |    |       |   |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |
| 1001b       | 12           | 32           |            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |             |              |              |       |   |   |       |   |    |       |   |    |       |   |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |
| 1010b       | 12           | 32           |            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |             |              |              |       |   |   |       |   |    |       |   |    |       |   |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |
| 1011b       | 16           | 32           |            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |             |              |              |       |   |   |       |   |    |       |   |    |       |   |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |
| 1100b       | 16           | 32           |            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |             |              |              |       |   |   |       |   |    |       |   |    |       |   |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |
| 1101b       | 16           | 32           |            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |             |              |              |       |   |   |       |   |    |       |   |    |       |   |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |
| 1110b       | 16           | 32           |            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |             |              |              |       |   |   |       |   |    |       |   |    |       |   |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |
| 1111b       | 32           | 32           |            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |             |              |              |       |   |   |       |   |    |       |   |    |       |   |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |

### 3.1.31 Jitter Reduction Control

Table 3-32. Jitter Reduction Control (Jitter\_reduc: Address 4Ah)

| Bits | Type | Default | Label         | Description                                                                                                                                                                                                                                                                                                 |
|------|------|---------|---------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:6  | R/W  | 01b     | RSVD internal | N/A                                                                                                                                                                                                                                                                                                         |
| 5    | R/W  | 0b      | lowjitter     | <p>When data rate is in the range (2.45 Gbps–2.55 Gbps)/DRD, setting this bit to 1b will reduce output jitter (DRD is data rate divider).</p> <p>0b: Normal operation<br/>1b: Reduce output jitter</p> <p><b>NOTE:</b> This bit should be set to 1b for SONET STS-N, and Gigabit Ethernet applications.</p> |
| 4:0  | R/W  |         | RSVD internal | Any value may be written to this register with no effect on performance.                                                                                                                                                                                                                                    |

# Appendix

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## A.1 Glossary of Terms/Acronyms

|        |                                 |
|--------|---------------------------------|
| BER    | Bit Error Rate                  |
| BIST   | Built-In Self Test              |
| RCLK   | Reclocker                       |
| DRD    | Data Rate Divider               |
| EVM    | Evaluation Module               |
| FLL    | Frequency Lock Loop             |
| FRA    | Frequency Reference Acquisition |
| ISI    | Inter Symbol Interference       |
| LOA    | Loss of Activity                |
| LOL    | Loss of Lock                    |
| LOLCir | Loss of Lock Circuitry          |
| MLF    | Micro Lead Frame                |
| NRW    | Narrow Reference Window         |
| PCB    | Printed Circuit Board           |
| PLL    | Phase Lock Loop                 |
| RFD    | Reference Frequency Divider     |
| SONET  | Synchronous Optical Network     |
| VCD    | VCO Comparison Divider          |
| WRW    | Wide Reference Window           |
| XPTS   | Crosspoint Switch               |

## A.2 Reference Documents

### A.2.1 External

The following external documents were referenced in this data sheet.

- Synchronous Optical Network (SONET) Transport Systems: Common Generic Criteria GR-253-CORE
- The I<sup>2</sup>C Bus Specification version 2.1
- InfiniBand Architecture Specification Volume 2 Release 1.1
- Serial ATA: High Speed Serialized AT Attachment revision 1.0a
- Fibre Channel—Methodologies for Jitter and Signal Quality Specification—MJSQ
- Application Notes for Surface Mount Assembly of Amkor's Micro Lead Frame (MLF) Packages
- Amkor Technology Thermal Test Report TT-00-06
- SMPTE 292M, SMPTE 259M, SMPTE 344M
- DVB-ASI

### A.2.2 MACOM

The following MACOM documents were referenced in this data sheet.

- Application Note: Equipment Protection Switching Using Low-Cost Crosspoint Elements
- M2125x and M2126x ARD Software Description (212xx-SWG-001)
- Jitter tolerance and generation of MACOM crosspoint switches and CDR arrays (2110x-APP-003)

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