

Vishay Siliconix

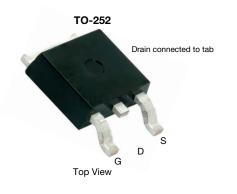
RoHS

COMPLIANT HALOGEN

FREE

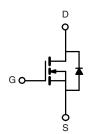
Automotive N-Channel 60 V (D-S) 175 °C MOSFET

PRODUCT SUMMARY ^d				
V _{DS} (V)	60			
$R_{DS(on)} (\Omega)$ at $V_{GS} = 10 V$	0.042			
$R_{DS(on)} (\Omega)$ at $V_{GS} = 4.5 V$	0.060			
I _D (A)	15			
Configuration	Single			
Package	TO-252			



FEATURES

- TrenchFET[®] power MOSFET
- 100 % R_g and UIS tested
- AEC-Q101 qualified
- Package with low thermal resistance
- Material categorization: for definitions of compliance please see <u>www.vishay.com/doc?99912</u>



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ($T_C = 25 \text{ °C}$, unless otherwise noted)				
PARAMETER		SYMBOL	LIMIT	UNIT
Drain-Source Voltage		V _{DS}	60	- V
Gate-Source Voltage	Gate-Source Voltage		± 20	v
Continuous Drain Current	T _C = 25 °C ^a	– I _D –	15	
Continuous Drain Current	T _C = 125 °C		10	
Continuous Source Current (Diode Conduction) ^a		I _S	15	А
Pulsed Drain Current ^b		I _{DM}	50	
Single Pulse Avalanche Current		I _{AS}	18	
Single Pulse Avalanche Energy		E _{AS}	16.2	mJ
Maximum Power Dissipation ^b	T _C = 25 °C	- P _D	37	W
Maximum Fower Dissipation -	T _C = 125 °C		11	~~~
Operating Junction and Storage Temperature Range		T _J , T _{stg}	-55 to +175	°C

THERMAL RESISTANCE RATINGS				
PARAMETER		SYMBOL	LIMIT	UNIT
Junction-to-Ambient PCB Mount ^c		R _{thJA}	50	°C/W
Junction-to-Case (Drain)		R _{thJC}	4	0/10

Notes

a. Package limited.

b. Pulse test; pulse width \leq 300 µs, duty cycle \leq 2 %.

c. When mounted on 1" square PCB (FR4 material).



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PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT	
Static								
Drain-Source Breakdown Voltage	V _{DS}	$V_{GS} = 0 V, I_D = 250 \mu A$		60	-	-		
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} =	V _{GS} , I _D = 250 μA	1.5	2	2.5	V	
Gate-Source Leakage	I _{GSS}	V _{DS} =	0 V, $V_{GS} = \pm 20 V$	-	-	± 100	nA	
		$V_{GS} = 0 V$	V _{DS} = 60 V	-	-	1		
Zero Gate Voltage Drain Current	I _{DSS}	$V_{GS} = 0 V$	V _{DS} = 60 V, T _J = 125 °C	-	-	50	μA	
		$V_{GS} = 0 V$	V _{DS} = 60 V, T _J = 175 °C	-	-	150		
On-State Drain Current ^a	I _{D(on)}	V _{GS} = 10 V	$V_{DS} \ge 5 V$	30	-	-	Α	
		V _{GS} = 10 V	I _D = 10 A	-	0.036	0.042		
		$V_{GS} = 10 V$	I _D = 10 A, T _J = 125 °C	-	-	0.075		
		V _{GS} = 10 V	I _D = 10 A, T _J = 175 °C	-	-	0.090		
Drain-Source On-State Resistance ^a	R _{DS(on)}	$V_{GS} = 4.5 V$	I _D = 10 A, T _J = 125 °C	-	0.092	-	Ω	
		$V_{GS} = 4.5 V$	I _D = 10 A, T _J = 175 °C	-	0.110	-		
		V _{GS} = 4.5 V	I _D = 10 A	-	0.048	0.060	-	
Forward Transconductance b	9 _{fs}	V _{DS}	= 15 V, I _D = 6 A	-	11	-	S	
Dynamic ^b	-	-						
Input Capacitance	C _{iss}			-	425	535		
Output Capacitance	C _{oss}	$V_{GS} = 0 V$	V _{DS} = 25 V, f = 1 MHz	-	95	120	pF	
Reverse Transfer Capacitance	C _{rss}			-	40	50		
Total Gate Charge ^c	Qg			-	9.5	15		
Gate-Source Charge ^c	Q _{gs}	V _{GS} = 10 V	V _{DS} = 30 V, I _D = 15 A	-	1.7	-	nC	
Gate-Drain Charge ^c	Q _{gd}			-	2.5	-		
Gate Resistance	R _g	f = 1 MHz		1.2	2.5	5.4	Ω	
Turn-On Delay Time ^c	t _{d(on)}				5	8	ns	
Rise Time ^c	t _r	$V_{DD} = 30 \text{ V}, \text{ R}_L = 2 \Omega$ $I_D \cong 15 \text{ A}, \text{ V}_{\text{GEN}} = 10 \text{ V}, \text{ R}_g = 1 \Omega$		-	10	15		
Turn-Off Delay Time ^c	t _{d(off)}			-	13	20		
Fall Time ^c	t _f			-	8	12		
Source-Drain Diode Ratings and Chara	acteristics ^b			•				
Pulsed Current ^a	I _{SM}			-	-	50	Α	
Forward Voltage	V _{SD}	I _F =	10 A, V _{GS} = 0 V	-	0.9	1.2	V	
Reverse Recovery Time	t _{rr}	$I_F = 15 \text{ A}, \text{ dI/dt} = 100 \text{ A/µs}$		-	29	60	ns	

Notes

a. Pulse test; pulse width \leq 300 µs, duty cycle \leq 2 %.

b. Guaranteed by design, not subject to production testing.

c. Independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

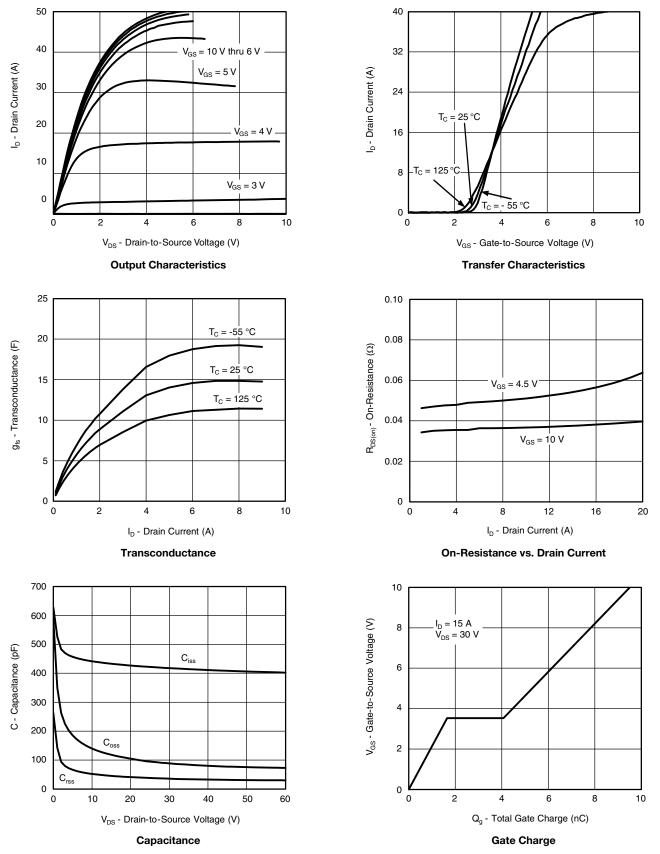
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SQD15N06-42L

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TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



S15-1873-Rev. G, 10-Aug-15

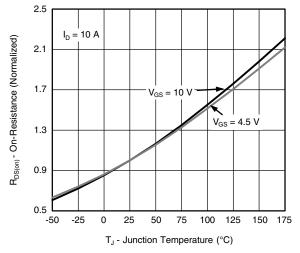
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Document Number: 68880

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SQD15N06-42L

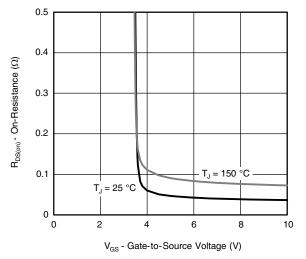
TYPICAL CHARACTERISTICS ($T_A = 25 \text{ °C}$, unless otherwise noted)



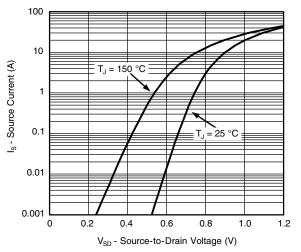
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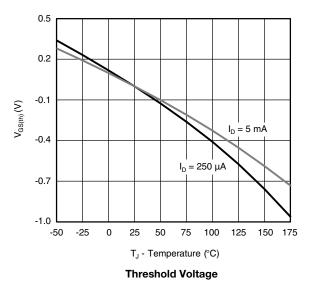
On-Resistance vs. Junction Temperature

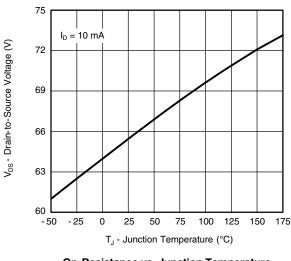


On-Resistance vs. Gate-to-Source Voltage



Source Drain Diode Forward Voltage





On-Resistance vs. Junction Temperature

S15-1873-Rev. G, 10-Aug-15

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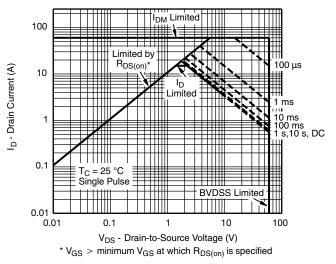
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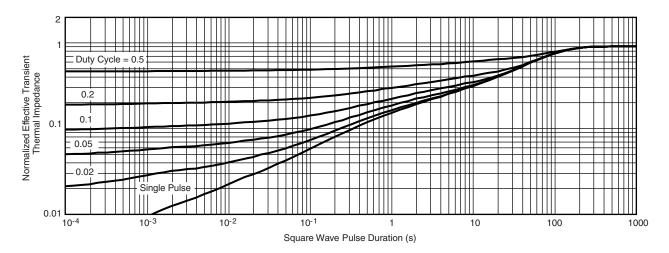


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THERMAL RATINGS ($T_A = 25 \text{ °C}$, unless otherwise noted)



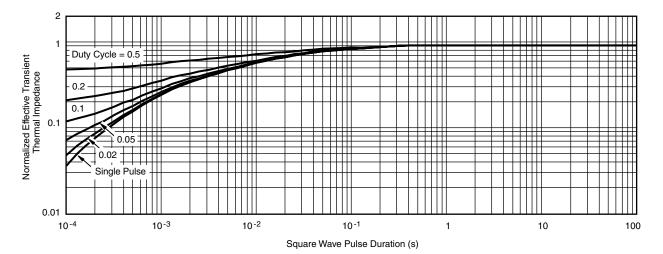
Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Ambient



THERMAL RATINGS (T_A = 25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Case

Note

• The characteristics shown in the two graphs

- Normalized Transient Thermal Impedance Junction-to-Ambient (25 °C)

- Normalized Transient Thermal Impedance Junction-to-Case (25 °C)

are given for general guidelines only to enable the user to get a "ball park" indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions.

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?68880.



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REVISION	HISTORY ^a	
REVISION	DATE	DESCRIPTION OF CHANGE
G	04-Aug-15	Revised R _g minimum limit

Note

a. As of April 2014





Е b3 Ľ Δ ŝ b2 e1 Б E1

C2 т gage plane height (0.5 mm)

-C

- A1

TO-252AA Case Outline

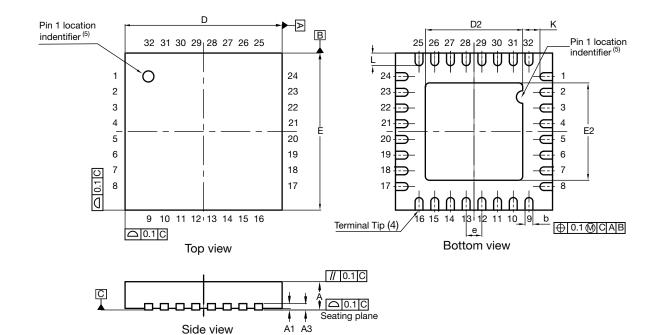
	MILLIMETERS		INCHES	
DIM.	MIN.	MAX.	MIN.	MAX.
А	2.18	2.38	0.086	0.094
A1	-	0.127	-	0.005
b	0.64	0.88	0.025	0.035
b2	0.76	1.14	0.030	0.045
b3	4.95	5.46	0.195	0.215
С	0.46	0.61	0.018	0.024
C2	0.46	0.89	0.018	0.035
D	5.97	6.22	0.235	0.245
D1	4.10	-	0.161	-
Е	6.35	6.73	0.250	0.265
E1	4.32	-	0.170	-
Н	9.40	10.41	0.370	0.410
е	2.28	2.28 BSC 0.090 BSC		
e1	4.56 BSC		0.180 BSC	
L	1.40	1.78	0.055	0.070
L3	0.89	1.27	0.035	0.050
L4	-	1.02	-	0.040
L5	1.01	1.52	0.040	0.060
ECN: T13-0592-Rev. A, 02-Sep-13 DWG: 6019				

Note

• Dimension L3 is for reference only.







QFN32 5 x 5 Case Outline

MILLIMETERS INCHES DIM. MIN. NOM. MAX. MIN. NOM. MAX. 0.75 0.85 0.95 0.029 0.033 0.037 А 0.002 A1 0.00 0.05 0.000 --A3 0.20 ref. 0.008 ref. 0.012 b 0.18 0.25 0.30 0.007 0.010 D 5.00 BSC 0.197 BSC D2 3.00 3.20 0.122 0.126 3.10 0.118 0.50 BSC 0.020 BSC е 5.00 BSC 0.197 BSC Е E2 3.00 3.10 3.20 0.118 0.122 0.126 κ 0.20 0.008 ----L 0.30 0.40 0.50 0.012 0.016 0.020 N ⁽³⁾ 32 32 Nd ⁽³⁾ 8 8 Ne ⁽³⁾ 8 8

Notes

- ⁽¹⁾ Use millimeters as the primary measurement
- ⁽²⁾ Dimensioning and tolerances conform to ASME Y14.5M. 1994
- ⁽³⁾ N is the number of terminals, Nd is the number of terminals in X-direction and Ne is the number of terminals in Y-direction.
- ⁽⁴⁾ Dimension b applies to plated terminal and is measured between 0.15 mm and 0.30 mm from terminal tip
- ⁽⁵⁾ The pin #1 identifier must be existed on the top surface of the package by using indentation mark or other feature of package body
 ⁽⁶⁾ Package warpage max. 0.05 mm

S14-2079-Rev. A, 20-Oct-14 DWG: 6027

Revision: 20-Oct-14

Document Number: 67244

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RECOMMENDED MINIMUM PADS FOR DPAK (TO-252)



Recommended Minimum Pads Dimensions in Inches/(mm)

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