A product Line of
Diodes Incorporated

PI3USB32

High-Speed USB 2.0 (480 Mbps) 1-Port Switch with Full Power Down Feature

Features

- V_{DD} Operation at 3 V and 4.3 V
- 1.8-V Compatible Control-Pin Inputs
- I_{OFF} Supports Full Power-Down Mode Operation
- r_{on} = 6-Ohm Typical
- Dr_{on} <0.35-Ohm Typical
- Cio(ON) = 5 pF Typical
- Low Power Consumption
- ESD Performance
  - 7kV Human-Body Model, per JESD22 spec (A114-B, Class II)
  - 1000-V Charged-Device Model (C101)
  - ±4kV contact, per IEC61000-4-2
- Wide –3-dB Bandwidth = 2110 MHz Typical
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. “Green” Device (Note 3)
- Packaged in 8-Lead TLLGA (1.5 mm x 1.5 mm)

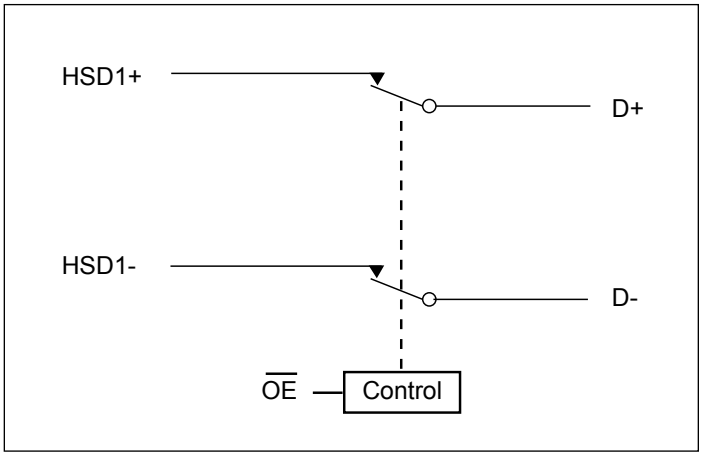
Description

The PI3USB32 is a high-bandwidth switch specially designed for the switching of high-speed USB 2.0 signals in handset and consumer applications, such as cell phones, digital cameras, and notebooks with hubs or controllers with limited USB I/Os. The wide bandwidth (750 MHz) of this switch allows signals to pass with minimum edge and phase distortion. The switch is bidirectional and offers little or no attenuation of the high-speed signals at the outputs. It is designed for low bit-to-bit skew and high channel-to-channel noise isolation, and is compatible with various standards, such as high-speed USB 2.0 (480 Mbps).

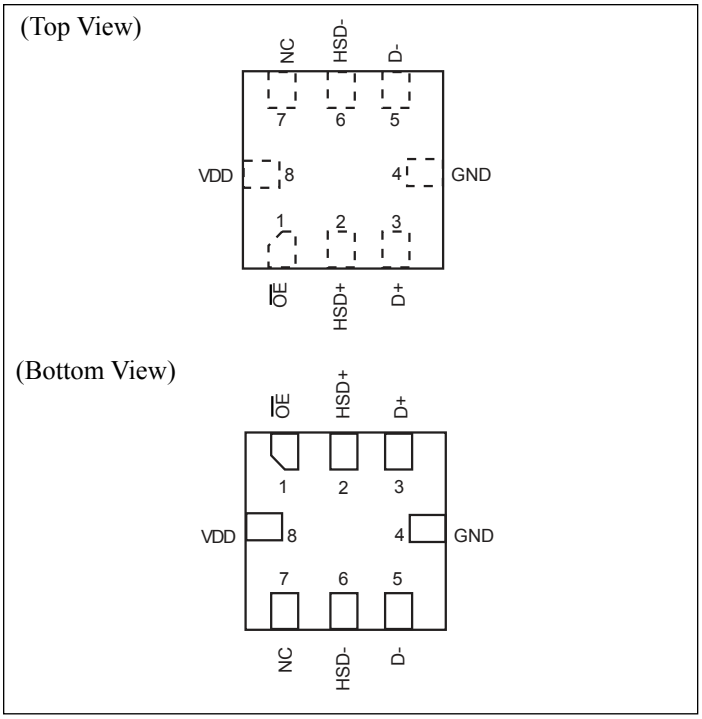
Application

- Routes Signals for USB 1.0, 1.1, and 2.0

Block Diagram



Pin Configuiration



NC = No Internal Connection

Notes:

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated’s definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green” products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

Pin Description

Name	Description
$\overline{OE}$	Bus-switch enable
D+, D-, HSD+, HSD-	Data ports
NC	No connect

Truth Table

$\overline{OE}$	Description
H	Disconnect
L	D+, D- = HSD+, HSD-

Absolute Maximum Ratings(1)

(Over operating free-air temperature range unless otherwise noted.)

Supply Voltage Range (V_{DD}) ..... –0.5V to +7V
Control Input Voltage Range (V_{IN})(2)(3) ..... –0.5V to +7V
VI/O Switch I/O Voltage Range(2)(3)(4)
HSD+, HSD– ..... –0.5V to V_{DD}+0.3
D+, D– when V_{DD} > 0 ..... –0.5V to V_{DD}+0.3
D+, D– when V_{DD} > 0 ..... 5.25V
Control Input Clamp Current ..... –50 mA
I/O Port Clamp Current ..... –50 mA
ON-state switch current(5) ..... ±64 mA
Continuous current through V_{DD} or GND ..... ±100 mA
I/O Port Clamp Current ..... –50 mA

Note:
(1) Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
(2) All voltages are with respect to ground, unless otherwise specified.
(3) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(4) V_I and V_O are used to denote specific conditions for $V_{I/O}$.
(5) I_I and I_O are used to denote specific conditions for $I_{I/O}$.

Reccomended Operating Conditions(1)

Parameter	Description		Min.	Max.	Units
V_{DD}	Supply voltage		3.0	4.3	V
V_{IH}	High-level control input voltage	V_{DD} = 3V to 3.6V	1.3		V
		V_{DD} = 4.3 V	1.7		
V_{IL}	Input LOW Voltage	V_{DD} = 3V to 3.6V		0.5	V
		V_{DD} = 4.3 V		0.6	
$V_{I/O}$	Data input/output voltage		0	V_{DD}	V
T_A	Operating free-air temperature		-40	85	°C

Notes:
1. All unused control inputs of the device must be held at VDD or GND to ensure proper device operation.

Electrical Characteristics over operating free-air temperature range (unless otherwise noted)

Parameter		Test Conditions[1]	Min	Typ.[2]	Max	Unit
V_{IK}		V_{DD} = 3 V, I_I = –18 mA			-1.2	V
I_{IN}	Control inputs	V_{DD} = 4.3 V, V_{IN} = 0 to 4.3 V, V_{DD} = 0 V			±1	µA
I_{OZ}[3]		V_{DD} = 4.3 V, V_O = 0 to 3.6V, V_I = 0, Switch OFF			±1	µA
I_{OFF}	D+ and D-	V_{DD} = 0 V, V_O = 0 to 4.3 V, V_I = 0, V_{IN} = V_{DD} or GND			±2	µA
I_{CC}		V_{DD} = 4.3 V, $I_{I/O}$ = 0			70	µA
DI_{CC}[4]	Control inputs	V_{DD} = 4.3 V, V_{IN} = 2.6 V			10	µA
C_{IN}	Control inputs	V_{DD} = 0 V, V_{IN} = V_{DD} or GND		1		pF
Cio(OFF)		V_{DD} = 3.3 V, Switch OFF		2		pF
Cio(ON)		V_{DD} = 3.3 V, Switch ON		5		pF
R_{ON}[5]		V_{DD} = 3 V, V_I = 0.4 V, IO = –8 mA		6	10	W
DR_{ON}		V_{DD} = 3 V, V_I = 0.4 V, IO = –8 mA		0.35		W
$DR_{ON(flat)}$		V_{DD} = 3 V, V_I = 0 V or 1 V, IO = –8 mA		2		W

Notes:

1. V_{IN} and I_{IN} refer to control input ($\overline{OE}$). V_I, V_O, I_I, and I_O refer to data pins.
2. All typical values are at V_{DD} = 3.3 V (unless otherwise noted), T_A = 25°C.
3. For I/O ports, the parameter I_{OZ} includes the input leakage current.
4. This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{DD} or GND.
5. Measured by the voltage drop between the D and HSD terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two terminals.

Dynamic Electrical Characteristics (over operating range, T_A = –40°C TO 85°C, V_{DD} = 3.3 V ± 10%, GND = 0 V)

Parameter	Description	Test Conditions[1]	Typ.[1]	Units
O_{IRR}	OFF isolation	R_L = 50-Ohms, f = 240 MHz	-30	dB
BW	Bandwidth (-3 dB)	R_L = 50-Ohms	2110	MHz
Xtalk	Crosstalk	R_L =50-Ohms, f = 240 MHz	-55	dB

Notes:

1. For Max or Min conditions, use the appropriate value specified under Electrical Characteristics for the applicable device type.

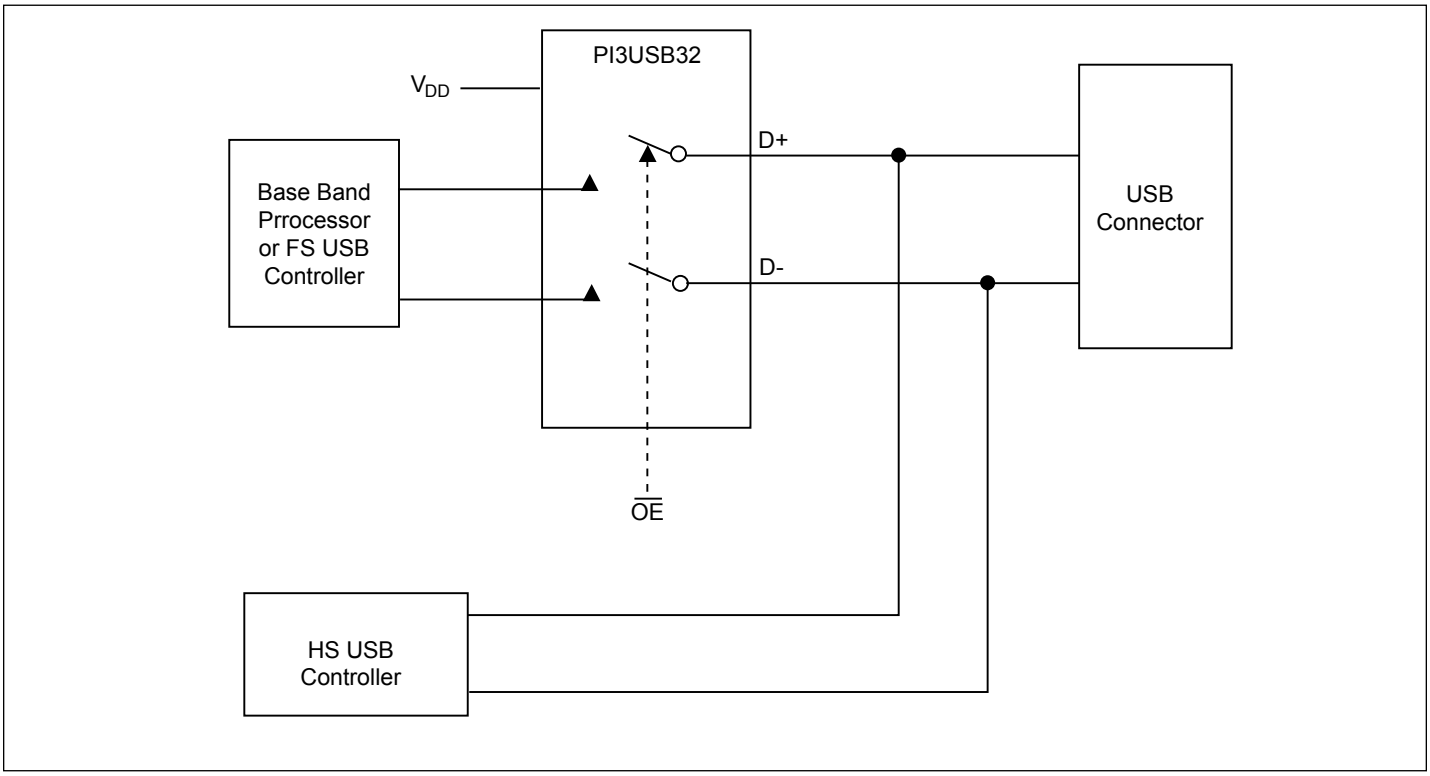
Switching Characteristics (over operating range, T_A = –40°C TO 85°C, V_{DD} = 3.3 V ± 10%, GND = 0 V)

Parameters	Description	Test Conditions (1)	Min.	Typ.	Max.	Units
t_{PD}	Propagation Delay(2,3)	R_L = 50 Ω, C_L = 5 pF			0.35	ns
t_{ON}	Line Enable Time, $\overline{OE}$ to D+/D-	R_L = 50 Ω, C_L = 5 pF			55	ns
t_{OFF}	Line Disable Time - $\overline{OE}$ to D+/D-	R_L = 50 Ω, C_L = 5 pF			25	ns
$t_{SK(P)}$	Skew between opposite transitions of the same output (t_{PHL} - t_{PLH})[2]	R_L = 50 Ω, C_L = 5 pF		50		ps
t_J	Total Jitter[2]	R_L = 50 Ω, C_L = 5 pF, tR = t_F = 500 ps at 480 Mbps (PBRS= 2^{15} - 1)		200		ps

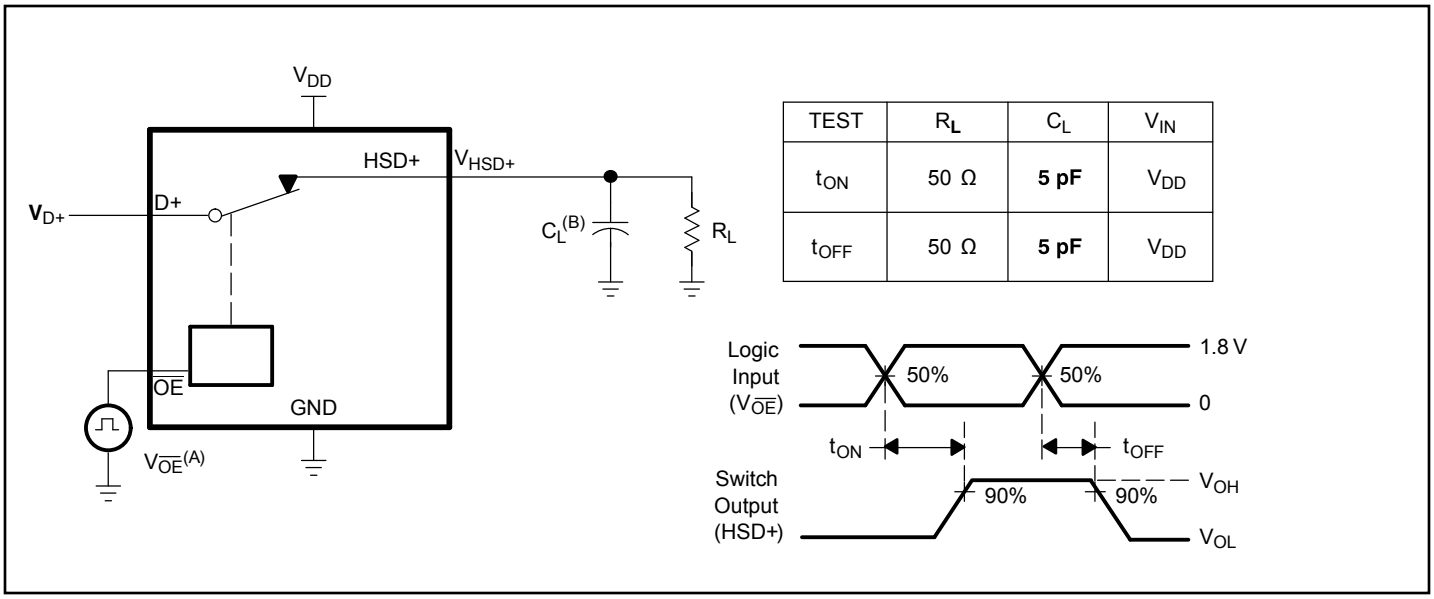
Notes:

1. For Max or Min conditions, use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Guaranteed by design.
3. The bus switch contributes no propagational delay other than the RC delay of the on resistance of the switch and the load capacitance. The time constant for the switch alone is of the order of 0.25 ns for 10-pF load. Since this time constant is much smaller than the rise/fall times of typical driving signals, it adds very little propagational delay to the system. Propagational delay of the bus switch, when used in a system, is determined by the driving circuit on the driving side of the switch and its interactions with the load on the driven side.

Application Information



Application Diagram



TEST	R_L	C_L	V_{IN}
t_{ON}	50 Ω	**5 pF**	V_{DD}
t_{OFF}	50 Ω	**5 pF**	V_{DD}

Figure 1. Turn-On (t_{ON}) and Turn-Off Time (t_{OFF})

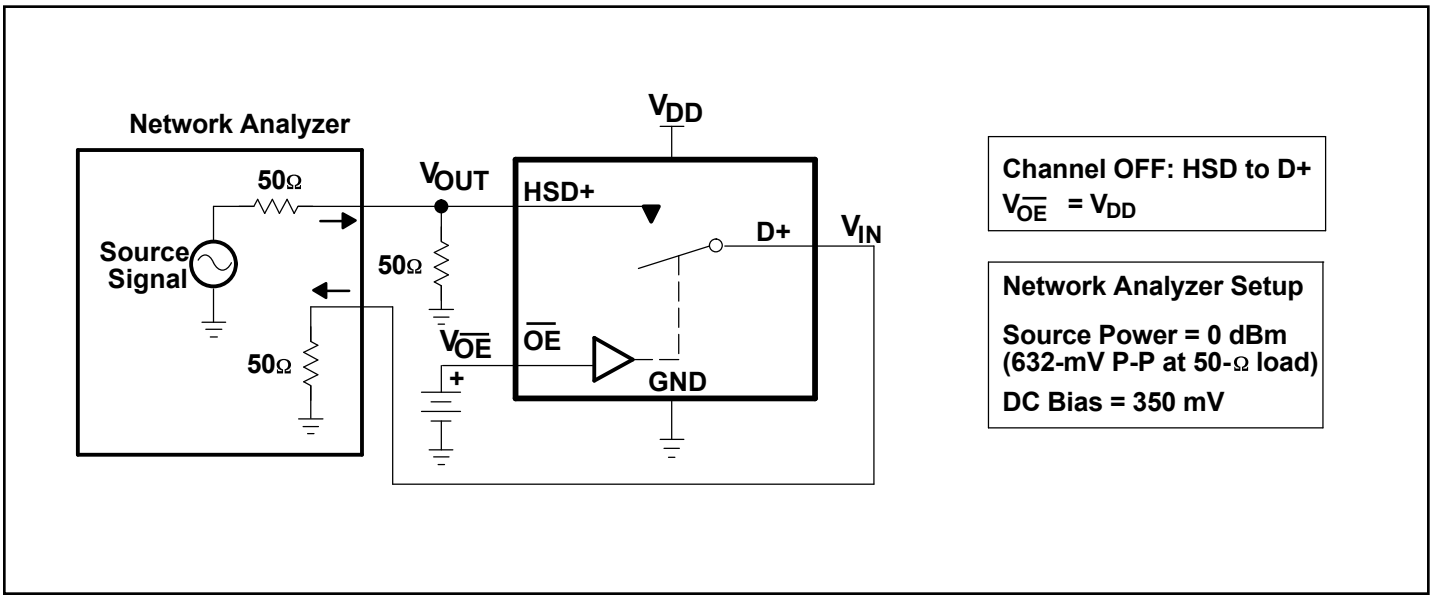


Figure 2. OFF Isolation (OIRR)

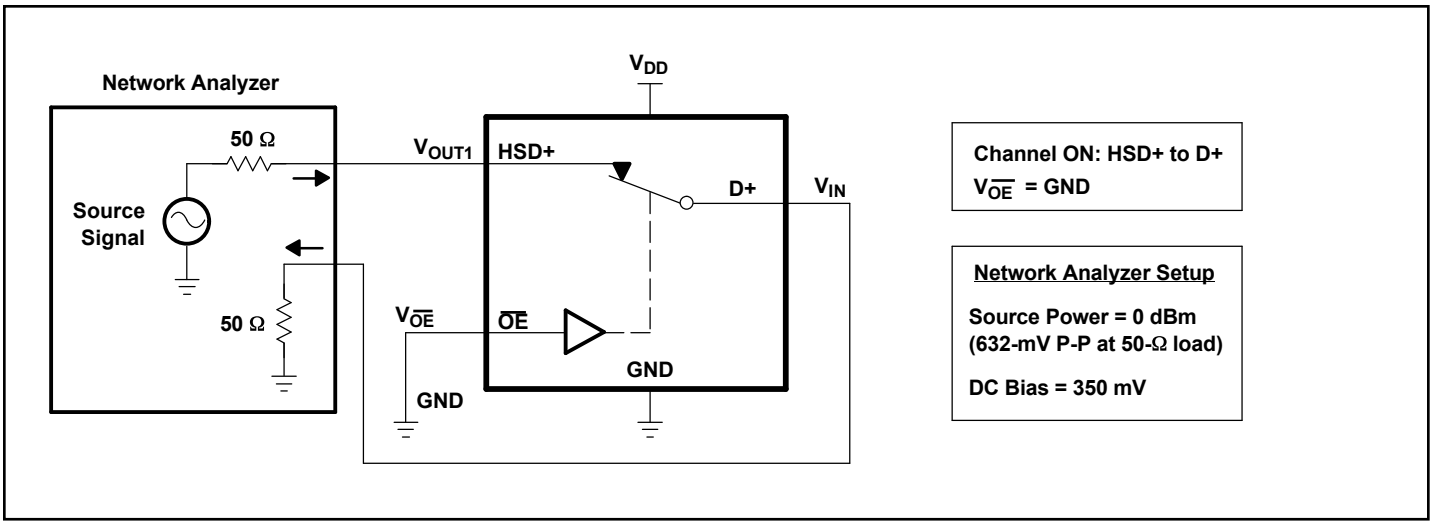


Figure 3. Bandwidth (BW)

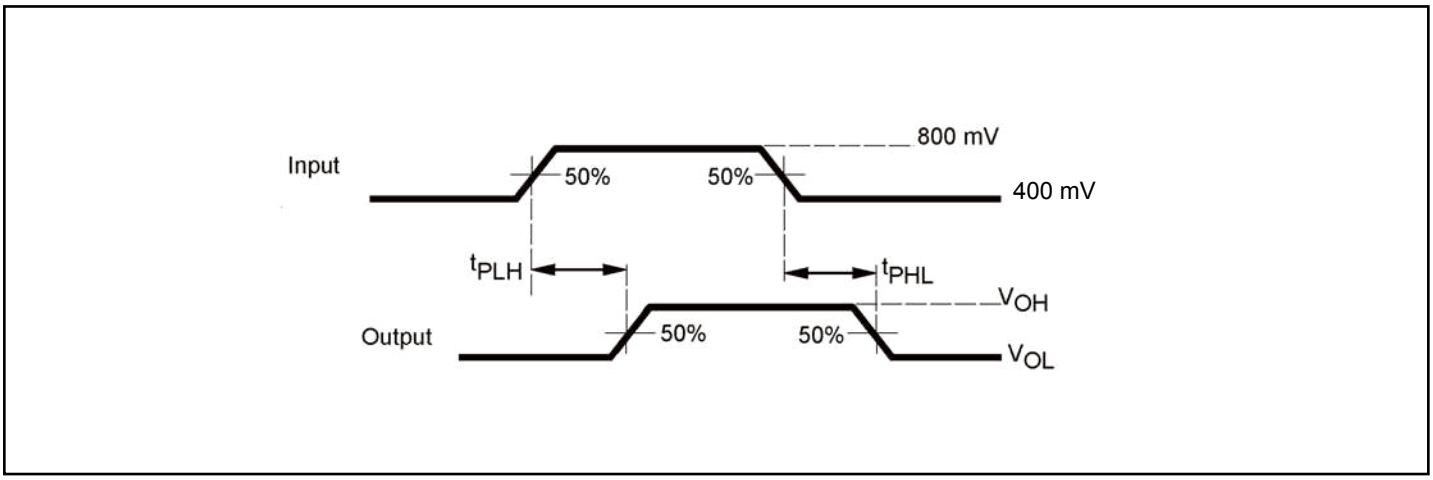
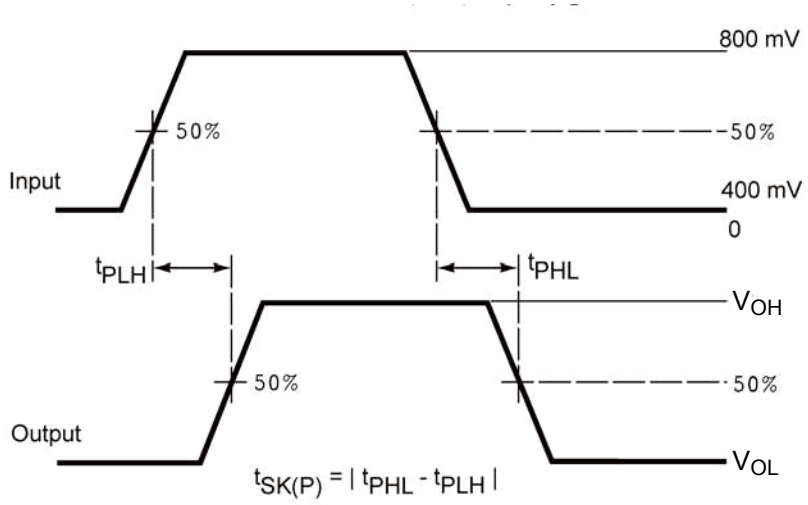
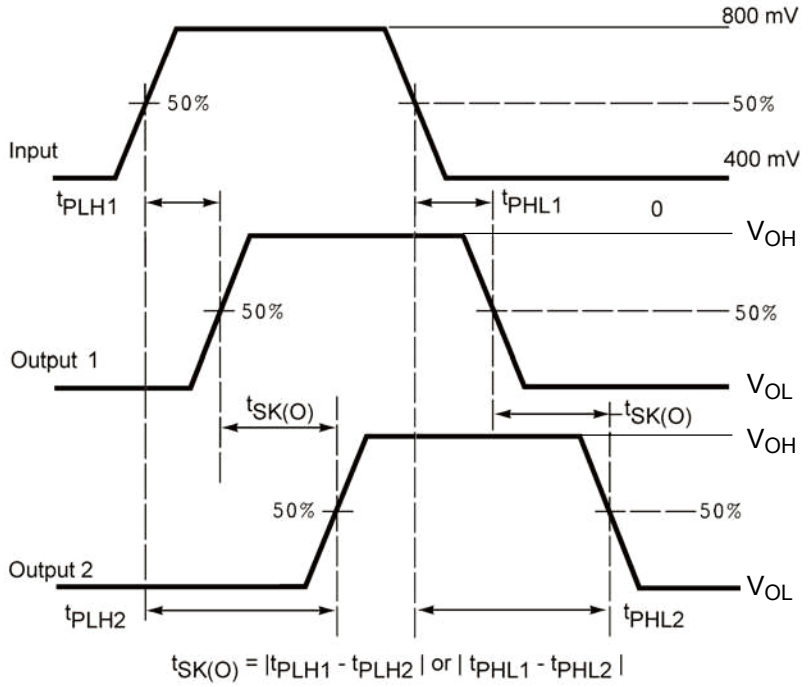


Figure 4. Propagation Delay



Pulse Skew $t_{SK(P)}$



Output Skew $t_{SK(P)}$

Figure 5. Skew Test

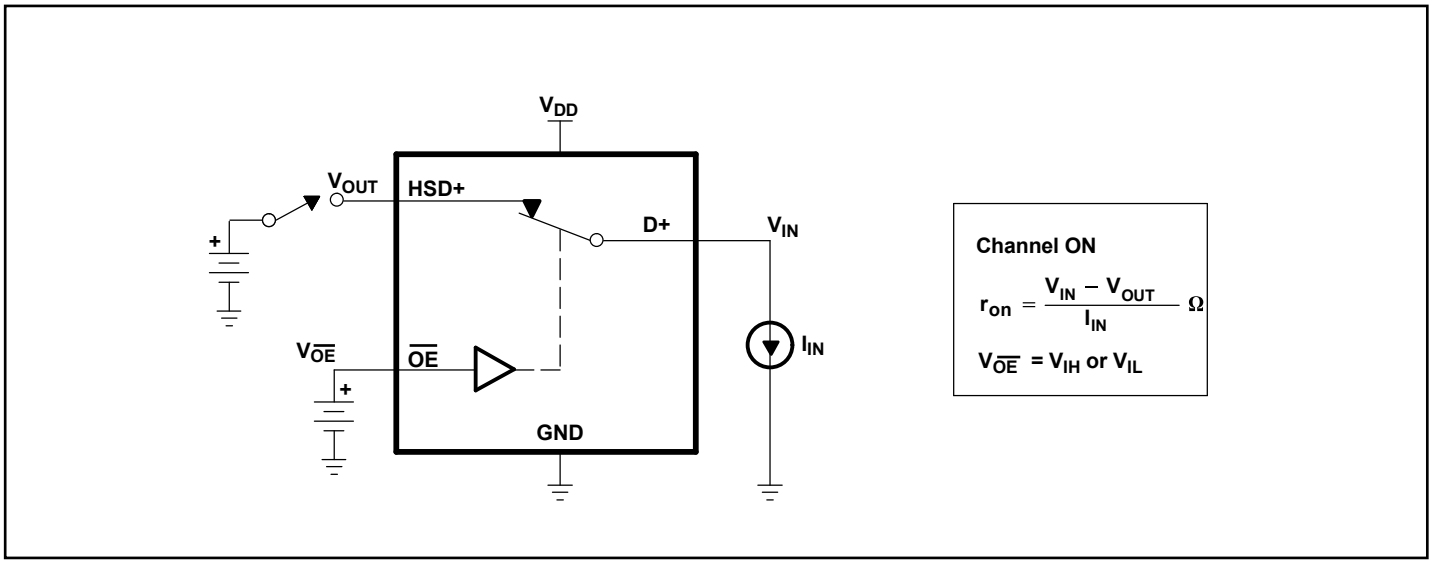


Figure 6. ON-State Resistance (r_{on})

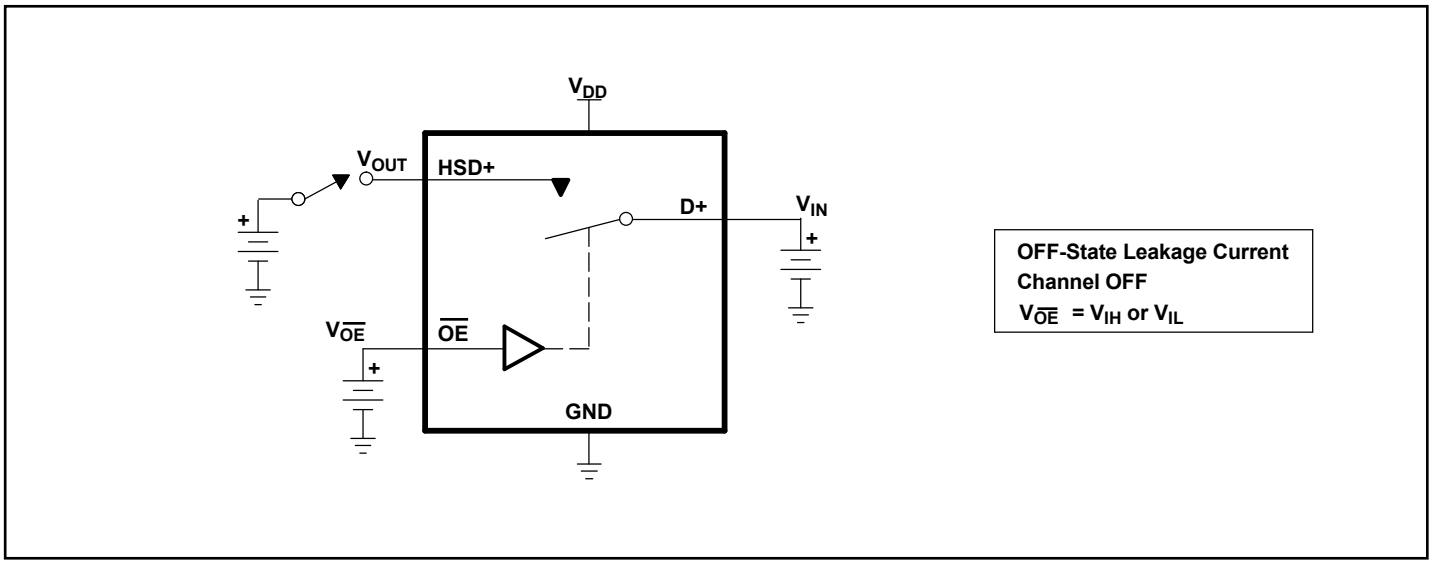


Figure 7. OFF-State Leakage Current

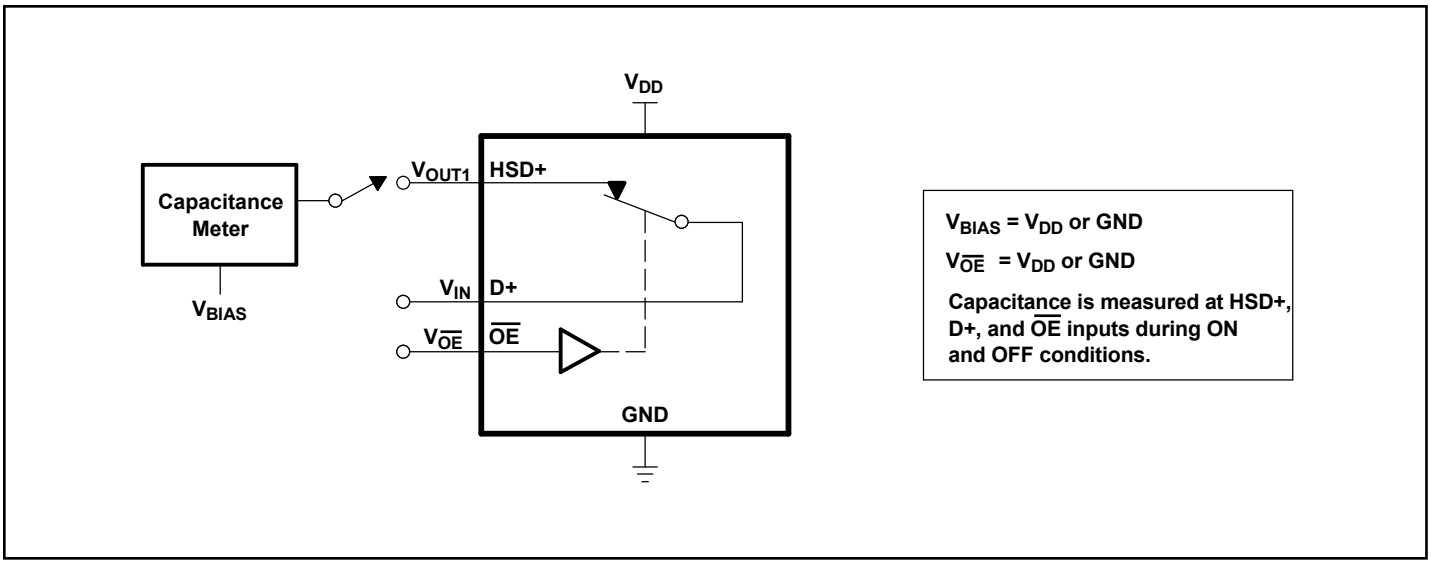


Figure 8. Capacitance

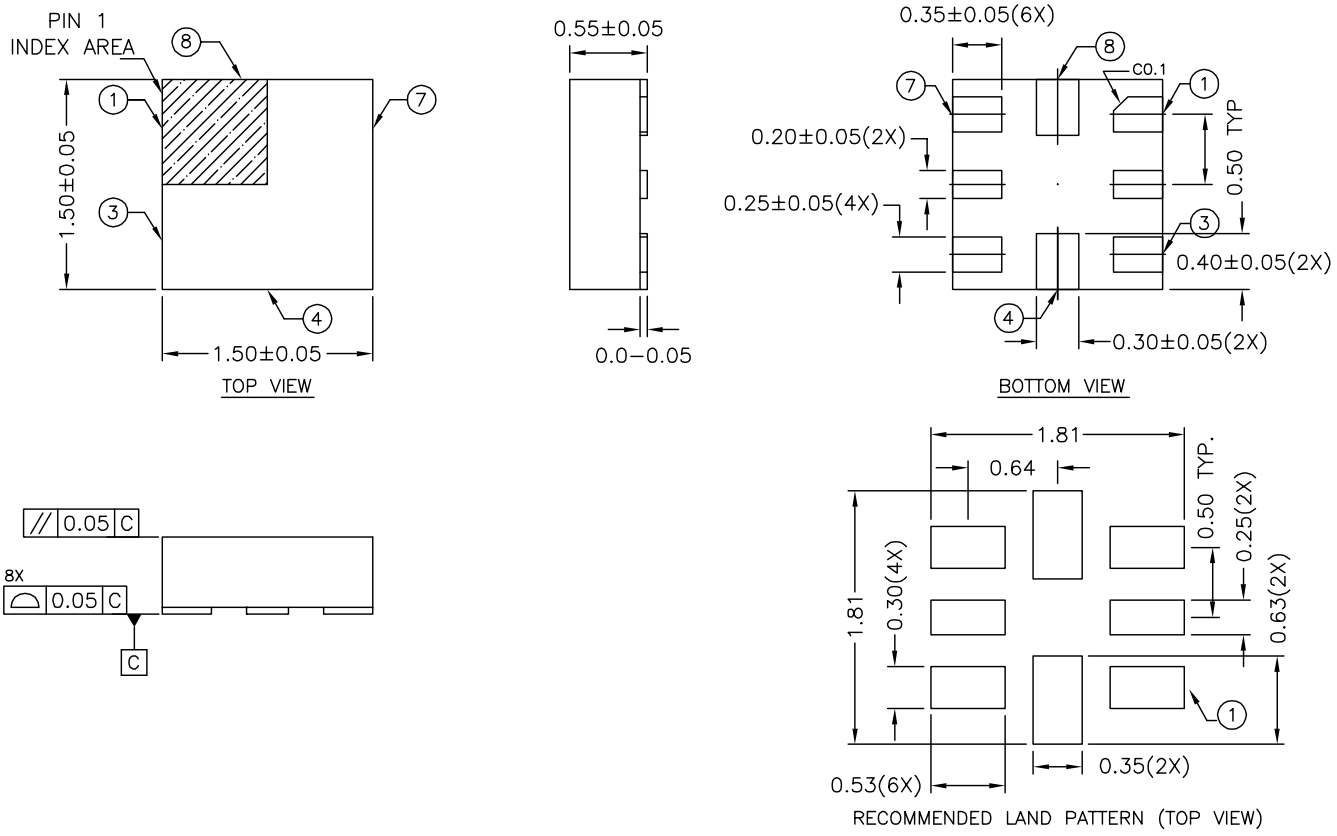
Part Marking

XA Package

Top mark not available at this time. To obtain advance information regarding the top mark, please contact your local sales representative.

Packaging Mechanical:

8-TLLGA (XA)



NOTE :

1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS
3. REFER JEDEC MO-288
4. RECOMMENDED LAND PATTERN IS FOR REFERENCE ONLY.

PERICOM Semiconductor Corporation — DATE:01/28/09

DESCRIPTION: 8-Lead, Thin Leadframe Land Grid Array (TLLGA)

PACKAGE CODE: XA8

DOCUMENT CONTROL #: PD-2081 — REVISION: A

09-0065

For latest package info.

please check: http://www.diodes.com/design/support/packaging/pericom-packaging/packaging-mechanicals-and-thermal-characteristics/

Ordering Information

Ordering Code	Package Code	Description	Top Mark
PI3USB32XAEX	XA	8-Lead, Thin Leadframe Land Grid Array (TLLGA)	EK

Notes:

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
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3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. E = Pb-free and Green
5. X suffix = Tape/Reel

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