

N-Channel 100 V (D-S) MOSFET

PRODUCT SUMMARY

V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)	Q_g (Typ)
100	0.200 at $V_{GS} = 10$ V	6.5	2.7
	0.225 at $V_{GS} = 4.5$ V	6	

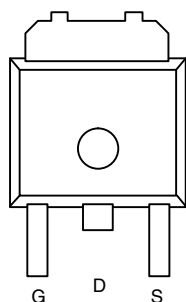
FEATURES

- TrenchFET® Power MOSFETs
- Material categorization:
For definitions of compliance please see www.vishay.com/doc?99912



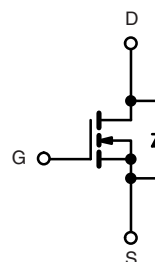
RoHS
COMPLIANT
HALOGEN
FREE

TO-252



Top View

Drain Connected to Tab



N-Channel MOSFET

Order Number:

SUD06N10-225L-GE3 (Lead (Pb)-free and Halogen-free)

ABSOLUTE MAXIMUM RATINGS ($T_A = 25$ °C, unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	100	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current ($T_J = 150$ °C) ^b	I_D	6.5	A
		2.9	
Pulsed Drain Current	I_{DM}	8	
Continuous Source Current (Diode Conduction)	I_S	6.5	
Avalanche Current	I_{AR}	5	
Repetitive Avalanche Energy (Duty Cycle ≤ 1 %)	$L = 0.1$ mH E_{AR}	1.25	mJ
Maximum Power Dissipation	P_D	16.7 ^b	W
		1.25 ^a	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to 150	°C

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Typical	Maximum	Unit
Junction-to-Ambient ^a	R_{thJA}	40	50	°C/W
		80	100	
Junction-to-Case	R_{thJC}	6	7.5	

Notes:

a. Surface mounted on 1" x 1" FR4 board.

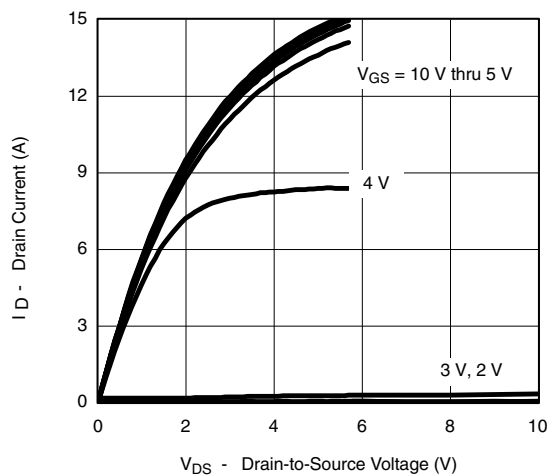
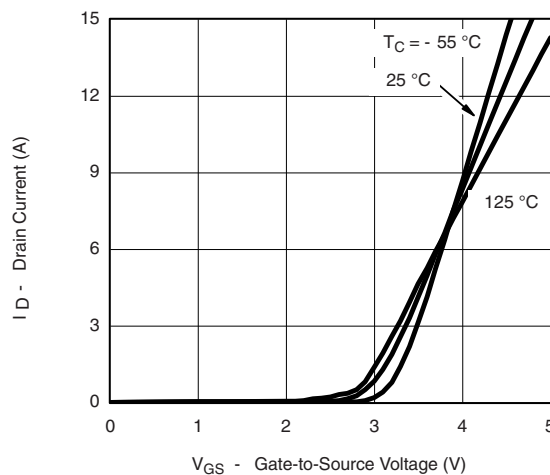
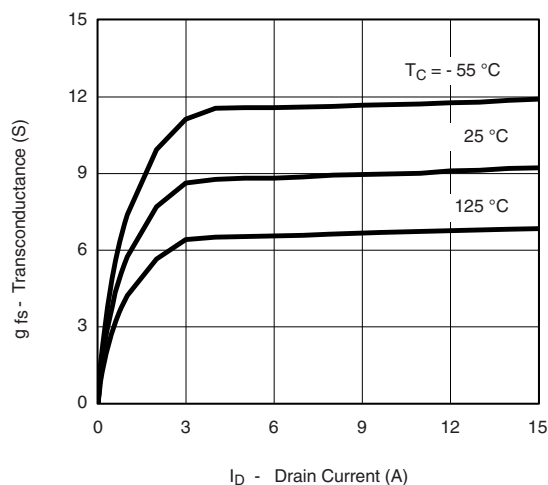
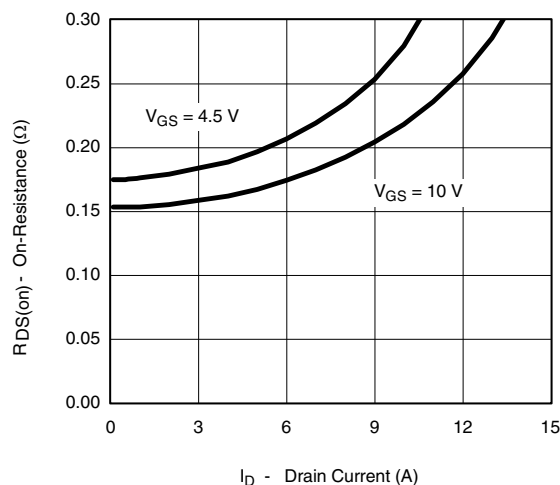
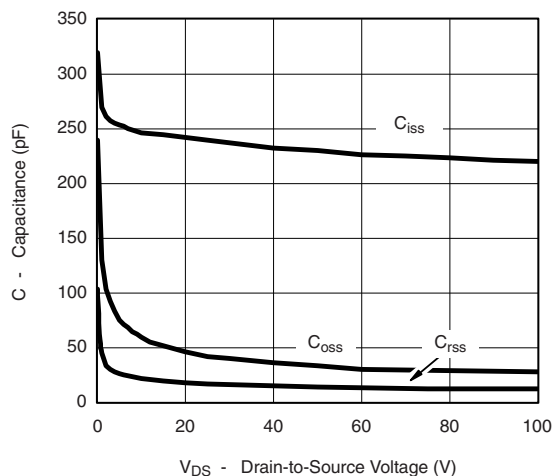
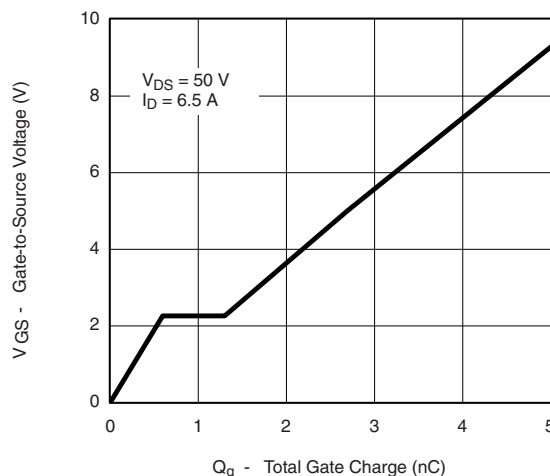
b. See SOA curve for voltage derating.

SPECIFICATIONS (T _A = 25 °C, unless otherwise noted)						
Parameter	Symbol	Test Conditions	Min.	Typ. ^a	Max.	Unit.
Static						
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA	100			V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	1		3	
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20 V			± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 100 V, V _{GS} = 0 V			1	μA
		V _{DS} = 100 V, V _{GS} = 0 V, T _J = 125 °C			50	
On-State Drain Current ^b	I _{D(on)}	V _{DS} = 5 V, V _{GS} = 10 V	8			A
Drain-Source On-State Resistance ^b	R _{DS(on)}	V _{GS} = 10 V, I _D = 3 A		0.160	0.200	Ω
		V _{GS} = 10 V, I _D = 3 A, T _J = 125 °C			0.350	
		V _{GS} = 4.5 V, I _D = 1 A		0.180	0.225	
Forward Transconductance ^b	g _{fs}	V _{DS} = 15 V, I _D = 3 A		8.5		S
Dynamic ^a						
Input Capacitance	C _{iss}	V _{GS} = 0 V, V _{DS} = 25 V, F = 1 MHz		240		pF
Output Capacitance	C _{oss}			42		
Reverse Transfer Capacitance	C _{rss}			17		
Total Gate Charge ^c	Q _g	V _{DS} = 50 V, V _{GS} = 5 V, I _D = 6.5 A		2.7	4	nC
Gate-Source Charge ^c	Q _{gs}			0.6		
Gate-Drain Charge ^c	Q _{gd}			0.7		
Turn-On Delay Time ^c	t _{d(on)}	V _{DD} = 50 V, R _L = 7.5 Ω I _D ≡ 6.5 A, V _{GEN} = 10 V, R _g = 2.5 Ω		7	11	ns
Rise Time ^c	t _r			8	12	
Turn-Off Delay Time ^c	t _{d(off)}			8	12	
Fall Time ^c	t _f			9	14	
Source-Drain Diode Ratings and Characteristics (T _C = 25 °C)						
Pulsed Current	I _{SM}				8	A
Diode Forward Voltage ^b	V _{SD}	I _F = 6.5 A, V _{GS} = 0 V		0.9	1.3	V
Source-Drain Reverse Recovery Time	t _{rr}	I _F = 6.5 A, dI/dt = 100 A/μs		35	60	ns

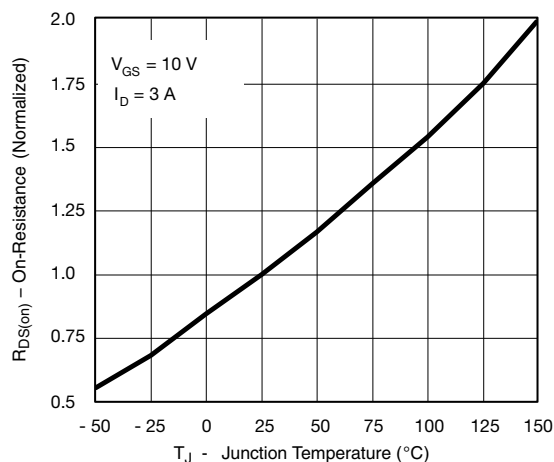
Notes:

- a. Guaranteed by design, not subject to production testing.
b. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
c. Independent of operating temperature.

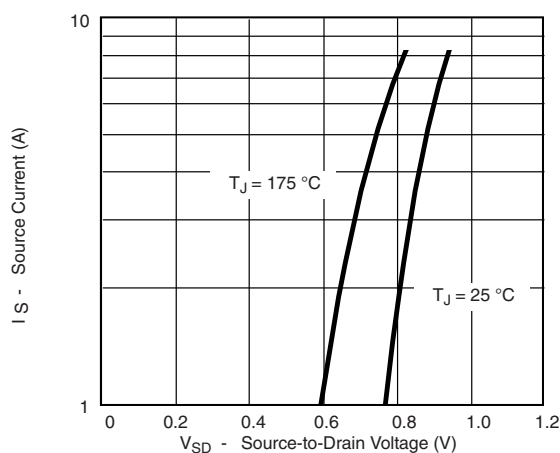
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)

Output Characteristics

Transfer Characteristics

Transconductance

On-Resistance vs. Drain Current

Capacitance

Gate Charge

TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)

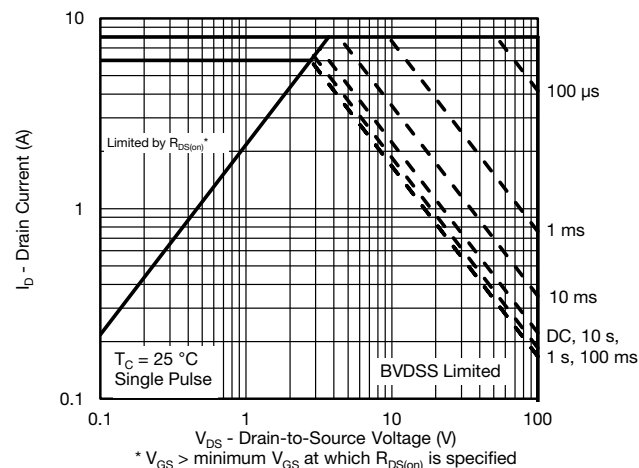
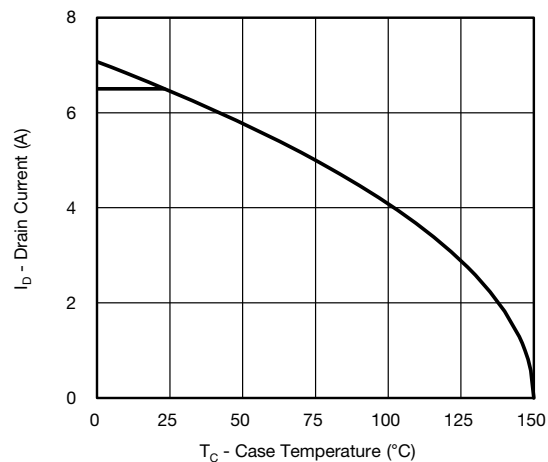


On-Resistance vs. Junction Temperature



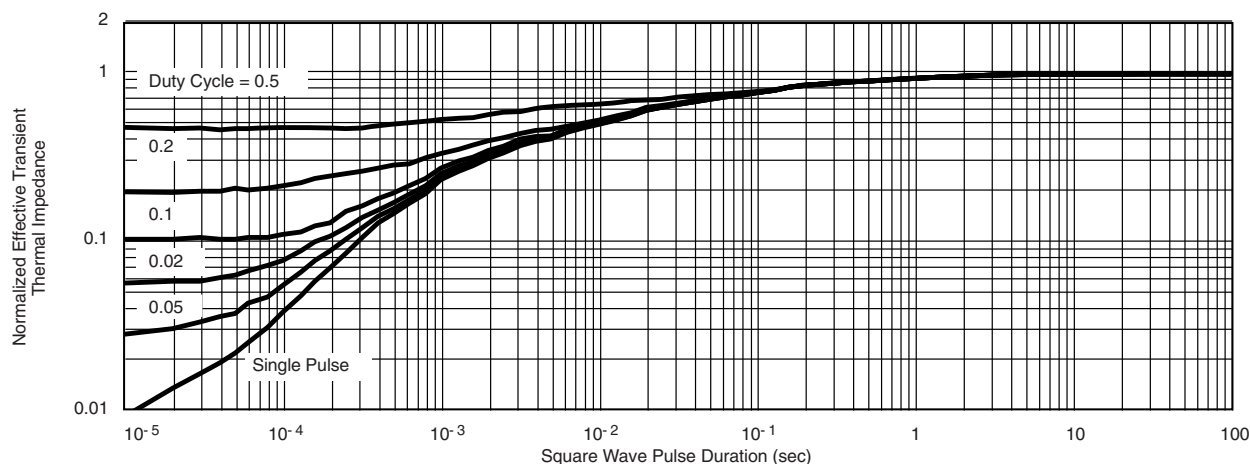
Source-Drain Diode Forward Voltage

THERMAL RATINGS



Maximum Avalanche Drain Current vs. Case Temperature

Safe Operating Area

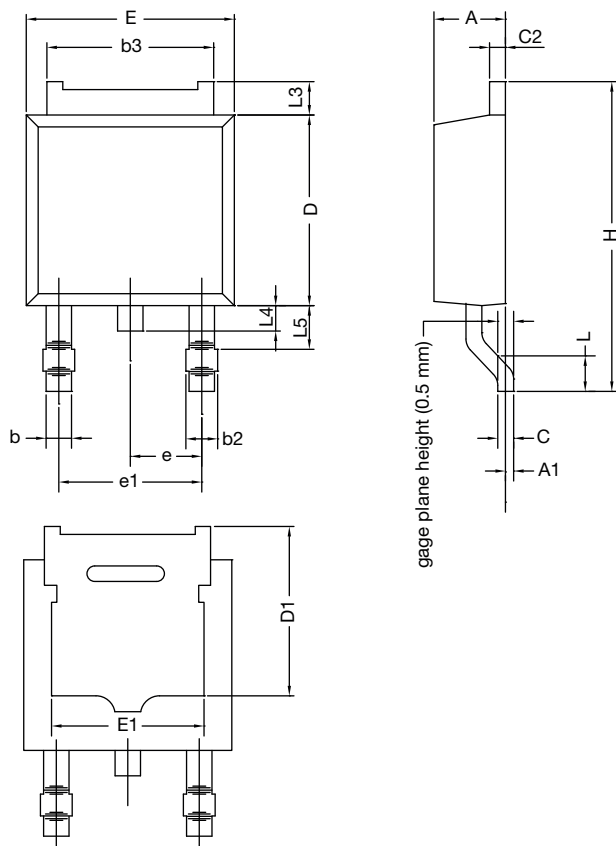


Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?62831.



TO-252AA Case Outline

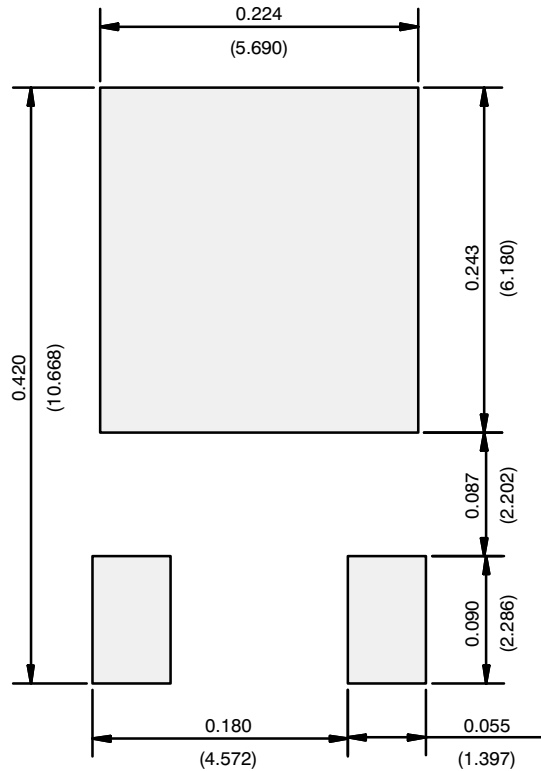


DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	2.18	2.38	0.086	0.094
A1	-	0.127	-	0.005
b	0.64	0.88	0.025	0.035
b2	0.76	1.14	0.030	0.045
b3	4.95	5.46	0.195	0.215
C	0.46	0.61	0.018	0.024
C2	0.46	0.89	0.018	0.035
D	5.97	6.22	0.235	0.245
D1	4.10	-	0.161	-
E	6.35	6.73	0.250	0.265
E1	4.32	-	0.170	-
H	9.40	10.41	0.370	0.410
e	2.28 BSC		0.090 BSC	
e1	4.56 BSC		0.180 BSC	
L	1.40	1.78	0.055	0.070
L3	0.89	1.27	0.035	0.050
L4	-	1.02	-	0.040
L5	1.01	1.52	0.040	0.060
ECN: T16-0236-Rev. P, 16-May-16 DWG: 5347				

Notes

- Dimension L3 is for reference only.

RECOMMENDED MINIMUM PADS FOR DPAK (TO-252)



Recommended Minimum Pads
Dimensions in Inches/(mm)

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