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FDS8840NZ

N-Channel PowerTrench® MOSFET

40 V, 18.6 A, 4.5 mΩ

Features

- Max $r_{DS(on)}$ = 4.5 mΩ at $V_{GS} = 10\text{ V}$, $I_D = 18.6\text{ A}$
- Max $r_{DS(on)}$ = 6.0 mΩ at $V_{GS} = 4.5\text{ V}$, $I_D = 14.9\text{ A}$
- HBM ESD protection level of 6 kV typical(note 3)
- High performance trench technology for extremely low $r_{DS(on)}$ and fast switching
- High power and current handling capability
- Termination is Lead-free and RoHS Compliant

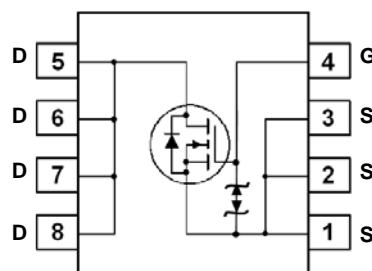
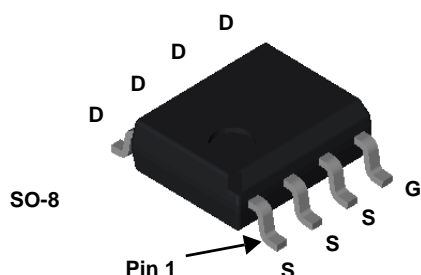


General Description

The FDS8840NZ has been designed to minimize losses in power conversion application. Advancements in both silicon and package technologies have been combined to offer the lowest $r_{DS(on)}$ while maintaining excellent switching performance.

Applications

- Synchronous Buck for Vcore and Server
- Notebook Battery Pack
- Load Switch



MOSFET Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DS}	Drain to Source Voltage	40	V
V_{GS}	Gate to Source Voltage	± 20	V
I_D	Drain Current -Continuous	18.6	A
	-Pulsed	63	
E_{AS}	Single Pulse Avalanche Energy (Note 4)	600	mJ
P_D	Power Dissipation $T_A = 25^\circ\text{C}$ (Note 1a)	2.5	W
	Power Dissipation $T_A = 25^\circ\text{C}$ (Note 1b)	1.0	
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ\text{C}$

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case (Note 1)	25	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	50	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDS8840NZ	FDS8840NZ	SO8	13 "	12 mm	2500 units

Electrical Characteristics $T_J = 25\text{ }^{\circ}\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250\text{ }\mu\text{A}$, $V_{GS} = 0\text{ V}$	40			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$, referenced to $25\text{ }^{\circ}\text{C}$		31		mV/ $^{\circ}\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 32\text{ V}$, $V_{GS} = 0\text{ V}$			1	μA
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 20\text{ V}$, $V_{DS} = 0\text{ V}$			± 10	μA

On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 250\text{ }\mu\text{A}$	1.0	1.8	3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$, referenced to $25\text{ }^{\circ}\text{C}$		-6		mV/ $^{\circ}\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{ V}$, $I_D = 18.6\text{ A}$		3.9	4.5	m Ω
		$V_{GS} = 4.5\text{ V}$, $I_D = 14.9\text{ A}$		4.6	6.0	
		$V_{GS} = 10\text{ V}$, $I_D = 18.6\text{ A}$, $T_J = 125\text{ }^{\circ}\text{C}$		5.9	7.0	
g_{FS}	Forward Transconductance	$V_{DS} = 5\text{ V}$, $I_D = 18.6\text{ A}$		83		S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 20\text{ V}$, $V_{GS} = 0\text{ V}$, $f = 1\text{ MHz}$		5665	7535	pF
C_{oss}	Output Capacitance			650	865	pF
C_{rss}	Reverse Transfer Capacitance			445	670	pF
R_g	Gate Resistance			1.2		Ω

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 20\text{ V}$, $I_D = 18.6\text{ A}$, $V_{GS} = 10\text{ V}$, $R_{GEN} = 6\text{ }\Omega$		18	32	ns
t_r	Rise Time			13	23	ns
$t_{d(off)}$	Turn-Off Delay Time			57	103	ns
t_f	Fall Time			11	20	ns
Q_g	Total Gate Charge	$V_{GS} = 0\text{ V}$ to 10 V	$V_{DD} = 20\text{ V}$, $I_D = 18.6\text{ A}$	103	144	nC
Q_g	Total Gate Charge	$V_{GS} = 0\text{ V}$ to 5 V		54	76	nC
Q_{gs}	Gate to Source Charge			16		nC
Q_{gd}	Gate to Drain "Miller" Charge			19		nC

Drain-Source Diode Characteristics

V_{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}$, $I_S = 18.6\text{ A}$		0.8	1.2	V
		$V_{GS} = 0\text{ V}$, $I_S = 2.1\text{ A}$		0.7	1.2	
t_{rr}	Reverse Recovery Time	$I_F = 18.6\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$		33	53	ns
Q_{rr}	Reverse Recovery Charge			21	34	nC

NOTES:

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 50 $^{\circ}\text{C}/\text{W}$ when mounted on a 1 in² pad of 2 oz copper.



b) 125 $^{\circ}\text{C}/\text{W}$ when mounted on a minimum pad.

2. Pulse Test: Pulse Width < 300 μs , Duty cycle < 2.0%.

3. The diode connected between the gate and source serves only as protection against ESD. No gate overvoltage rating is implied.

4. Starting $T_J = 25\text{ }^{\circ}\text{C}$, $L = 3\text{ mH}$, $I_{AS} = 20\text{ A}$, $V_{DD} = 40\text{ V}$, $V_{GS} = 10\text{ V}$.

Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

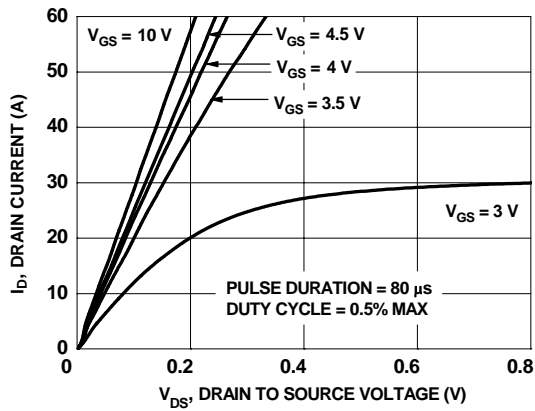


Figure 1. On-Region Characteristics

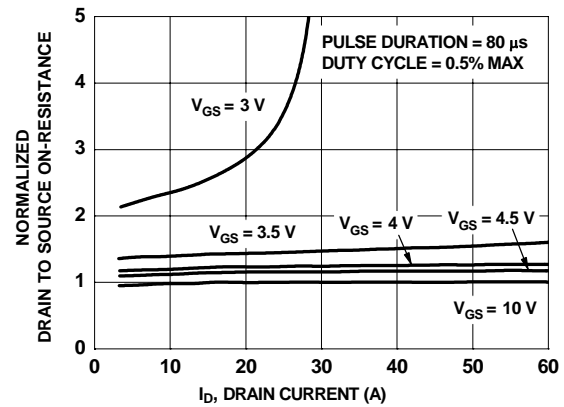


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

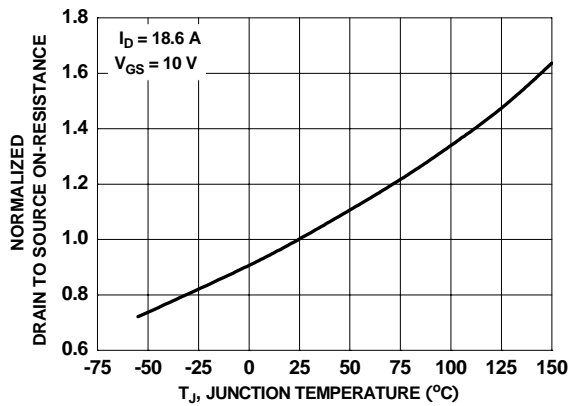


Figure 3. Normalized On-Resistance vs Junction Temperature

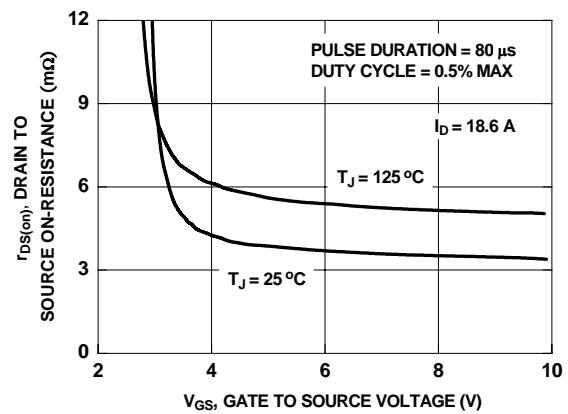


Figure 4. On-Resistance vs Gate to Source Voltage

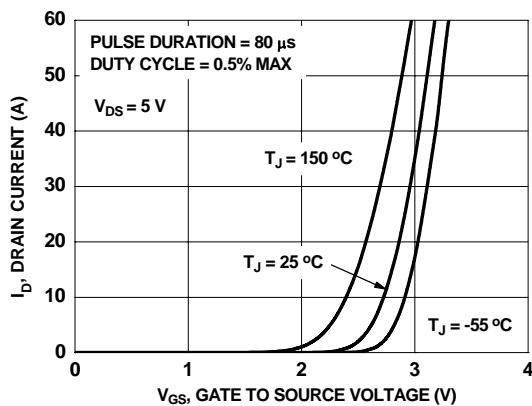


Figure 5. Transfer Characteristics

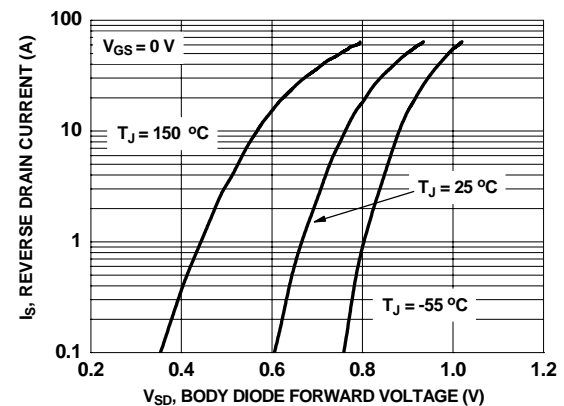


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

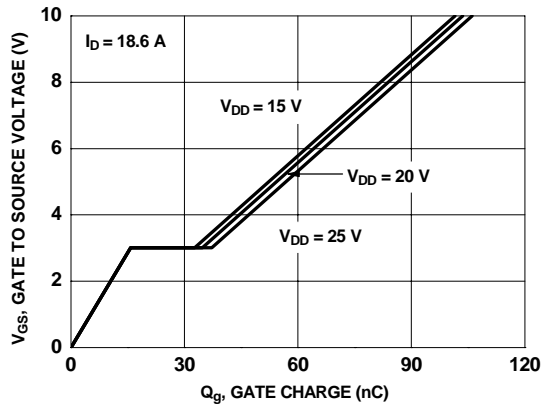


Figure 7. Gate Charge Characteristics

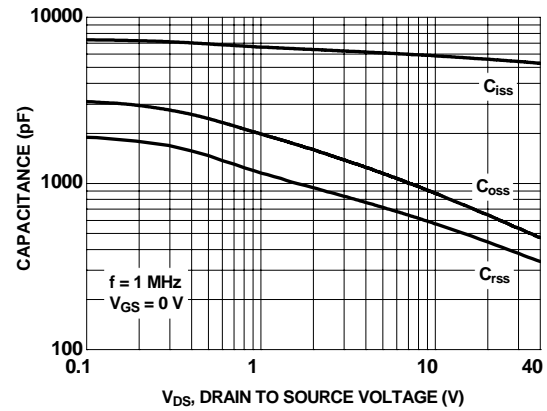


Figure 8. Capacitance vs Drain to Source Voltage

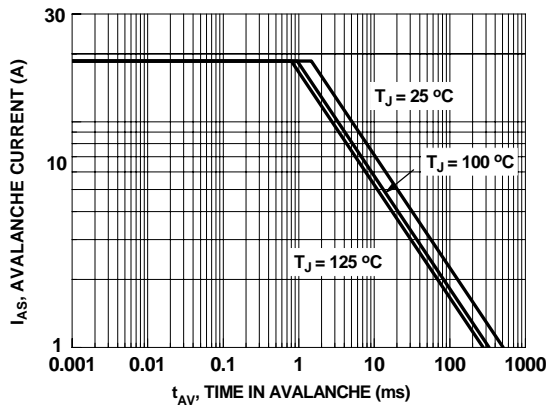


Figure 9. Unclamped Inductive Switching Capability

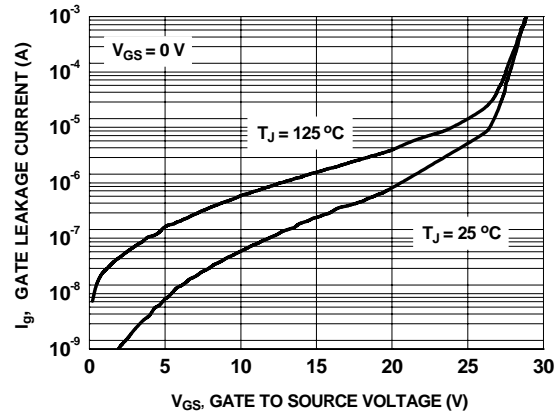


Figure 10. I_{gss} vs V_{GS}

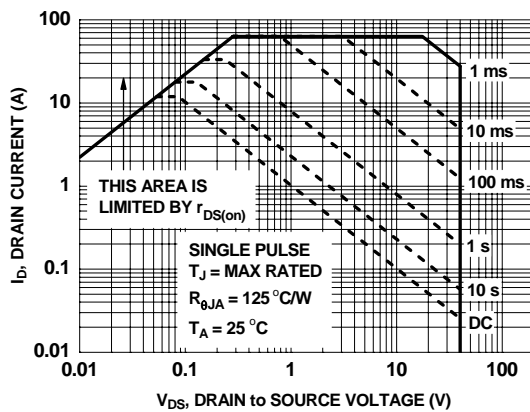


Figure 11. Forward Bias Safe Operating Area

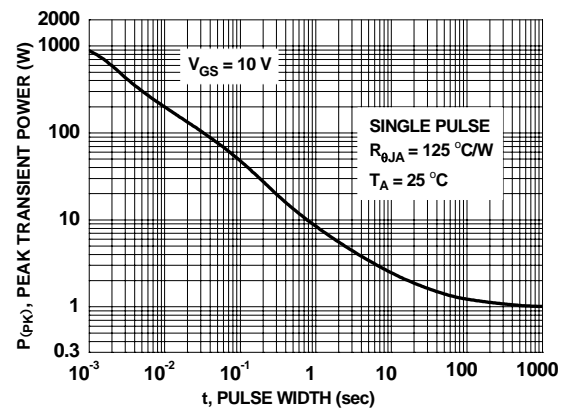
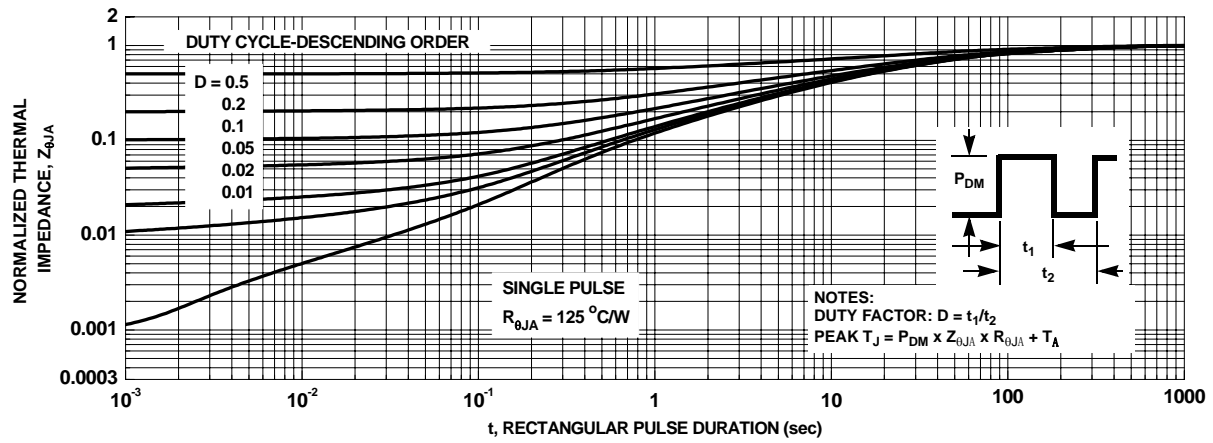


Figure 12. Single Pulse Maximum Power Dissipation



Typical Characteristics $T_J = 25\text{ }^{\circ}\text{C}$ unless otherwise noted







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