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FDMC6296

Single N-Channel Logic-Level Power Trench® MOSFET

30 V, 11.5 A, 10.5 mΩ

Features

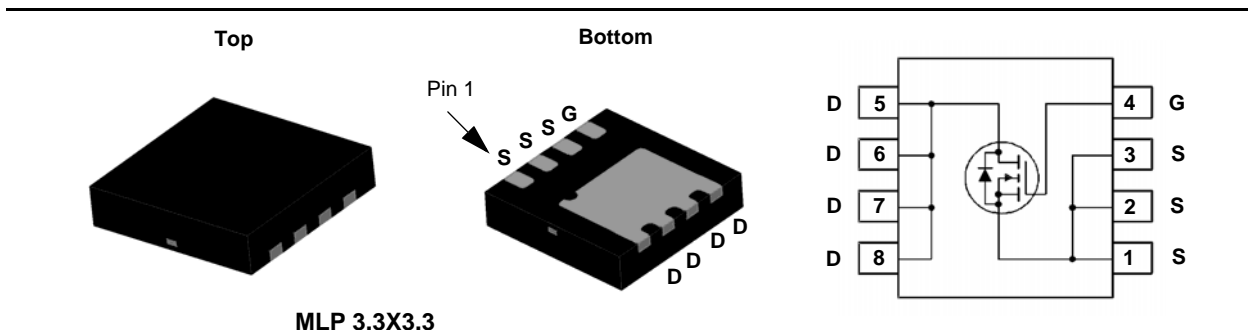
- Max $r_{DS(on)}$ = 10.5 mΩ at $V_{GS} = 10$ V, $I_D = 11.5$ A
- Max $r_{DS(on)}$ = 15 mΩ at $V_{GS} = 4.5$ V, $I_D = 10$ A
- Low Qg, Qgd and Rg for efficient switching performance
- RoHS Compliant

General Description

This single N-Channel MOSFET in the thermally efficient MicroFET Package has been specifically designed to perform well in Point of Load converters. Providing an optimized balance between $r_{DS(on)}$ and gate charge this device can be effectively used as a "high side" control switch or "low side" synchronous rectifier.

Application

- Point of Load Converters
- 1/16 Brick Synchronous Rectifier



MOSFET Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DS}	Drain to Source Voltage	30	V
V_{GS}	Gate to Source Voltage	± 20	V
I_D	Drain Current -Continuous $T_A = 25^\circ\text{C}$ (Note 1a)	11.5	A
	-Pulsed	40	
P_D	Power Dissipation $T_C = 25^\circ\text{C}$	2.1	W
	Power Dissipation $T_A = 25^\circ\text{C}$ (Note 1a)	0.9	
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ\text{C}$

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	(Note 1)	3	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	53	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMC6296	FDMC6296	MLP 3.3X3.3	13 "	12 mm	3000 units

Electrical Characteristics $T_J = 25\text{ }^{\circ}\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250\text{ }\mu\text{A}$, $V_{GS} = 0\text{ V}$	30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$, referenced to $25\text{ }^{\circ}\text{C}$		26		mV/ $^{\circ}\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 24\text{ V}$, $V_{GS} = 0\text{ V}$			1	μA
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 20\text{ V}$, $V_{DS} = 0\text{ V}$			± 100	nA

On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 250\text{ }\mu\text{A}$	1	1.8	3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$, referenced to $25\text{ }^{\circ}\text{C}$		-6		mV/ $^{\circ}\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{ V}$, $I_D = 11.5\text{ A}$		8.7	10.5	m Ω
		$V_{GS} = 4.5\text{ V}$, $I_D = 10\text{ A}$		10.6	15	
		$V_{GS} = 10\text{ V}$, $I_D = 11.5\text{ A}$, $T_J = 125\text{ }^{\circ}\text{C}$		13	17	
g_{FS}	Forward Transconductance	$V_{DD} = 5\text{ V}$, $I_D = 11.5\text{ A}$		49		S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 15\text{ V}$, $V_{GS} = 0\text{ V}$, $f = 1\text{ MHz}$		1610	2141	pF
C_{oss}	Output Capacitance			406	540	pF
C_{rss}	Reverse Transfer Capacitance			150	225	pF
R_g	Gate Resistance	$V_{GS} = 0\text{ V}$, $f = 1\text{ MHz}$		0.9		Ω

Switching Characteristics

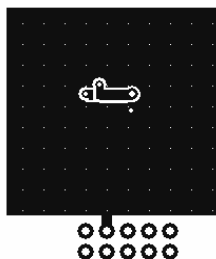
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 15\text{ V}$, $I_D = 1.0\text{ A}$, $V_{GS} = 10\text{ V}$, $R_{GEN} = 6\text{ }\Omega$		10	20	ns
t_r	Rise Time			3	10	ns
$t_{d(off)}$	Turn-Off Delay Time			27	43	ns
t_f	Fall Time			8	16	ns
$Q_{g(TOT)}$	Total Gate Charge at 5V	$V_{GS} = 5\text{ V}$		14	19	nC
Q_{gs}	Total Gate Charge	$V_{DD} = 15\text{ V}$,		4		nC
Q_{gd}	Gate to Drain "Miller" Charge	$I_D = 11.5\text{ A}$		4		nC

Drain-Source Diode Characteristics

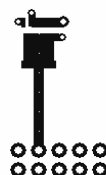
V_{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}$, $I_S = 2\text{ A}$ (Note 2)		0.7	1.2	V
t_{rr}	Reverse Recovery Time	$I_F = 11.5\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$		30		ns
Q_{rr}	Reverse Recovery Charge			22		nC

Notes:

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in^2 pad 2 oz copper pad on a $1.5 \times 1.5\text{ in.}$ board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. $53\text{ }^{\circ}\text{C/W}$ when mounted on a 1 in^2 pad of 2 oz copper



b. $125\text{ }^{\circ}\text{C/W}$ when mounted on a minimum pad of 2 oz copper

2. Pulse Test: Pulse Width $< 300\text{ }\mu\text{s}$, Duty cycle $< 2.0\%$.

Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

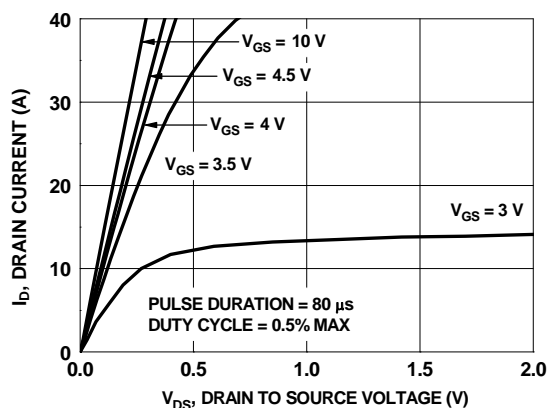


Figure 1. On Region Characteristics

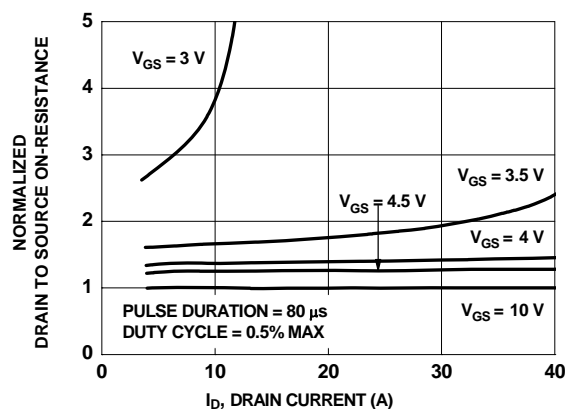


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

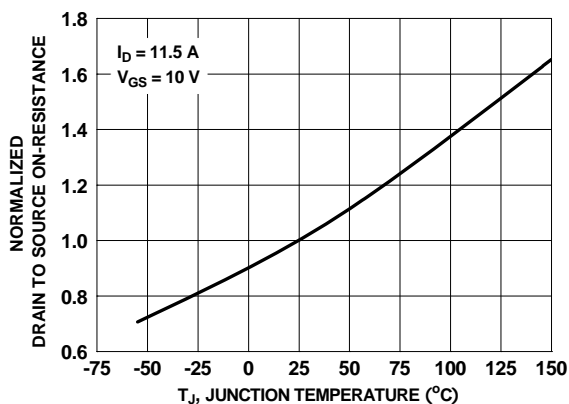


Figure 3. Normalized On Resistance vs Junction Temperature

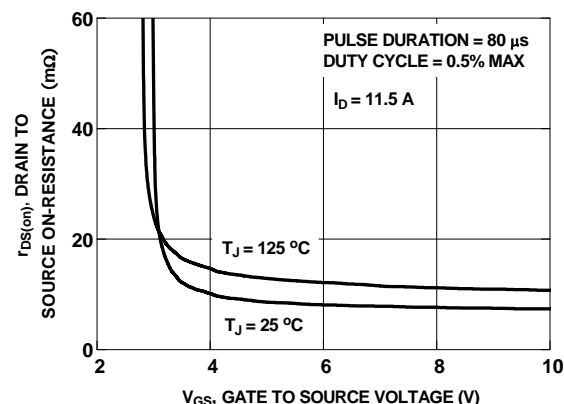


Figure 4. On-Resistance vs Gate to Source Voltage

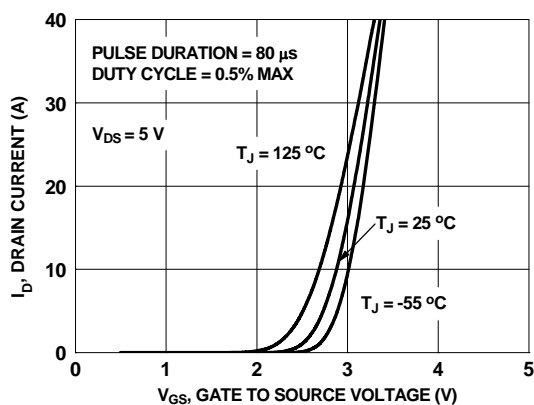


Figure 5. Transfer Characteristics

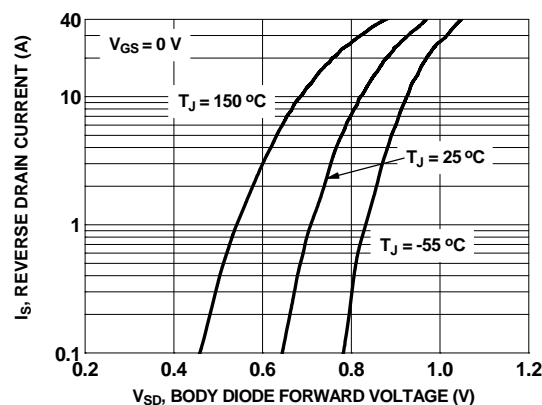


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

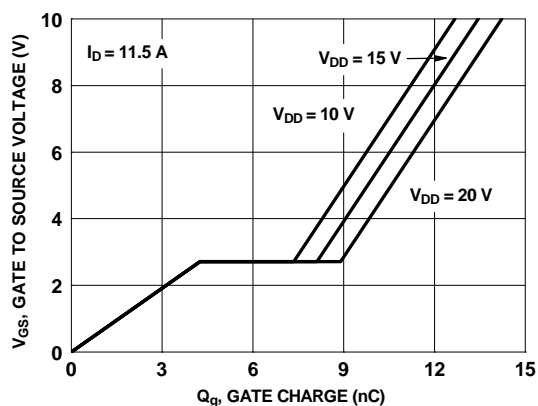


Figure 7. Gate Charge Characteristics

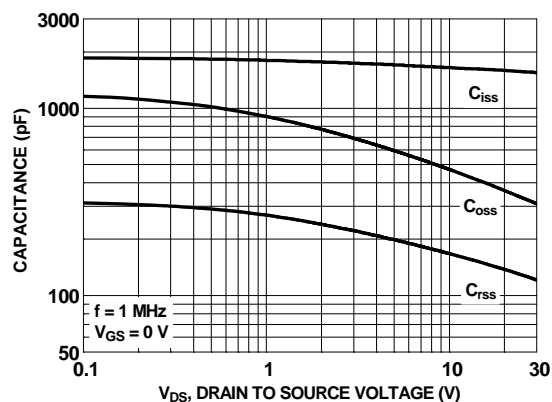


Figure 8. Capacitance vs Drain to Source Voltage

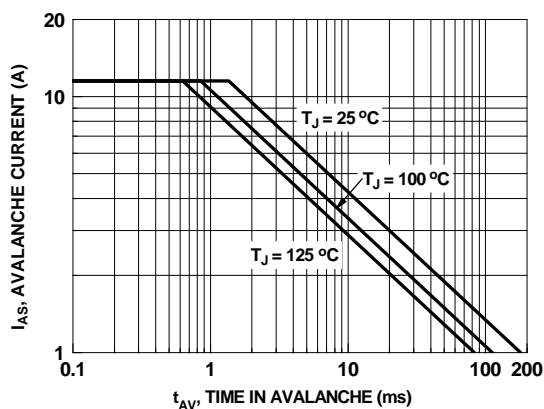


Figure 9. Unclamped Inductive Switching Capability

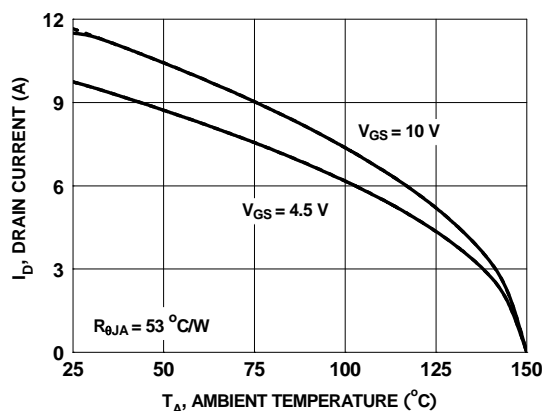


Figure 10. Maximum Continuous Drain Current vs Ambient Temperature

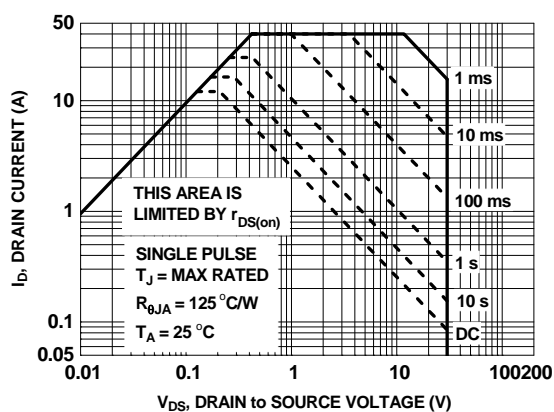


Figure 11. Forward Bias Safe Operating Area

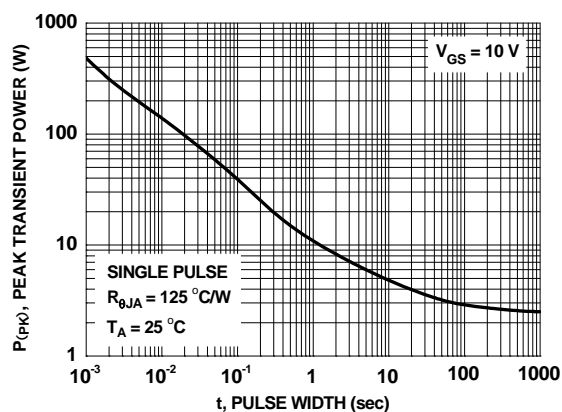


Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

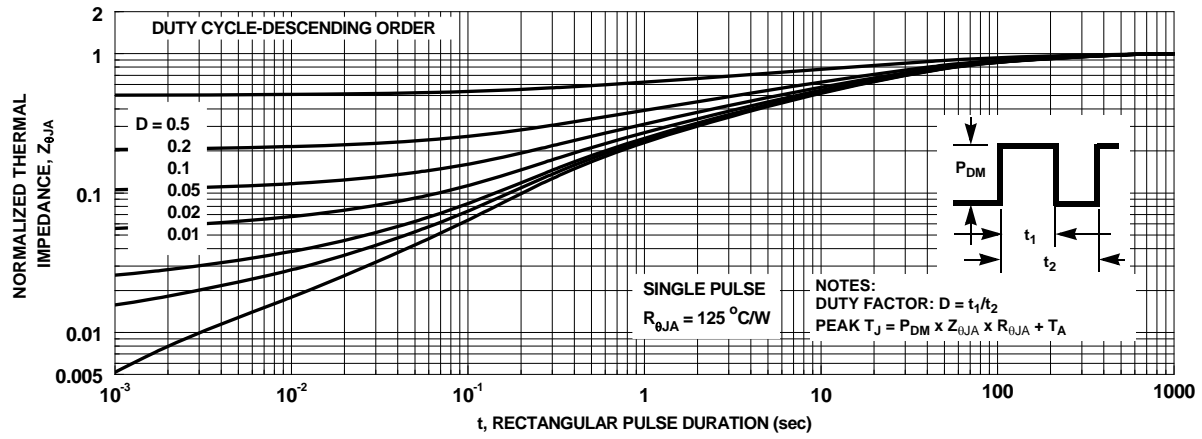
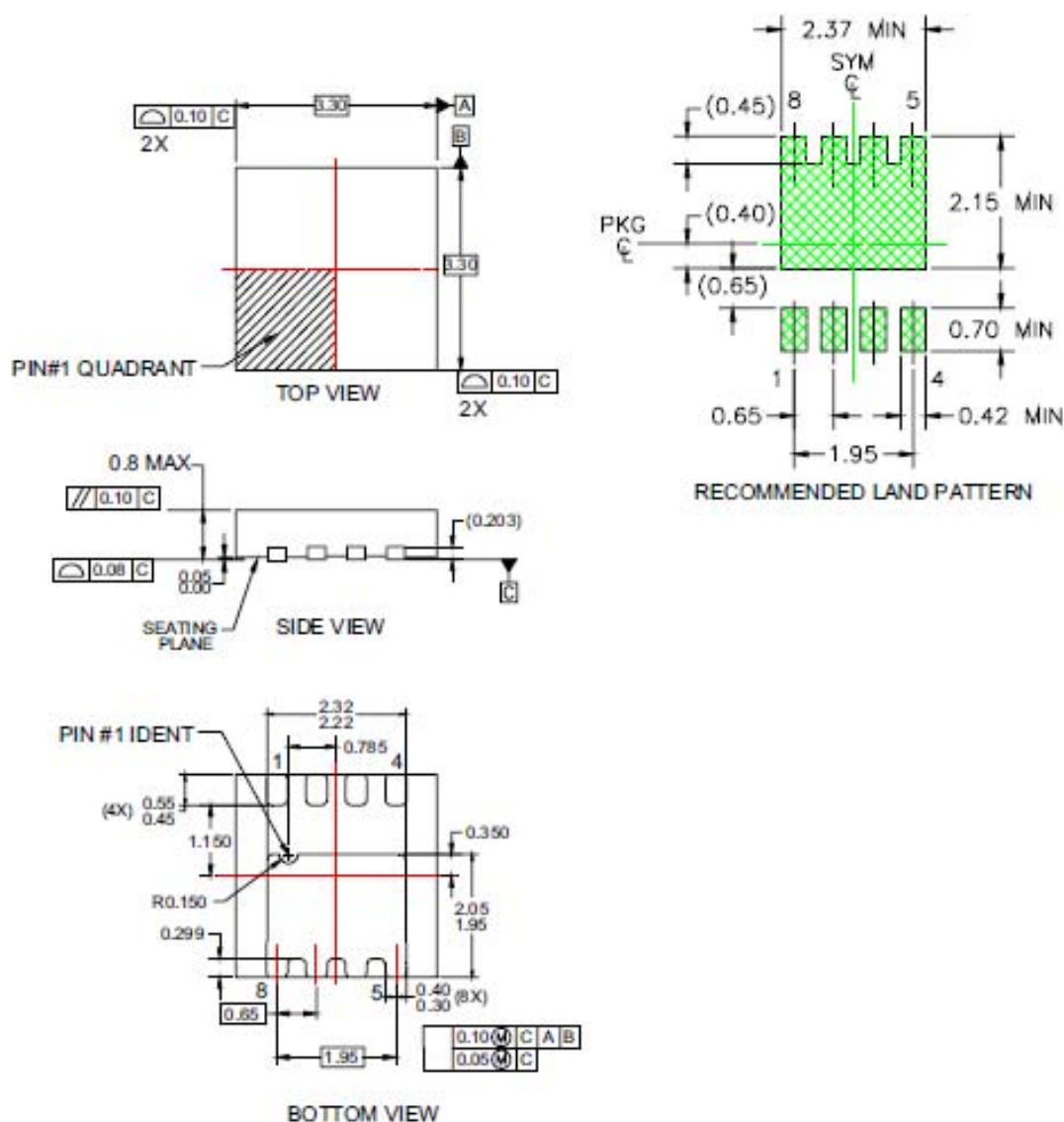


Figure 13. Junction-to-Ambient Transient Thermal Response Curve

Dimensional Outline and Pad Layout



NOTES:

- A. DOES NOT CONFORM TO JEDEC REGISTRATION MO-229
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994
- D. DRAWING FILE NAME : MLP08SREVA
- E. LAND PATTERN RECOMMENDATION IS BASED ON FSC DESIGN ONLY





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No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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