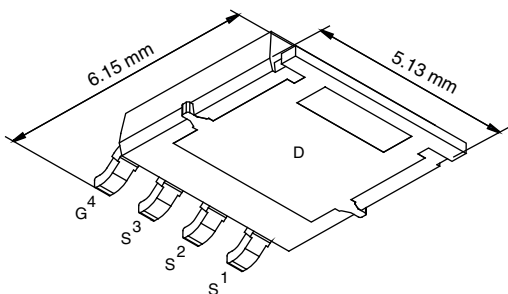




N-Channel 80 V (D-S) MOSFET

PRODUCT SUMMARY

V_{DS} (V)	$R_{DS(on)}$ (Ω) (Max.)	I_D (A) ^{a, g}	Q_g (Typ.)
80	0.0062 at $V_{GS} = 10$ V	60	24 nC
	0.0065 at $V_{GS} = 7.5$ V		
	0.0095 at $V_{GS} = 4.5$ V		

PowerPAK® SO-8L Single

Ordering Information:

SiJ482DP-T1-GE3 (Lead (Pb)-free and Halogen-free)

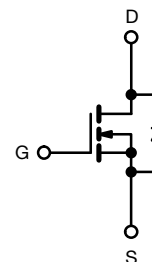
FEATURES

- TrenchFET® Power MOSFET
- 100 % R_g and UIS Tested
- Capable of Operating with 5 V Gate Drive
- Material categorization:
For definitions of compliance please see www.vishay.com/doc?99912


RoHS
 COMPLIANT
 HALOGEN
FREE

APPLICATIONS

- DC/DC Primary Side Switch
- Synchronous Rectification
- High Current Switching



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ($T_A = 25$ °C, unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	80	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current ($T_J = 150$ °C)	$T_C = 25$ °C	60 ^g	A
	$T_C = 70$ °C	60 ^g	
	$T_A = 25$ °C	21.1 ^{b, c}	
	$T_A = 70$ °C	16.9 ^{b, c}	
Pulsed Drain Current ($t = 300$ μ s)	I_{DM}	100	
Continuous Source-Drain Diode Current	$T_C = 25$ °C	60 ^g	
	$T_A = 25$ °C	4.5 ^{b, c}	
Single Pulse Avalanche Current	I_{AS}	30	
Single Pulse Avalanche Energy	E_{AS}	45	mJ
Maximum Power Dissipation	$T_C = 25$ °C	69.4	W
	$T_C = 70$ °C	44.4	
	$T_A = 25$ °C	5 ^{b, c}	
	$T_A = 70$ °C	3.2 ^{b, c}	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to 150	°C
Soldering Recommendations (Peak Temperature) ^{d, e}		260	

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{b, f}	R_{thJA}	20	25	°C/W
Maximum Junction-to-Case (Drain)	R_{thJC}	1.3	1.8	

Notes:

 a. Based on $T_C = 25$ °C.

b. Surface mounted on 1" x 1" FR4 board.

 c. $t = 10$ s.

 d. See solder profile (www.vishay.com/doc?73257). The PowerPAK SO-8L is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.

e. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.

f. Maximum under steady state conditions is 65 °C/W.

g. Package limited.

SiJ482DP

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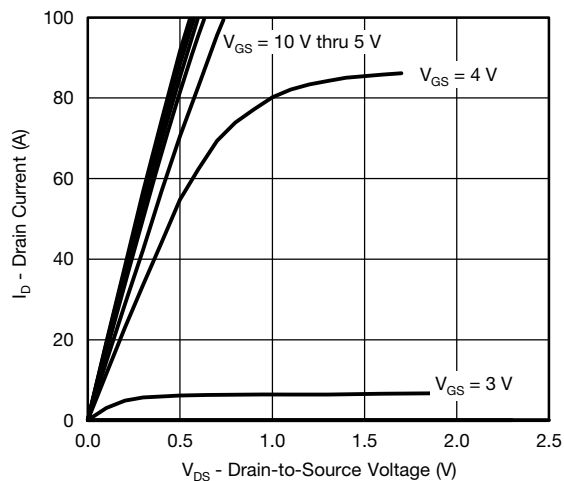
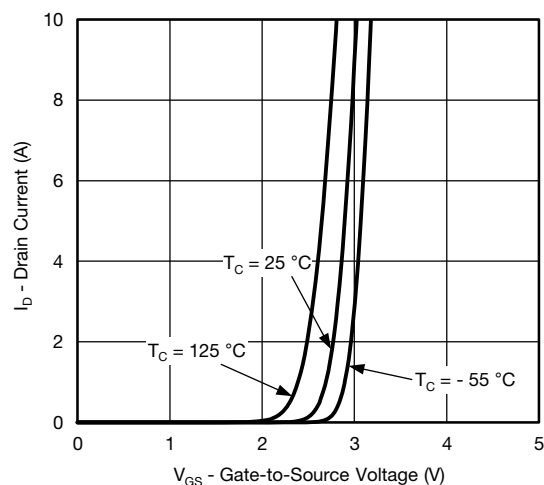
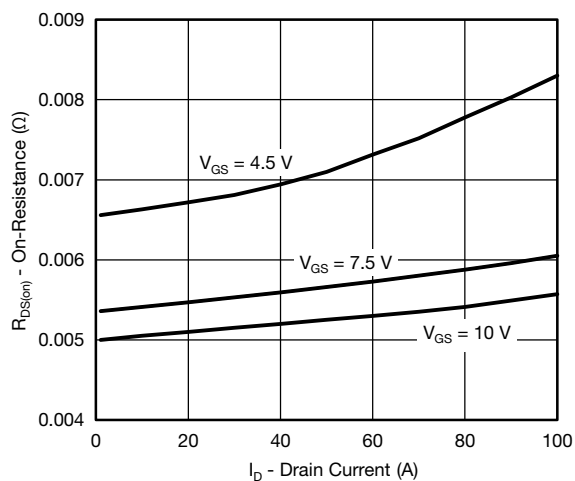
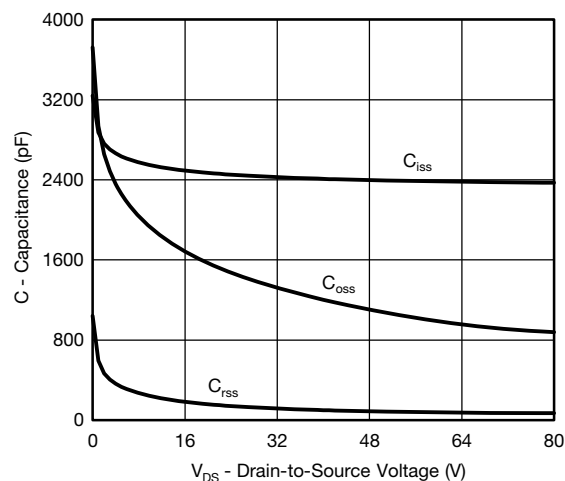
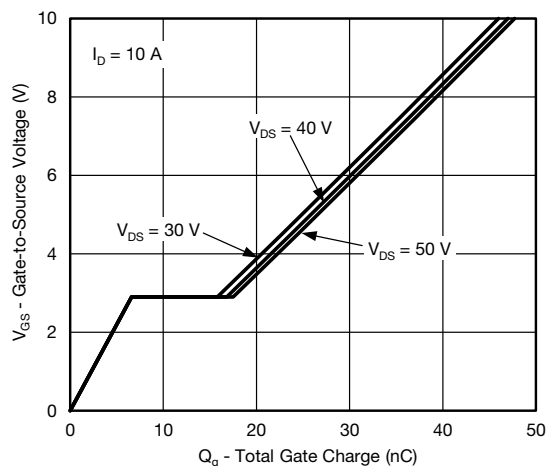
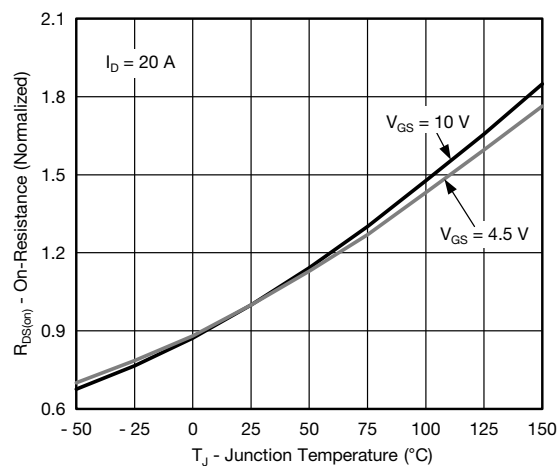
SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA	80			V
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	I _D = 250 μA		36		mV/°C
V _{GS(th)} Temperature Coefficient	ΔV _{GS(th)} /T _J			- 5.7		
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	1.5		2.7	V
Gate-Source Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20 V			± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 80 V, V _{GS} = 0 V			1	μA
		V _{DS} = 80 V, V _{GS} = 0 V, T _J = 55 °C			10	
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = 10 V	30			A
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = 10 V, I _D = 20 A		0.0051	0.0062	Ω
		V _{GS} = 7.5 V, I _D = 15 A		0.0054	0.0065	
		V _{GS} = 4.5 V, I _D = 10 A		0.0068	0.0095	
Forward Transconductance ^a	g _{fs}	V _{DS} = 10 V, I _D = 20 A		68		S
Dynamic ^b						
Input Capacitance	C _{iss}	V _{DS} = 40 V, V _{GS} = 0 V, f = 1 MHz		2425		pF
Output Capacitance	C _{oss}			1180		
Reverse Transfer Capacitance	C _{rss}			100		
Total Gate Charge	Q _g	V _{DS} = 40 V, V _{GS} = 10 V, I _D = 10 A		47	71	nC
		V _{DS} = 40 V, V _{GS} = 7.5 V, I _D = 10 A		36.5	55	
		V _{DS} = 40 V, V _{GS} = 4.5 V, I _D = 10 A		24	36	
			Gate-Source Charge	Q _{gs}		
Gate-Drain Charge	Q _{gd}			10.2		
Output Charge	Q _{oss}	V _{DS} = 40 V, V _{GS} = 0 V		69	105	
Gate Resistance	R _g	f = 1 MHz	0.4	1.1	2.2	Ω
Turn-On Delay Time	t _{d(on)}	V _{DD} = 40 V, R _L = 4 Ω I _D ≅ 10 A, V _{GEN} = 10 V, R _g = 1 Ω		14	28	ns
Rise Time	t _r			11	22	
Turn-Off Delay Time	t _{d(off)}			36	72	
Fall Time	t _f			9	18	
Turn-On Delay Time	t _{d(on)}	V _{DD} = 40 V, R _L = 4 Ω I _D ≅ 10 A, V _{GEN} = 7.5 V, R _g = 1 Ω		16	32	
Rise Time	t _r			13	26	
Turn-Off Delay Time	t _{d(off)}			35	70	
Fall Time	t _f			11	22	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C			60	A
Pulse Diode Forward Current ^a	I _{SM}				100	
Body Diode Voltage	V _{SD}	I _S = 4 A		0.73	1.1	V
Body Diode Reverse Recovery Time	t _{rr}	I _F = 10 A, dI/dt = 100 A/μs, T _J = 25 °C		46	90	ns
Body Diode Reverse Recovery Charge	Q _{rr}			44	86	nC
Reverse Recovery Fall Time	t _a			21		ns
Reverse Recovery Rise Time	t _b			25		

Notes:

a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.

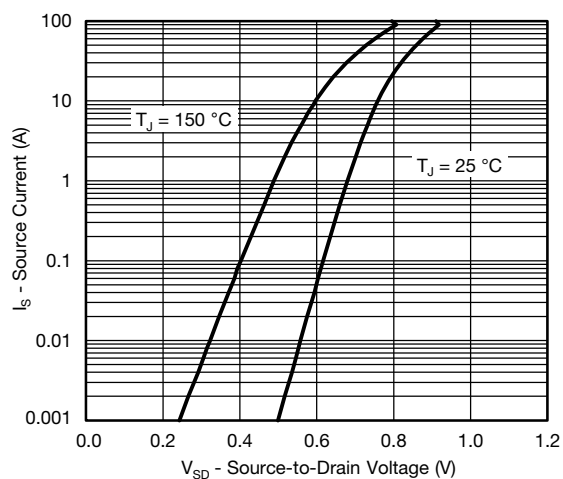
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

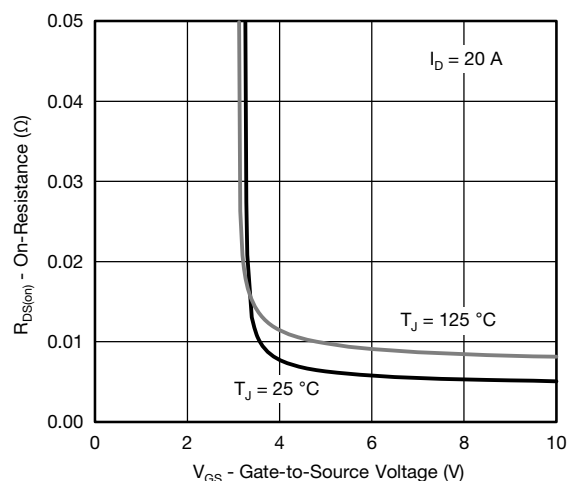

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Output Characteristics

Transfer Characteristics

On-Resistance vs. Drain Current and Gate Voltage

Capacitance

Gate Charge

On-Resistance vs. Junction Temperature

SiJ482DP

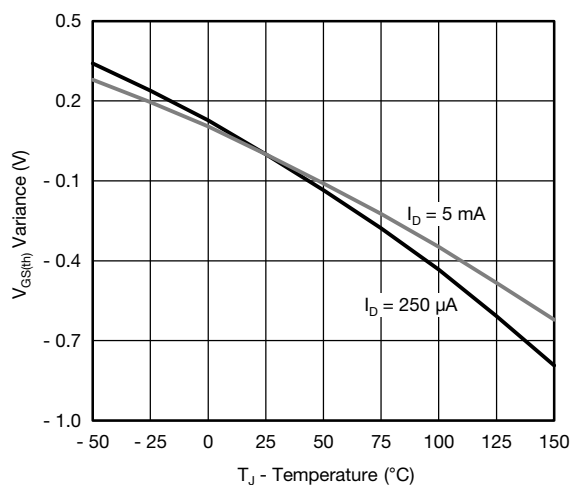
Vishay Siliconix

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

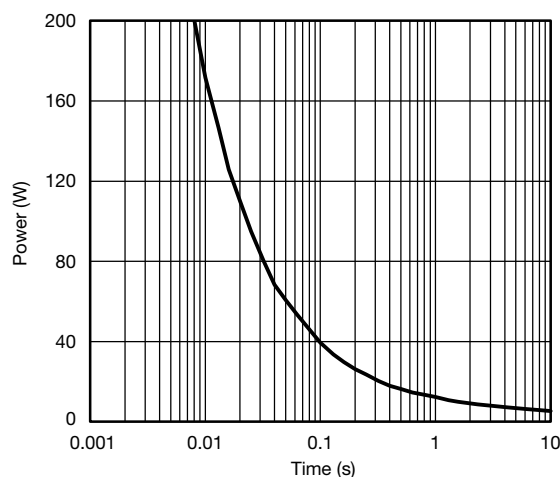
Source-Drain Diode Forward Voltage



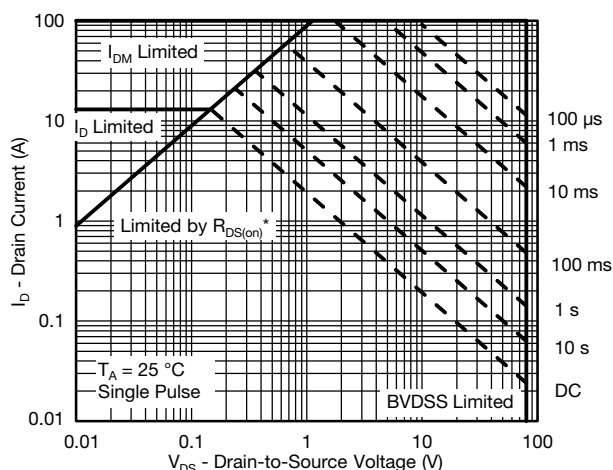
On-Resistance vs. Gate-to-Source Voltage



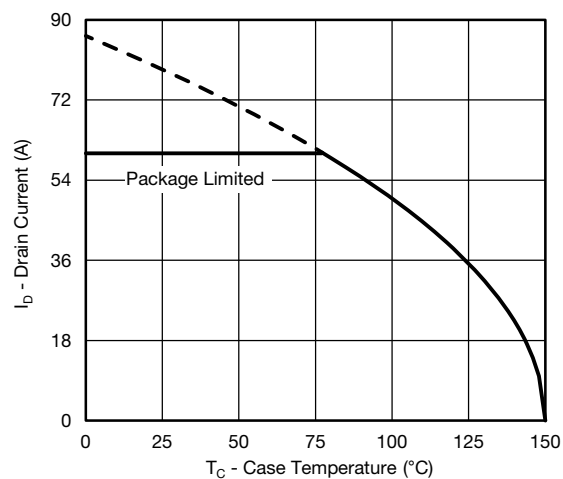
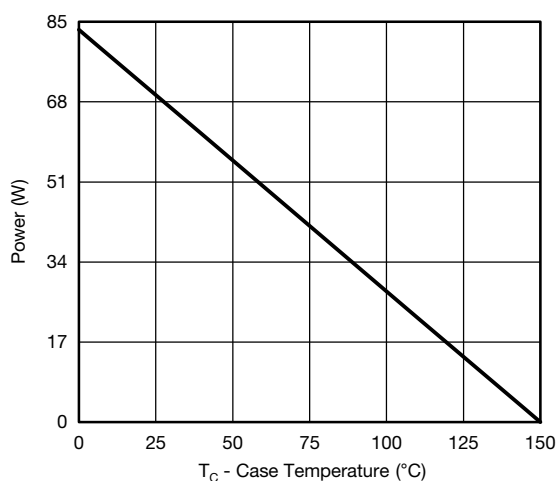
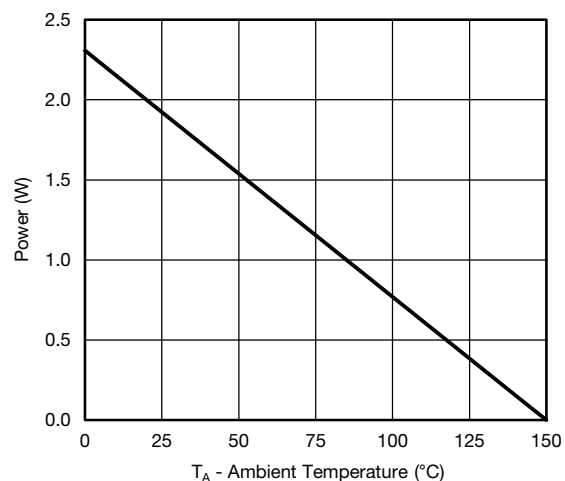
Threshold Voltage



Single Pulse Power, Junction-to-Ambient

* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

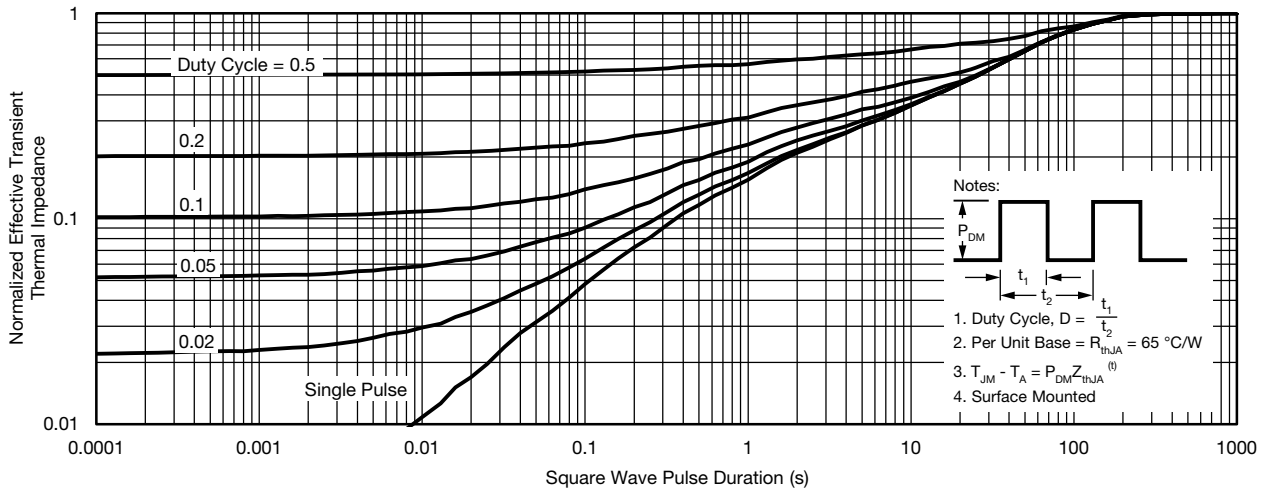
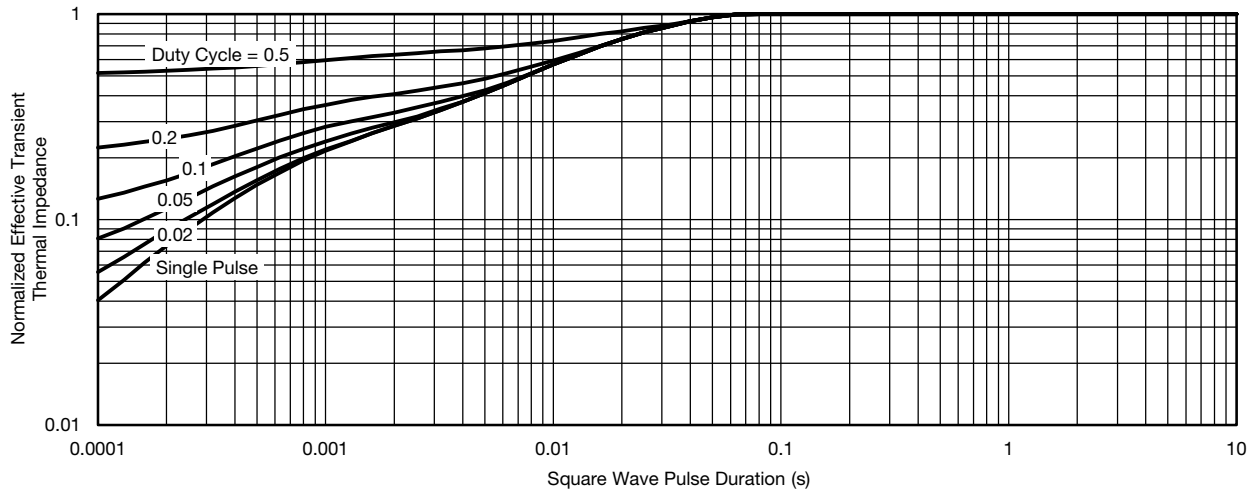
Safe Operating Area, Junction-to-Ambient


TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Current Derating*

Power, Junction-to-Case

Power, Junction-to-Ambient

* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

SiJ482DP

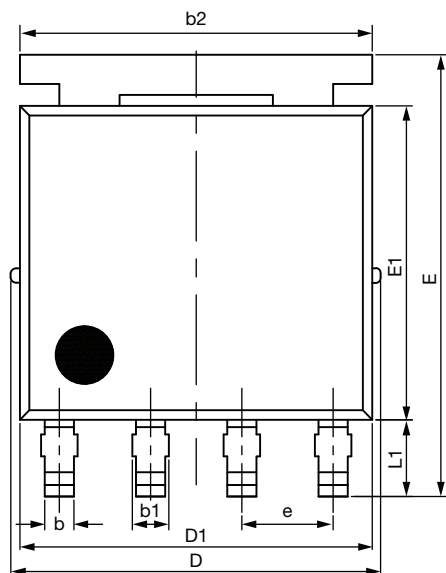
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**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)**Normalized Thermal Transient Impedance, Junction-to-Ambient****Normalized Thermal Transient Impedance, Junction-to-Case**

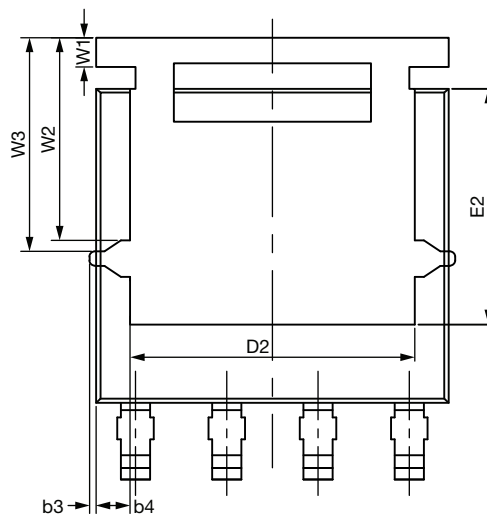
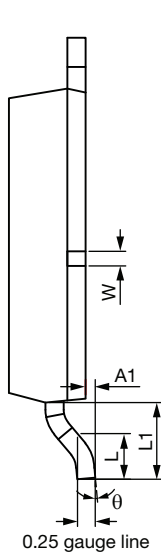
Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?63728.



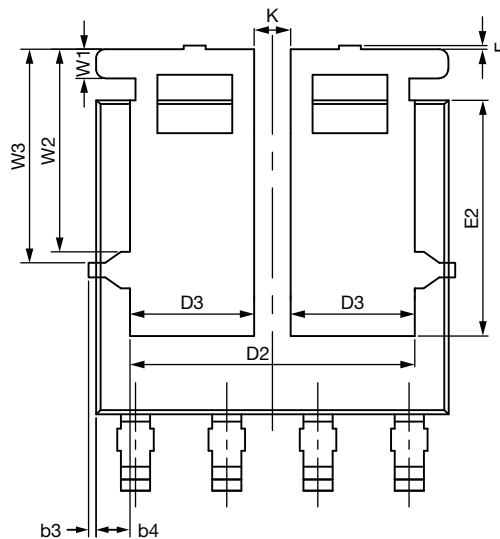
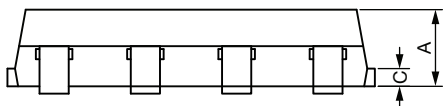
PowerPAK® SO-8L Case Outline for Non-AI Parts



Topside view



Backside view (single)



Backside view (dual)



DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	1.00	1.07	1.14	0.039	0.042	0.045
A1	0.00	-	0.127	0.00	-	0.005
b	0.33	0.41	0.48	0.013	0.016	0.019
b1	0.44	0.51	0.58	0.017	0.020	0.023
b2	4.80	4.90	5.00	0.189	0.193	0.197
b3	0.094			0.004		
b4	0.47			0.019		
c	0.20	0.25	0.30	0.008	0.010	0.012
D	5.00	5.13	5.25	0.197	0.202	0.207
D1	4.80	4.90	5.00	0.189	0.193	0.197
D2	3.86	3.96	4.06	0.152	0.156	0.160
D3	1.63	1.73	1.83	0.064	0.068	0.072
e	1.27 BSC			0.050 BSC		
E	6.05	6.15	6.25	0.238	0.242	0.246
E1	4.27	4.37	4.47	0.168	0.172	0.176
E2	3.18	3.28	3.38	0.125	0.129	0.133
F	-	-	0.15	-	-	0.006
L	0.62	0.72	0.82	0.024	0.028	0.032
L1	0.92	1.07	1.22	0.036	0.042	0.048
K	0.51			0.020		
W	0.23			0.009		
W1	0.41			0.016		
W2	2.82			0.111		
W3	2.96			0.117		
θ	0°	-	10°	0°	-	10°
ECN: T16-0221-Rev. D, 16-May-16						
DWG: 5976						

Note

- Millimeters will govern



RECOMMENDED MINIMUM PAD FOR PowerPAK® SO-8L SINGLE



Recommended Minimum Pads
Dimensions in mm (inches)



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