

N-Channel 30-V (D-S) MOSFET

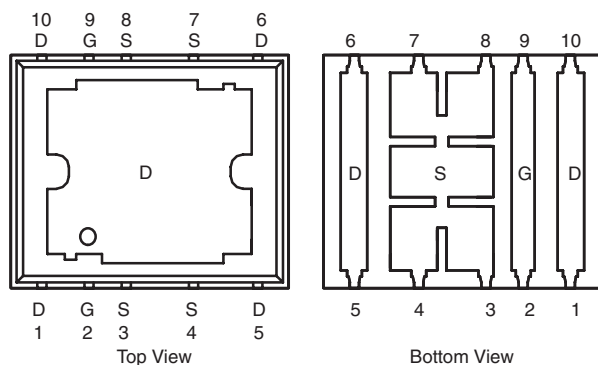
PRODUCT SUMMARY

V_{DS} (V)	$R_{DS(on)}$ (Ω) ^e	I_D (A)		Q_g (Typ.)
		Silicon Limit	Package Limit	
30	0.0017 at $V_{GS} = 10$ V	202	60	75 nC
	0.0021 at $V_{GS} = 4.5$ V	187	60	

Package Drawing

www.vishay.com/doc?72945

PolarPAK



Top surface is connected to pins 1, 5, 6, and 10

Ordering Information: SiE806DF-T1-E3 (Lead (Pb)-free)
SiE806DF-T1-GE3 (Lead (Pb)-free and Halogen-free)

FEATURES

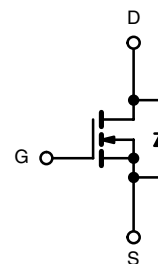
- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET[®] Gen II Power MOSFET
- Ultra Low Thermal Resistance Using Top-Exposed PolarPAK[®] Package for Double-Sided Cooling
- Leadframe-Based New Encapsulated Package
 - Die Not Exposed
 - Same Layout Regardless of Die Size
- Low Q_{gd}/Q_{gs} Ratio Helps Prevent Shoot-Through
- 100 % R_g and UIS Tested
- Compliant to RoHS directive 2002/95/EC



RoHS
COMPLIANT
HALOGEN
FREE
Available

APPLICATIONS

- VRM
- DC/DC Conversion: Low-Side
- Synchronous Rectification



N-Channel MOSFET

For Related Documents
www.vishay.com/ppg?73740

ABSOLUTE MAXIMUM RATINGS $T_A = 25$ °C, unless otherwise noted

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	30	V
Gate-Source Voltage	V_{GS}	± 12	V
Continuous Drain Current ($T_J = 150$ °C)	I_D	$T_C = 25$ °C	202 (Silicon Limit)
		$T_C = 70$ °C	60 ^a (Package Limit)
		$T_A = 25$ °C	60 ^a
		$T_A = 70$ °C	41.3 ^{b, c}
Pulsed Drain Current	I_{DM}	100	A
Continuous Source-Drain Diode Current	I_S	$T_C = 25$ °C	60 ^a
		$T_A = 25$ °C	4.3 ^{b, c}
Single Pulse Avalanche Current	I_{AS}	50	A
Avalanche Energy	E_{AS}	125	mJ
Maximum Power Dissipation	P_D	$T_C = 25$ °C	125
		$T_C = 70$ °C	80
		$T_A = 25$ °C	5.2 ^{b, c}
		$T_A = 70$ °C	3.3 ^{b, c}
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to 150	°C
Soldering Recommendations (Peak Temperature) ^{d, e}		260	

Notes:

a. Package limited is 60 A.

b. Surface Mounted on 1" x 1" FR4 board.

c. $t = 10$ s.

d. See Solder Profile (www.vishay.com/doc?73257). The PolarPAK is a leadless package. The end of the lead terminal is exposed copper not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.

e. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

THERMAL RESISTANCE RATINGS

Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{a, b}	$t \leq 10$ s	R_{thJA}	20	24	°C/W
Maximum Junction-to-Case (Drain Top)	Steady State	R_{thJC} (Drain)	0.8	1	
Maximum Junction-to-Case (Source) ^{a, c}		R_{thJFC} (Source)	2.2	2.7	

Notes:

a. Surface Mounted on 1" x 1" FR4 board.

b. Maximum under Steady State conditions is 68 °C/W.

c. Measured at source pin (on the side of the package).

SPECIFICATIONS $T_J = 25$ °C, unless otherwise noted

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}$, $I_D = 250\text{ }\mu\text{A}$	30			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = 250\text{ }\mu\text{A}$		29		mV/°C
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			- 5.1		
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	0.6	1.3	2	V
Gate-Source Leakage	I_{GSS}	$V_{DS} = 0\text{ V}$, $V_{GS} = \pm 12\text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 30\text{ V}$, $V_{GS} = 0\text{ V}$			1	μA
		$V_{DS} = 30\text{ V}$, $V_{GS} = 0\text{ V}$, $T_J = 55\text{ }^\circ\text{C}$			10	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}$, $V_{GS} = 10\text{ V}$	25			A
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$, $I_D = 25\text{ A}$		0.0014	0.0017	Ω
		$V_{GS} = 4.5\text{ V}$, $I_D = 25\text{ A}$		0.0017	0.0021	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 15\text{ V}$, $I_D = 25\text{ A}$		130		S
Dynamic ^b						
Input Capacitance	C_{iss}	$V_{DS} = 15\text{ V}$, $V_{GS} = 0\text{ V}$, $f = 1\text{ MHz}$		13000		pF
Output Capacitance	C_{oss}			1150		
Reverse Transfer Capacitance	C_{rss}			550		
Total Gate Charge	Q_g	$V_{DS} = 15\text{ V}$, $V_{GS} = 10\text{ V}$, $I_D = 20\text{ A}$		165	250	nC
		$V_{DS} = 15\text{ V}$, $V_{GS} = 4.5\text{ V}$, $I_D = 20\text{ A}$		75	115	
Gate-Source Charge	Q_{gs}			23		
Gate-Drain Charge	Q_{gd}			9.5		
Gate Resistance	R_g	$f = 1\text{ MHz}$		0.9	1.35	Ω
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 15\text{ V}$, $R_L = 1.5\text{ }\Omega$ $I_D \cong 10\text{ A}$, $V_{GEN} = 4.5\text{ V}$, $R_g = 1\text{ }\Omega$		125	190	ns
Rise Time	t_r			160	240	
Turn-Off Delay Time	$t_{d(off)}$			85	130	
Fall Time	t_f			15	25	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 15\text{ V}$, $R_L = 1.5\text{ }\Omega$ $I_D \cong 10\text{ A}$, $V_{GEN} = 10\text{ V}$, $R_g = 1\text{ }\Omega$		20	30	
Rise Time	t_r			50	75	
Turn-Off Delay Time	$t_{d(off)}$			85	130	
Fall Time	t_f			10	15	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	$T_C = 25\text{ }^\circ\text{C}$			60	A
Pulse Diode Forward Current ^a	I_{SM}				100	
Body Diode Voltage	V_{SD}	$I_S = 10\text{ A}$		0.9	1.2	V
Body Diode Reverse Recovery Time	t_{rr}	$I_F = 10\text{ A}$, $dI/dt = 100\text{ A}/\mu\text{s}$, $T_J = 25\text{ }^\circ\text{C}$		52	80	ns
Body Diode Reverse Recovery Charge	Q_{rr}			55	105	nC
Reverse Recovery Fall Time	t_a			25		ns
Reverse Recovery Rise Time	t_b			27		

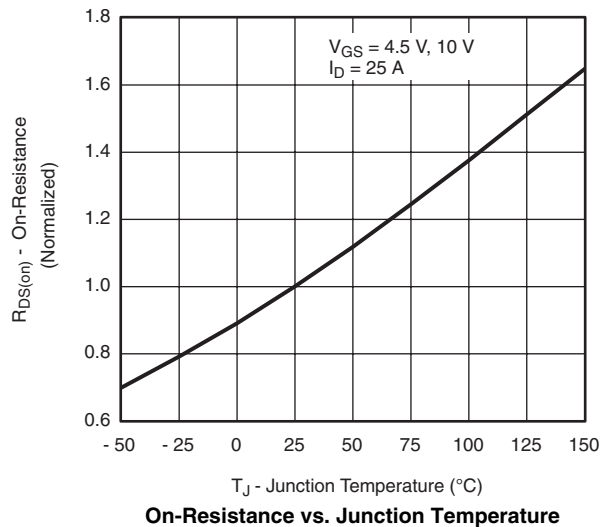
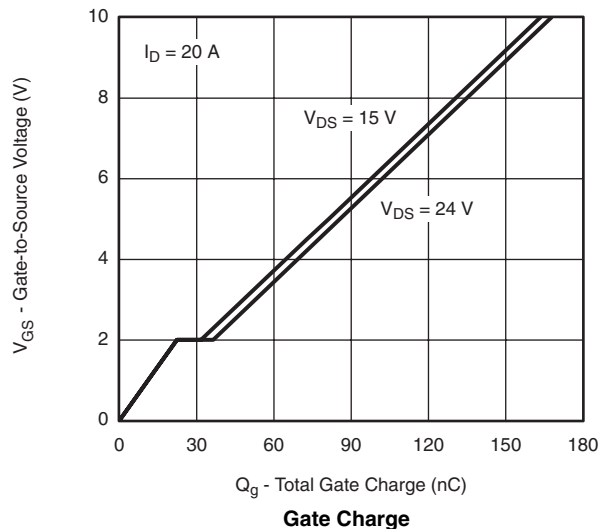
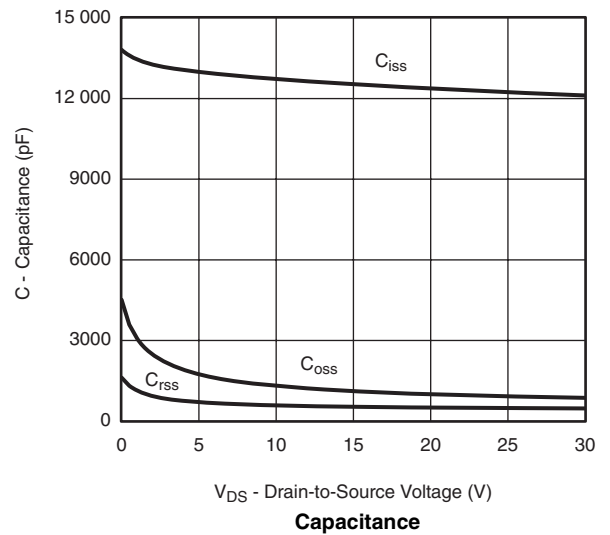
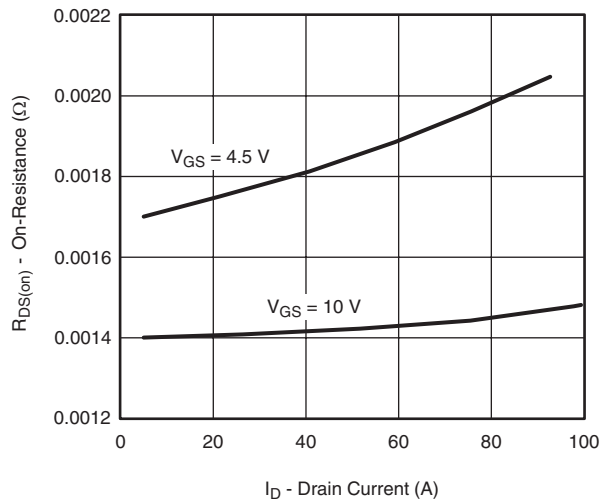
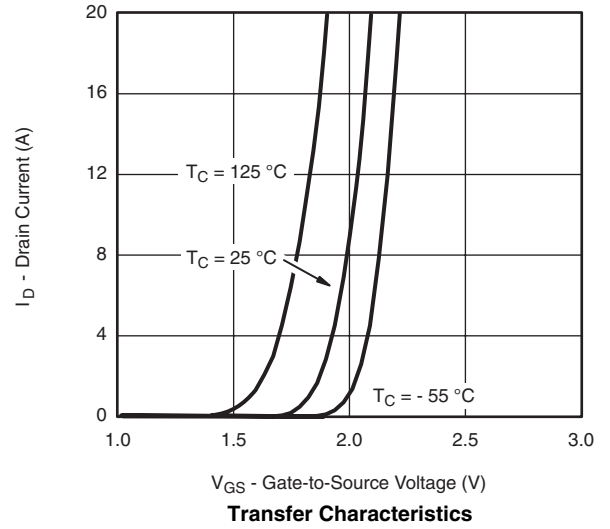
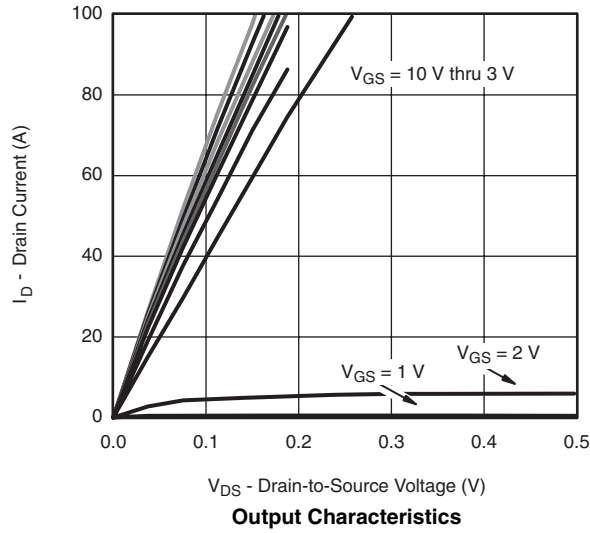
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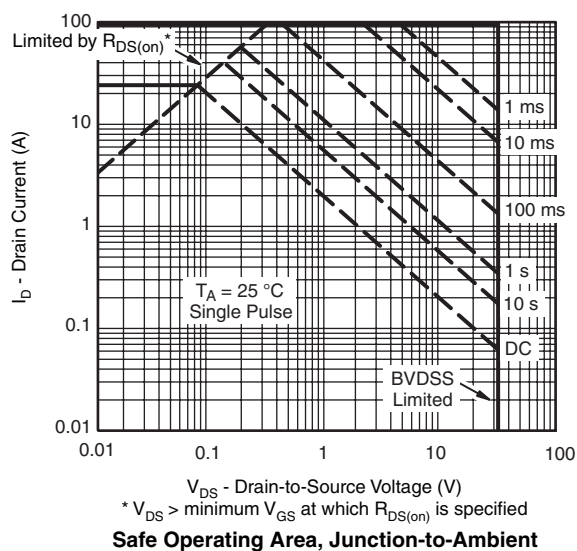
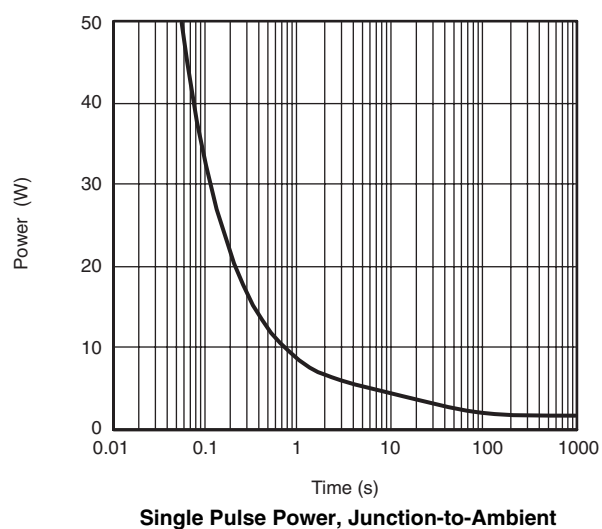
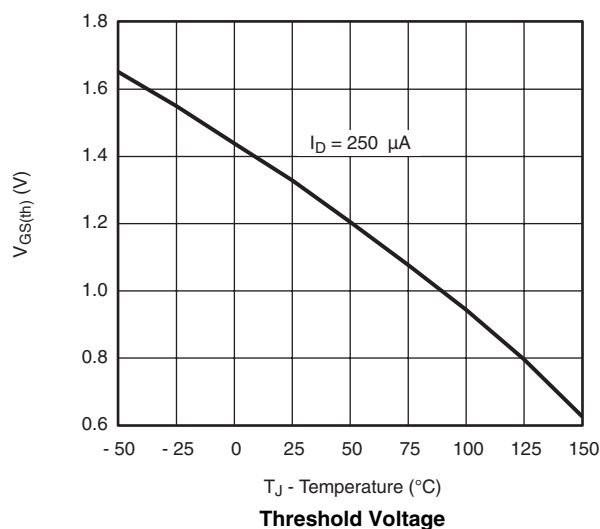
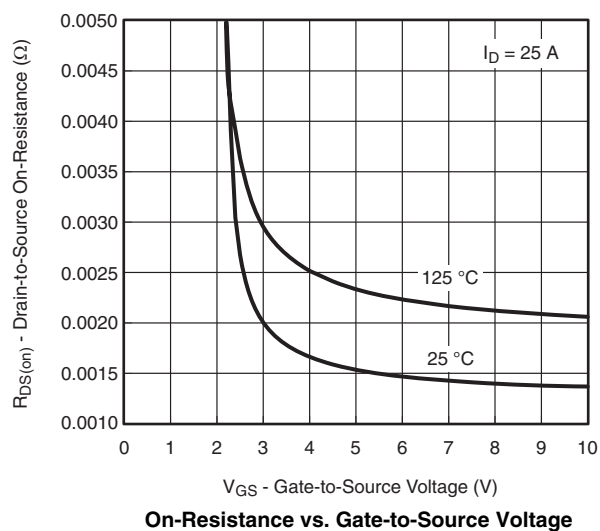
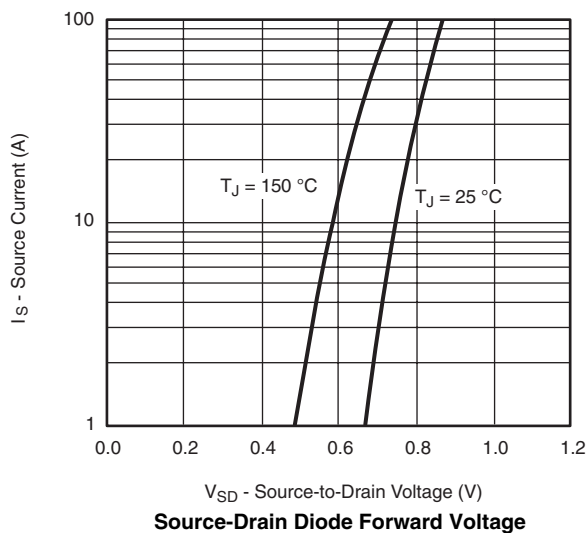
a. Pulse test; pulse width ≤ 300 μ s, duty cycle ≤ 2 %.

b. Guaranteed by design, not subject to production testing.

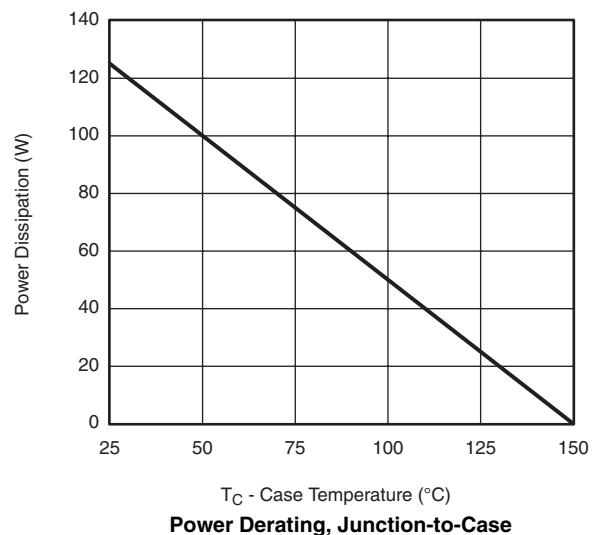
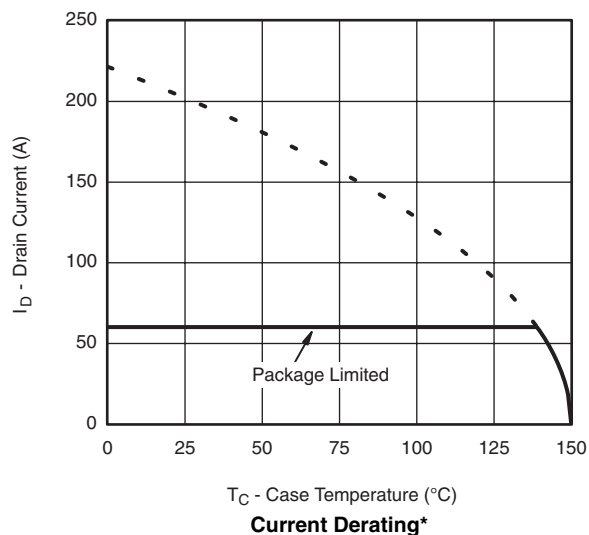
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

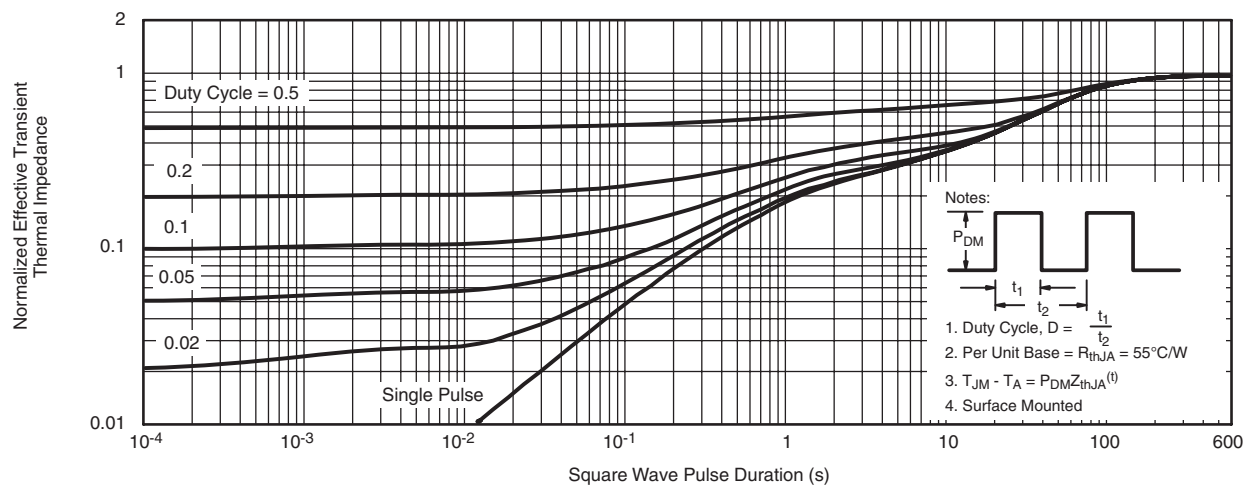
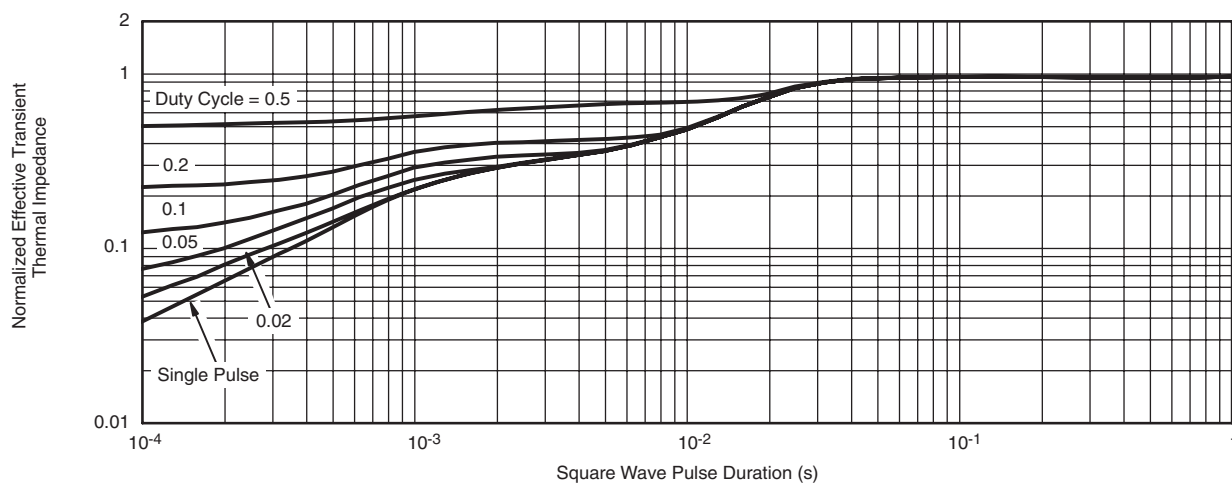
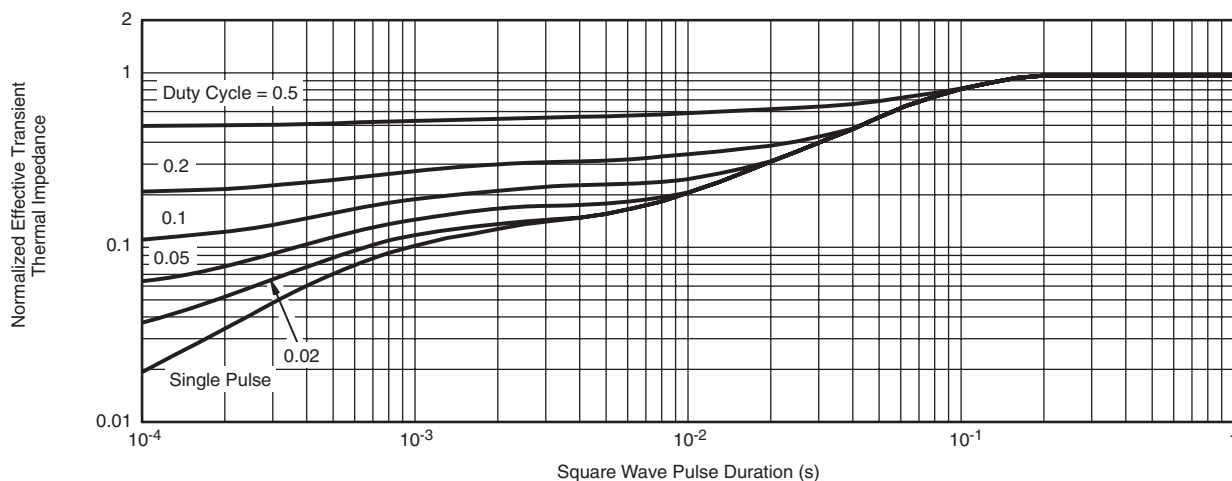


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* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted**Normalized Thermal Transient Impedance, Junction-to-Ambient****Normalized Thermal Transient Impedance, Junction-to-Case (Drain Top)****Normalized Thermal Transient Impedance, Junction-to-Source**

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