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October 2008

# FDS4559\_F085

# 60V Complementary PowerTrench®MOSFET

# **General Description**

This complementary MOSFET device is produced using Fairchild's advanced PowerTrench process that has been especially tailored to minimize the on-state resistance and yet maintain low gate charge for superior switching performance.

# **Applications**

- DC/DC converter
- · Power management
- LCD backlight inverter



### **Features**

• Q1: N-Channel

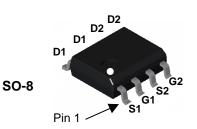
4.5 A, 60 V 
$$R_{DS(on)} = 55 \text{ m}\Omega @ V_{GS} = 10V$$
 
$$R_{DS(on)} = 75 \text{ m}\Omega @ V_{GS} = 4.5V$$

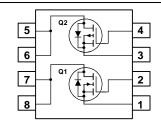
Q2: P-Channel

$$-3.5 \text{ A}, -60 \text{ V} \text{ R}_{DS(on)} = 105 \text{ m}\Omega \text{ @ V}_{GS} = -10 \text{V}$$

$$R_{DS(on)} = 135 \text{ m}\Omega @ V_{GS} = -4.5V$$

- Qualified to AEC Q101
- RoHS Compliant





# Absolute Maximum Ratings T<sub>A</sub> = 25°C unless otherwise noted

Symbol	Parameter		Q1	Q2	Units
V <sub>DSS</sub>	Drain-Source Voltage		60	-60	V
V <sub>GSS</sub>	Gate-Source Voltage		±20	±20	V
I <sub>D</sub>	Drain Current - Continuous	(Note 1a)	4.5	-3.5	Α
	- Pulsed		20	-20	
P <sub>D</sub>	Power Dissipation for Dual Operation		2	2	W
	Power Dissipation for Single Operation	(Note 1a)	1.	.6	
		(Note 1b)	1.	.2	
		(Note 1c)	:	2	
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Junction Temperature Range		-55 to	+150	°C

### **Thermal Characteristics**

R <sub>θJA</sub>	Thermal Resistance, Junction-to-Ambient	(Note 1a)	78	°C/W
R <sub>θJC</sub>	Thermal Resistance, Junction-to-Case	(Note 1)	40	°C/W

**Package Marking and Ordering Information** 

Device Marking	Device	Reel Size	Tape width	Quantity
FDS4559	FDS4559_F085	13"	12mm	2500 units

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<b>Symbol</b>	Parameter	Test Conditions	Type	Min	Тур	Max	Units
Drain-So	ource Avalanche Rating	QS (Note 1)			•		•
W <sub>DSS</sub>	Single Pulse Drain-Source Avalanche Energy	$V_{DD} = 30 \text{ V}, \qquad I_{D} = 4.5 \text{ A}$	Q1			90	mJ
I <sub>AR</sub>	Maximum Drain-Source Avalanche Current		Q1			4.5	А
Off Cha	racteristics						
BV <sub>DSS</sub>	Drain-Source Breakdown	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	Q1	60			V
	Voltage	$V_{GS} = 0 \text{ V}, I_{D} = -250 \mu\text{A}$	Q2	-60			
∆BV <sub>DSS</sub>	Breakdown Voltage	$I_D = 250 \mu\text{A}$ , Referenced to 25°C	Q1		58		mV/°C
ΔTJ	Temperature Coefficient	$I_D = -250 \mu\text{A}$ , Referenced to 25°C	Q2		-49		
I <sub>DSS</sub>	Zero Gate Voltage Drain	$V_{DS} = 48 \text{ V}, V_{GS} = 0 \text{ V}$	Q1 Q2			1	μΑ
ı	Current Gate-Body Leakage	$V_{DS} = -48 \text{ V}, V_{GS} = 0 \text{ V}$ $V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$	Q2 Q1			-1	nA
GSS	Gate-Body Leakage	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$ $V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$	Q2			<u>+</u> 100 +100	IIA
0 01	4 • 4•	VGS - <u>1</u> 20 V, VDS - 0 V	QZ			1100	
	racteristics (Note 2)	Tu					
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250 \mu\text{A}$	Q1	1	2.2	3	V
$\Delta V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$ , $I_D = -250 \mu A$ $I_D = 250 \mu A$ , Referenced to 25°C	Q2 Q1	<u>–1</u>	-1.6 -5.5	-3	mV/°C
$\Delta V_{GS(th)}$ $\Delta T_J$	Temperature Coefficient	$I_D = 250 \mu\text{A}$ , Referenced to 25°C $I_D = -250 \mu\text{A}$ , Referenced to 25°C	Q2		-3.5 4		mv/°C
R <sub>DS(on)</sub>	Static Drain-Source	$V_{GS} = 10 \text{ V}, I_D = 4.5 \text{ A}$	Q1		42	55	mΩ
VDS(on)	On-Resistance	$V_{GS} = 10 \text{ V}, I_{D} = 4.5 \text{ A}, T_{J} = 125^{\circ}\text{C}$	Q I		72	94	11152
					55	75	
		$V_{GS} = 4.5 \text{ V}, I_D = 4 \text{ A}$ $V_{GS} = -10 \text{ V}, I_D = -3.5 \text{ A}$	Q2		82	105	
		$V_{GS} = -10 \text{ V}, I_D = -3.5 \text{ A}, T_J = 125^{\circ}\text{C}$	Q		130	190	
					105	135	
I <sub>D(on)</sub>	On-State Drain Current	$V_{GS} = -4.5 \text{ V}, I_D = -3.1 \text{ A}$ $V_{GS} = 10 \text{ V}, V_{DS} = 5 \text{ V}$	Q1	20			Α
5(0.1)		$V_{GS} = -10 \text{ V}, V_{DS} = -5 \text{ V}$	Q2	-20			
g <sub>FS</sub>	Forward Transconductance	$V_{GS} = -10 \text{ V}, V_{DS} = -5 \text{ V}$ $V_{DS} = 10 \text{ V}, I_D = 4.5 \text{ A}$	Q1		14		S
		$V_{DS} = -5 \text{ V}, I_{D} = -3.5 \text{ A}$	Q2		9		
Dynami	c Characteristics						
Ciss	Input Capacitance	Q1	Q1		650		pF
		$V_{DS} = 25 \text{ V}, V_{GS} = 0 \text{ V},$	Q2		759		
Coss	Output Capacitance	f = 1.0 MHz	Q1		80		pF
		Q2	Q2		90		
$C_{rss}$	Reverse Transfer	$V_{DS} = -30 \text{ V}, V_{GS} = 0 \text{ V},$ f = 1.0  MHz	Q1		35		pF
	Capacitance	1 = 1.0 WH 12	Q2		39		
witchin	g Characteristics (Note 2	2)					
	Turn-On Delay Time	Q1	Q1		11	20	ns
(OII)	· · · · · · · · · · · · · · · · · · ·	$V_{DD} = 30 \text{ V}, I_D = 1 \text{ A},$	Q2		7	14	
	Turn-On Rise Time	$V_{GS} = 10V$ , $R_{GEN} = 6 \Omega$	Q1		8	18	ns
			Q2		10	20	
(off)	Turn-Off Delay Time	Q2	Q1		19	35	ns
		$V_{DD} = -30 \text{ V}, I_D = -1 \text{ A},$	Q2		19	34	
	Turn-Off Fall Time	$V_{GS} = -10 \text{ V}, R_{GEN} = 6 \Omega$	Q1		6	15	ns
	T / 10 / 01		Q2		12	22	<u> </u>
l <sub>g</sub>	Total Gate Charge	Q1	Q1		12.5	18	nC
	2-1- 2	$V_{DS} = 30 \text{ V}, I_{D} = 4.5 \text{ A}, V_{GS} = 10 \text{ V}$	Q2		15	21	
gs	Gate-Source Charge	Q2	Q1		2.4		nC
	Gate-Drain Chargo	$V_{DS} = -30 \text{ V}, I_{D} = -3.5 \text{ A}, V_{GS} = -10 \text{ V}$	Q2		2.5		nC
gd	Gate-Drain Charge	1.03 . 33 1, 10 = 3.071, 165 = 101	Q1 Q2		2.6 3.0		IIC

# **Electrical Characteristics** (continued) T<sub>A</sub> = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Туре	Min	Тур	Max	Units	
Drain-Source Diode Characteristics and Maximum Ratings								
Is	Maximum Continuous Drain-Source Diode Forward Current					1.3	Α	
			Q2			-1.3		
V <sub>SD</sub>	Drain-Source Diode Forward	$V_{GS} = 0 \text{ V}, I_S = 1.3 \text{ A} \text{ (Note 2)}$ $V_{GS} = 0 \text{ V}, I_S = -1.3 \text{ A} \text{ (Note 2)}$	Q1		0.8	1.2	V	
	Voltage	$V_{GS} = 0 \text{ V}, I_{S} = -1.3 \text{ A}$ (Note 2)	Q2		-0.8	-1.2		

1. R<sub>BJA</sub> is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



a) 78°C/W when mounted on a 0.5 in<sup>2</sup> pad of 2 oz copper



b) 125°C/W when mounted on a .02 in<sup>2</sup> pad of 2 oz copper



c) 135°C/W when mounted on a minimum pad.

Scale 1:1 on letter size paper

2. Pulse Test: Pulse Width <  $300\mu s$ , Duty Cycle < 2.0%

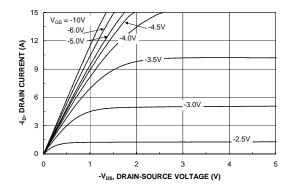


Figure 1. On-Region Characteristics.

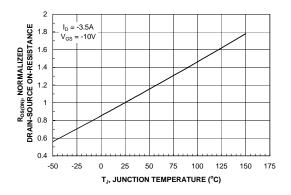


Figure 3. On-Resistance Variation with Temperature.

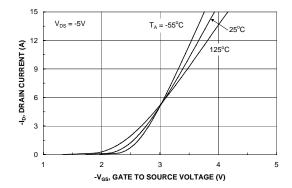


Figure 5. Transfer Characteristics.

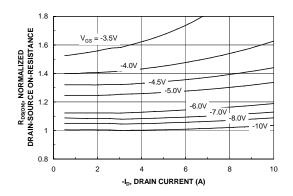


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

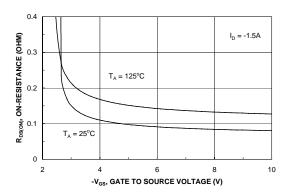


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

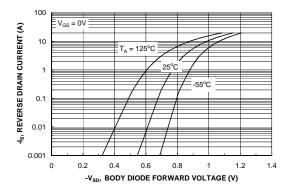


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

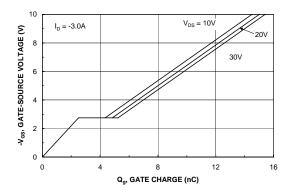


Figure 7. Gate Charge Characteristics.

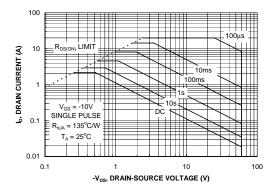


Figure 9. Maximum Safe Operating Area.

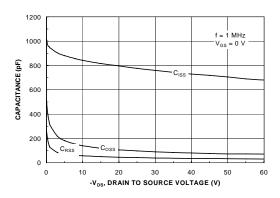


Figure 8. Capacitance Characteristics.

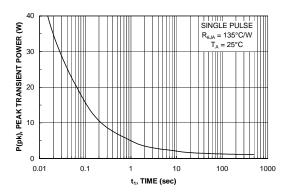


Figure 10. Single Pulse Maximum Power Dissipation.

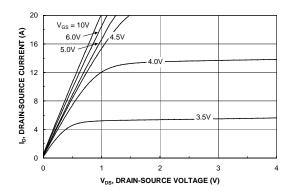


Figure 11. On-Region Characteristics.

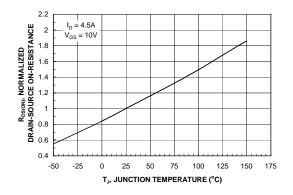


Figure 13. On-Resistance Variation with Temperature.

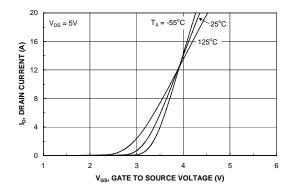


Figure 15. Transfer Characteristics.

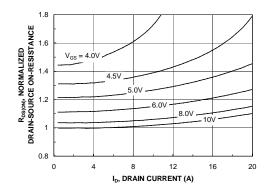


Figure 12. On-Resistance Variation with Drain Current and Gate Voltage.

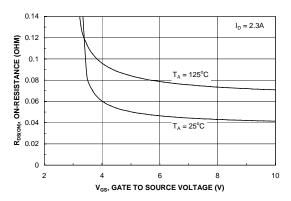


Figure 14. On-Resistance Variation with Gate-to-Source Voltage.

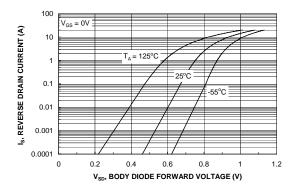
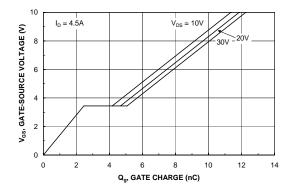


Figure 16. Body Diode Forward Voltage Variation with Source Current and Temperature.



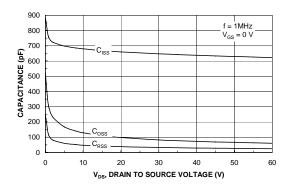
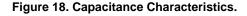
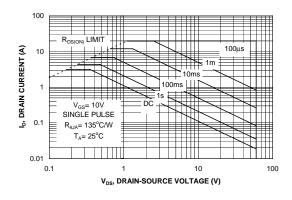


Figure 17. Gate Charge Characteristics.





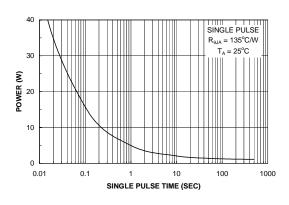


Figure 19. Maximum Safe Operating Area.

Figure 20. Single Pulse Maximum Power Dissipation.

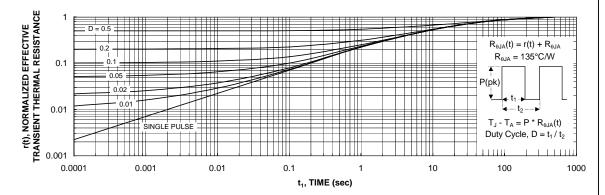


Figure 21. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1c. Transient thermal response will change depending on the circuit board design.





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Definition of Terms						
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Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.				
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