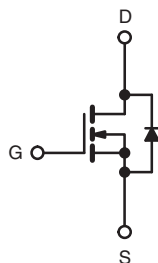
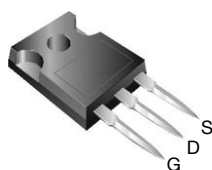


Power MOSFET

PRODUCT SUMMARY

V_{DS} (V)	500	
$R_{DS(on)}$ (Ω)	$V_{GS} = 10\text{ V}$	0.190
Q_g (Max.) (nC)	150	
Q_{gs} (nC)	44	
Q_{gd} (nC)	72	
Configuration	Single	

TO-247AC



N-Channel MOSFET

FEATURES

- Superfast Body Diode Eliminates the Need for External Diodes in ZVS Applications
- Lower Gate Charge Results in Simpler Drive Requirements
- Enhanced dV/dt Capabilities Offer Improved Ruggedness
- Higher Gate Voltage Threshold Offers Improved Noise Immunity
- Compliant to RoHS Directive 2002/95/EC



RoHS*
COMPLIANT

APPLICATIONS

- Zero Voltage Switching SMPS
- Telecom and Server Power Supplies
- Uninterruptible Power Supplies
- Motor Control Applications

ORDERING INFORMATION

Package	TO-247AC
Lead (Pb)-free	IRFP23N50LPbF
	SiHFP23N50L-E3
SnPb	IRFP23N50L
	SiHFP23N50L

ABSOLUTE MAXIMUM RATINGS ($T_C = 25\text{ }^\circ\text{C}$, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V_{DS}	500	V
Gate-Source Voltage	V_{GS}	± 30	
Continuous Drain Current	I_D	$T_C = 25\text{ }^\circ\text{C}$	A
		$T_C = 100\text{ }^\circ\text{C}$	
Pulsed Drain Current ^a	I_{DM}	92	
Linear Derating Factor		2.9	W/ $^\circ\text{C}$
Single Pulse Avalanche Energy ^b	E_{AS}	410	mJ
Repetitive Avalanche Current ^a	I_{AR}	23	A
Repetitive Avalanche Energy ^a	E_{AR}	37	mJ
Maximum Power Dissipation	P_D	370	W
Peak Diode Recovery dV/dt ^c	dV/dt	21	V/ns
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to + 150	$^\circ\text{C}$
Soldering Recommendations (Peak Temperature)	for 10 s	300 ^d	
Mounting Torque	6-32 or M3 screw	10	
		1.1	N · m

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- Starting $T_J = 25\text{ }^\circ\text{C}$, $L = 1.5\text{ mH}$, $R_g = 25\text{ }\Omega$, $I_{AS} = 23\text{ A}$ (see fig. 12).
- $I_{SD} \leq 23\text{ A}$, $dI/dt \leq 650\text{ A}/\mu\text{s}$, $V_{DD} \leq V_{DS}$, $T_J \leq 150\text{ }^\circ\text{C}$.
- 1.6 mm from case.

* Pb containing terminations are not RoHS compliant, exemptions may apply

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	40	°C/W
Case-to-Sink, Flat, Greased Surface	R_{thCS}	0.24	-	
Maximum Junction-to-Case (Drain)	R_{thJC}	-	0.34	

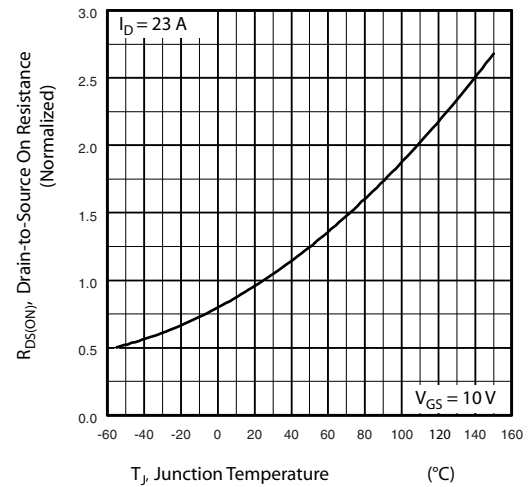
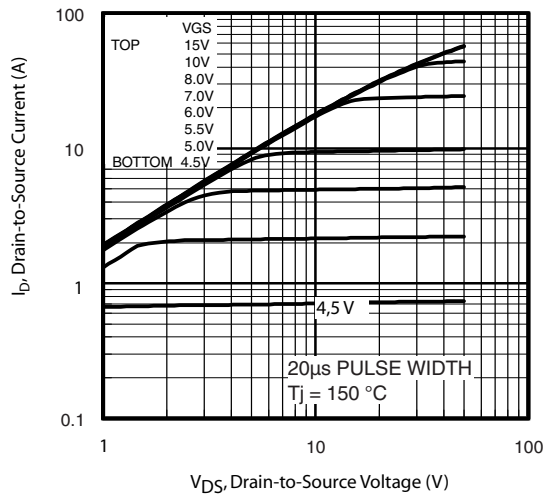
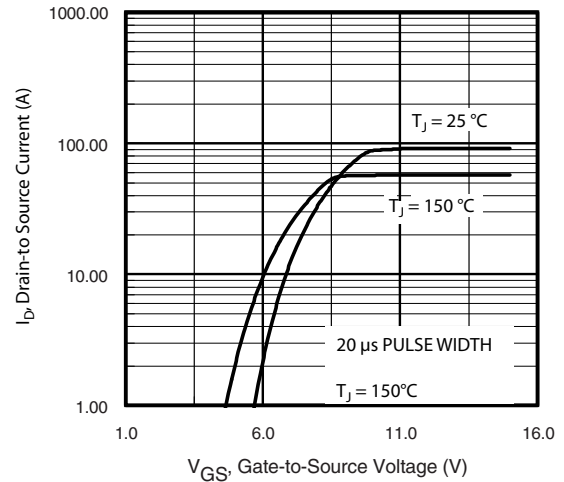
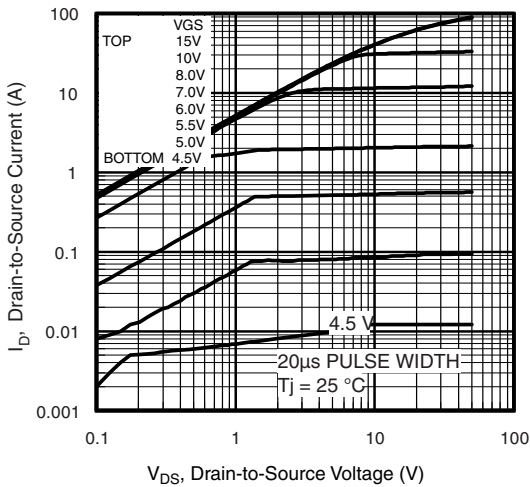
SPECIFICATIONS ($T_J = 25\text{ °C}$, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA		500	-	-	V
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	Reference to 25 °C, I _D = 1 mA ^d		-	0.27	-	V/°C
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA		3.0	-	5.0	V
Gate-Source Leakage	I _{GSS}	V _{GS} = ± 30 V		-	-	± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 500 V, V _{GS} = 0 V		-	-	50	μA
		V _{DS} = 400 V, V _{GS} = 0 V, T _J = 125 °C		-	-	2.0	mA
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} = 10 V	I _D = 14 A ^b	-	0.190	0.235	Ω
Forward Transconductance	g _{fs}	V _{DS} = 50 V, I _D = 14 A ^b		12	-	-	S
Dynamic							
Input Capacitance	C _{iss}	V _{GS} = 0 V, V _{DS} = 25 V, f = 1.0 MHz, see fig. 5		-	3600	-	pF
Output Capacitance	C _{oss}			-	380	-	
Reverse Transfer Capacitance	C _{rss}			-	37	-	
Output Capacitance	C _{oss}	V _{GS} = 0 V	V _{DS} = 1.0 V , f = 1.0 MHz	-	4800	-	
Effective Output Capacitance	C _{oss} eff.		V _{DS} = 400 V , f = 1.0 MHz	-	100	-	
Effective Output Capacitance (Energy Related)	C _{oss} eff. (ER)		V _{DS} = 0 V to 400 V ^c	-	220	-	
		V _{DS} = 0 V to 400 V ^d		-	160	-	
Internal Gate Resistance	R _G	f = 1 MHz, open drain		-	1.2	-	Ω
Total Gate Charge	Q _g	V _{GS} = 10 V	I _D = 23 A, V _{DS} = 400 V see fig. 6 and 13 ^b	-	-	150	nC
Gate-Source Charge	Q _{gs}			-	-	44	
Gate-Drain Charge	Q _{gd}			-	-	72	
Turn-On Delay Time	t _{d(on)}	V _{DD} = 250 V, I _D = 23 A R _g = 6.0, V _{GS} = 10 V see fig. 10 ^b		-	26	-	ns
Rise Time	t _r			-	94	-	
Turn-Off Delay Time	t _{d(off)}			-	53	-	
Fall Time	t _f			-	45	-	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I _S	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	23	A
Pulsed Diode Forward Current ^a	I _{SM}			-	-	92	
Body Diode Voltage	V _{SD}	T _J = 25 °C, I _S = 14 A, V _{GS} = 0 V ^b		-	-	1.5	V
Body Diode Reverse Recovery Time	t _{rr}	T _J = 25 °C	I _F = 23 A, dI/dt = 100 A/μs ^b	-	170	250	ns
		T _J = 125 °C		-	220	330	
Body Diode Reverse Recovery Charge	Q _{rr}	T _J = 25 °C		-	560	840	μC
		T _J = 125 °C		-	980	1500	
Reverse Recovery Current	I _{RRM}	T _J = 25 °C		-	7.6	11	A
Forward Turn-On Time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L _S and L _D)					

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
b. Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$.
c. $C_{oss\text{ eff.}}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DS} .
d. $C_{oss\text{ eff. (ER)}}$ is a fixed capacitance that stores the same energy time as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DS} .

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



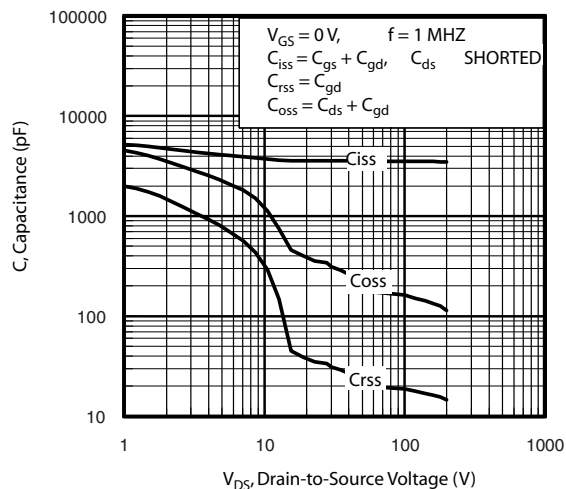


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

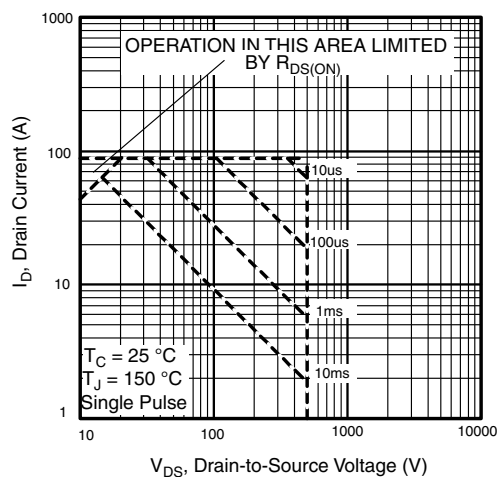


Fig. 7 - Maximum Safe Operating Area

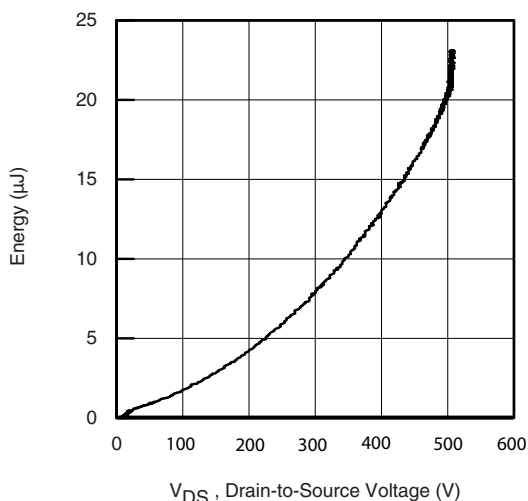


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

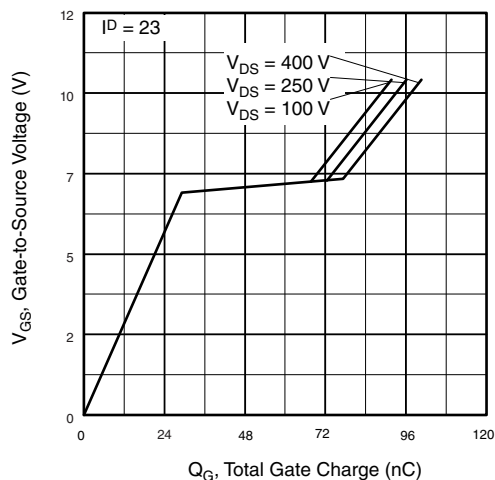


Fig. 8 - Typical Gate Charge vs. Gate-to-Source Voltage

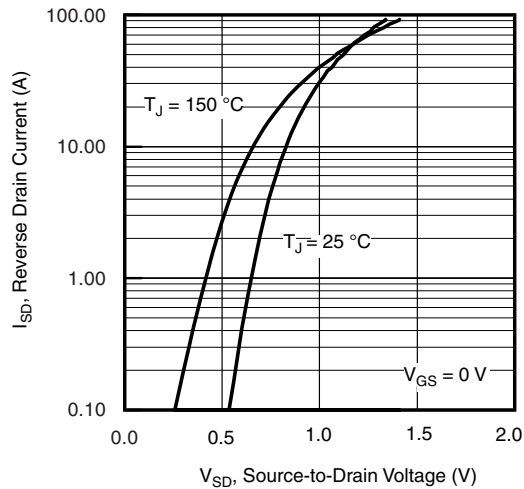


Fig. 9 - Typical Source-Drain Diode Forward Voltage

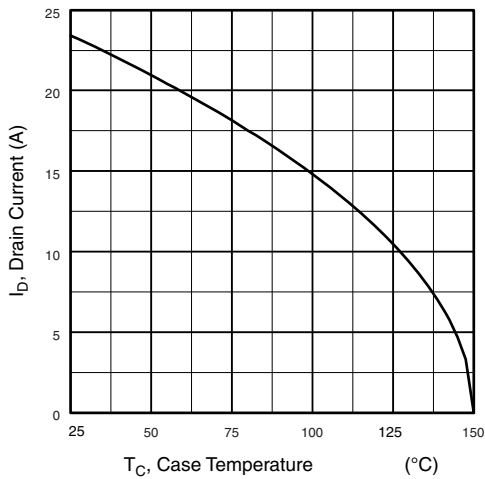


Fig. 10 - Maximum Drain Current vs. Case Temperature

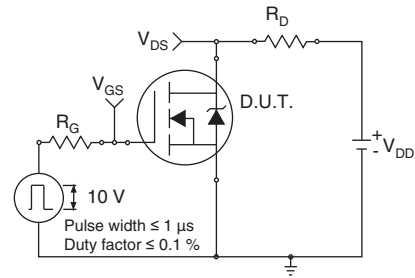


Fig. 11a - Switching Time Test Circuit

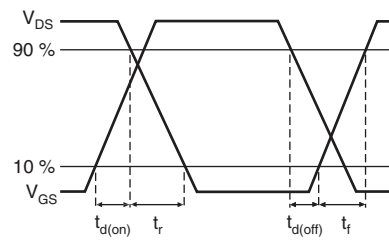


Fig. 11b - Switching Time Waveforms

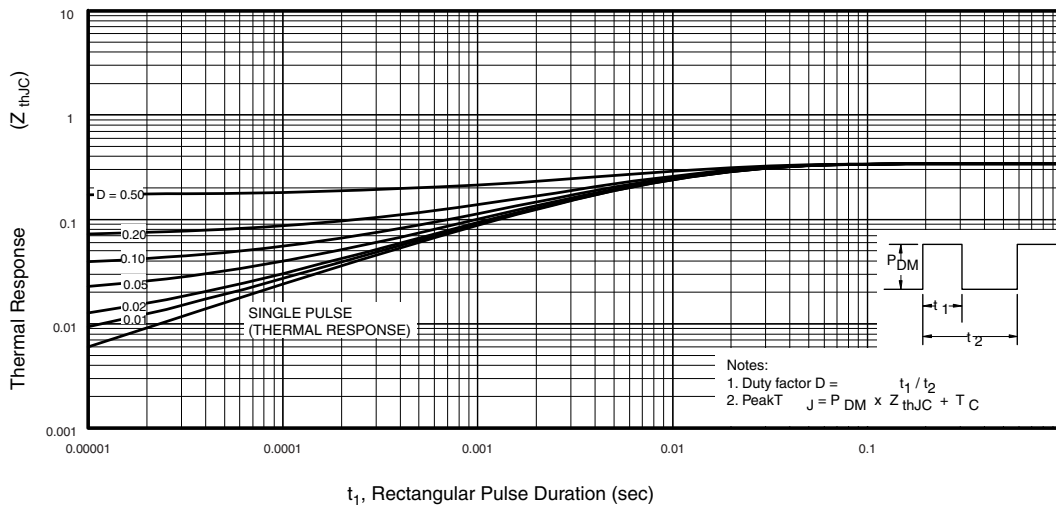


Fig. 12 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

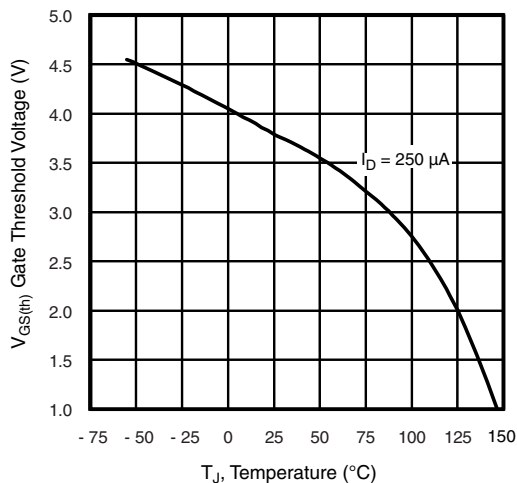


Fig. 13 - Threshold Voltage vs. Temperature

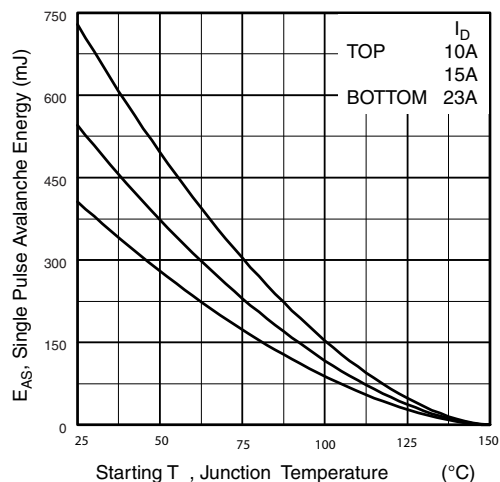


Fig. 14 - Maximum Avalanche Energy s. Drain Current

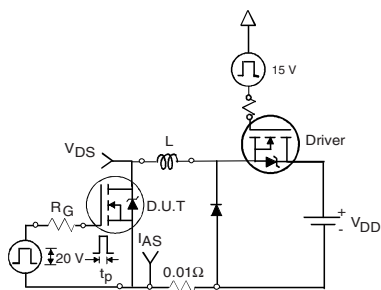


Fig. 15a - Unclamped Inductive Test Circuit

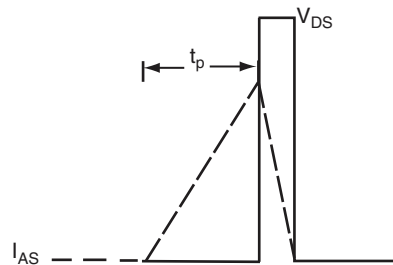


Fig. 15b - Unclamped Inductive Waveforms

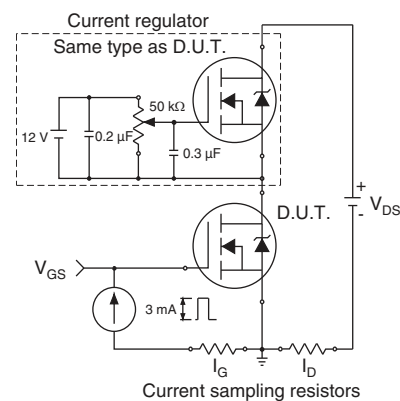


Fig. 16a - Gate Charge Test Circuit

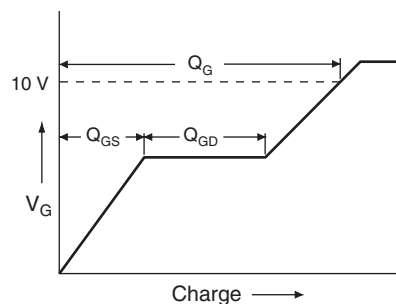


Fig. 16b - Basic Gate Charge Waveform



Note

a. $V_{GS} = 5 V$ for logic level devices

Fig. 17 - For N-Channel

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TO-247AC (High Voltage)



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.58	5.31	0.180	0.209
A1	2.21	2.59	0.087	0.102
A2	1.17	2.49	0.046	0.098
b	0.99	1.40	0.039	0.055
b1	0.99	1.35	0.039	0.053
b2	1.53	2.39	0.060	0.094
b3	1.65	2.37	0.065	0.093
b4	2.42	3.43	0.095	0.135
b5	2.59	3.38	0.102	0.133
c	0.38	0.86	0.015	0.034
c1	0.38	0.76	0.015	0.030
D	19.71	20.82	0.776	0.820
D1	13.08	-	0.515	-

ECN: X13-0103-Rev. D, 01-Jul-13
DWG: 5971

DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
D2	0.51	1.30	0.020	0.051
E	15.29	15.87	0.602	0.625
E1	13.72	-	0.540	-
e	5.46 BSC		0.215 BSC	
Ø k	0.254		0.010	
L	14.20	16.25	0.559	0.640
L1	3.71	4.29	0.146	0.169
N	7.62 BSC		0.300 BSC	
Ø P	3.51	3.66	0.138	0.144
Ø P1	-	7.39	-	0.291
Q	5.31	5.69	0.209	0.224
R	4.52	5.49	0.178	0.216
S	5.51 BSC		0.217 BSC	

Notes

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Contour of slot optional.
3. Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outermost extremes of the plastic body.
4. Thermal pad contour optional with dimensions D1 and E1.
5. Lead finish uncontrolled in L1.
6. Ø P to have a maximum draft angle of 1.5 to the top of the part with a maximum hole diameter of 3.91 mm (0.154").
7. Outline conforms to JEDEC outline TO-247 with exception of dimension c.
8. Xian and Mingxin actually photo.





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