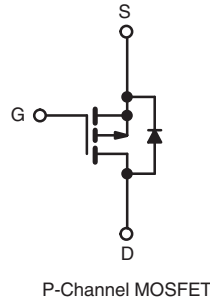


Power MOSFET

PRODUCT SUMMARY

V_{DS} (V)	- 200	
$R_{DS(on)}$ (Ω)	$V_{GS} = -10$ V	1.5
Q_g (Max.) (nC)	15	
Q_{gs} (nC)	3.2	
Q_{gd} (nC)	8.4	
Configuration	Single	

TO-220 FULLPAK


FEATURES

- Isolated Package
- High Voltage Isolation = 2.5 kV_{RMS} (t = 60 s; f = 60 Hz)
- Sink to Lead Creepage Dist. = 4.8 mm
- P-Channel
- Dynamic dV/dt
- Low Thermal Resistance
- Lead (Pb)-free Available


RoHS*
COMPLIANT

DESCRIPTION

Third generation Power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-220 FULLPAK eliminates the need for additional insulating hardware in commercial-industrial applications. The molding compound used provides a high isolation capability and a low thermal resistance between the tab and external heatsink. This isolation is equivalent to using a 100 micron mica barrier with standard TO-220 product. The FULLPAK is mounted to a heatsink using a single clip or by a single screw fixing.

ORDERING INFORMATION

Package	TO-220 FULLPAK
Lead (Pb)-free	IRFI9620GPbF SiHFI9620G-E3
SnPb	IRFI9620G SiHFI9620G

ABSOLUTE MAXIMUM RATINGS $T_C = 25^\circ\text{C}$, unless otherwise noted

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V_{DS}	- 200	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current	V_{GS} at - 10 V	$T_C = 25^\circ\text{C}$	A
		$T_C = 100^\circ\text{C}$	
Pulsed Drain Current ^a	I_{DM}	- 12	
Linear Derating Factor		0.24	W/ $^\circ\text{C}$
Single Pulse Avalanche Energy ^b	E_{AS}	80	mJ
Repetitive Avalanche Current ^a	I_{AR}	- 3.0	A
Repetitive Avalanche Energy ^a	E_{AR}	3.0	mJ
Maximum Power Dissipation	P_D	30	W
Peak Diode Recovery dV/dt ^c	dV/dt	- 5.0	V/ns
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to + 150	$^\circ\text{C}$
Soldering Recommendations (Peak Temperature)	for 10 s	300 ^d	
Mounting Torque	6-32 or M3 screw	10 1.1	

Notes

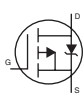
- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- $V_{DD} = -50$ V, starting $T_J = 25^\circ\text{C}$, $L = 13$ mH, $R_G = 25\ \Omega$, $I_{AS} = -3.0$ A (see fig. 12).
- $I_{SD} \leq -3.9$ A, $dI/dt \leq 95$ A/ μs , $V_{DD} \leq V_{DS}$, $T_J \leq 150^\circ\text{C}$.
- 1.6 mm from case.

* Pb containing terminations are not RoHS compliant, exemptions may apply

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	65	°C/W
Maximum Junction-to-Case (Drain)	R_{thJC}	-	4.1	

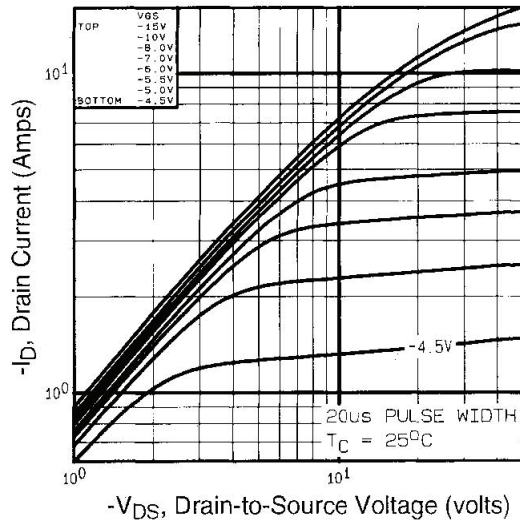
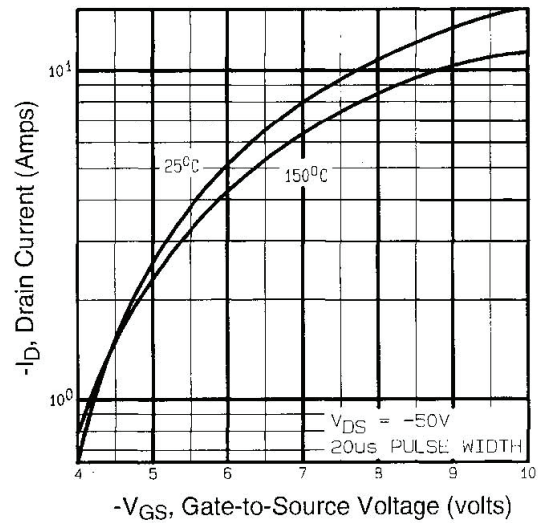
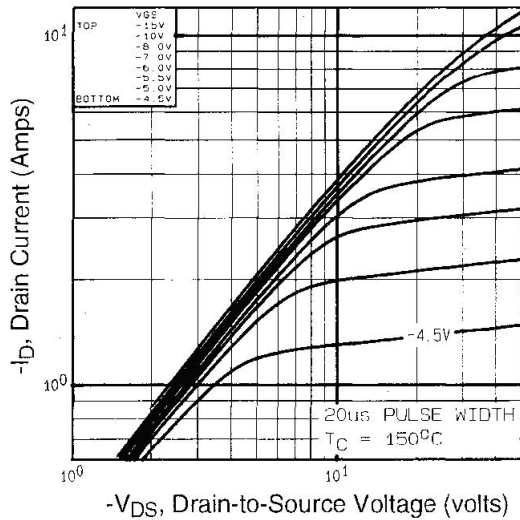
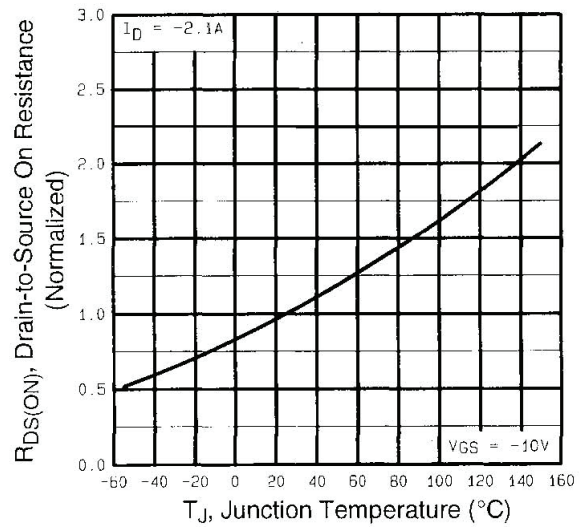
SPECIFICATIONS $T_J = 25\text{ }^{\circ}\text{C}$, unless otherwise noted

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}$, $I_D = -250\text{ }\mu\text{A}$		-200	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^{\circ}\text{C}$, $I_D = -1\text{ mA}$		-	-0.22	-	V/ $^{\circ}\text{C}$
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = -250\text{ }\mu\text{A}$		-2.0	-	-4.0	V
Gate-Source Leakage	I_{GSS}	$V_{GS} = \pm 20\text{ V}$		-	-	± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -200\text{ V}$, $V_{GS} = 0\text{ V}$		-	-	-100	μA
		$V_{DS} = -160\text{ V}$, $V_{GS} = 0\text{ V}$, $T_J = 125\text{ }^{\circ}\text{C}$		-	-	-500	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = -10\text{ V}$	$I_D = -1.8\text{ A}^b$	-	-	1.5	Ω
Forward Transconductance	g_{fs}	$V_{DS} = -50\text{ V}$, $I_D = -1.8\text{ A}^b$		1.3	-	-	S
Dynamic							
Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V}$, $V_{DS} = -15\text{ V}$, $f = 1.0\text{ MHz}$, see fig. 5		-	340	-	pF
Output Capacitance	C_{oss}			-	110	-	
Reverse Transfer Capacitance	C_{rss}			-	33	-	
Drain to Sink Capacitance	C	$f = 1\text{ MHz}$		-	12	-	
Total Gate Charge	Q_g	$V_{GS} = -10\text{ V}$	$I_D = -2.1\text{ A}$, $V_{DS} = -160\text{ V}$, see fig. 6 and 13 ^b	-	-	15	nC
Gate-Source Charge	Q_{gs}			-	-	3.2	
Gate-Drain Charge	Q_{gd}			-	-	8.4	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -100\text{ V}$, $I_D = -3.9\text{ A}$, $R_G = 18\text{ }\Omega$, $R_D = 24\text{ }\Omega$, see fig. 10 ^b		-	8.8	-	ns
Rise Time	t_r			-	27	-	
Turn-Off Delay Time	$t_{d(off)}$			-	7.3	-	
Fall Time	t_f			-	19	-	
Internal Drain Inductance	L_D	Between lead, 6 mm (0.25") from package and center of die contact 		-	4.5	-	nH
Internal Source Inductance	L_S			-	7.5	-	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	-3.0	A
Pulsed Diode Forward Current ^a	I_{SM}			-	-	-12	
Body Diode Voltage	V_{SD}	$T_J = 25\text{ }^{\circ}\text{C}$, $I_S = -3.0\text{ A}$, $V_{GS} = 0\text{ V}^b$		-	-	-6.3	V
Body Diode Reverse Recovery Time	t_{rr}	$T_J = 25\text{ }^{\circ}\text{C}$, $I_F = -3.9\text{ A}$, $dI/dt = 100\text{ A}/\mu\text{s}^b$		-	150	300	ns
Body Diode Reverse Recovery Charge	Q_{rr}			-	0.97	2.0	μC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)					

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).

b. Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

Fig. 1 - Typical Output Characteristics, $T_C = 25^\circ\text{C}$

Fig. 3 - Typical Transfer Characteristics

Fig. 2 - Typical Output Characteristics, $T_C = 150^\circ\text{C}$

Fig. 4 - Normalized On-Resistance vs. Temperature

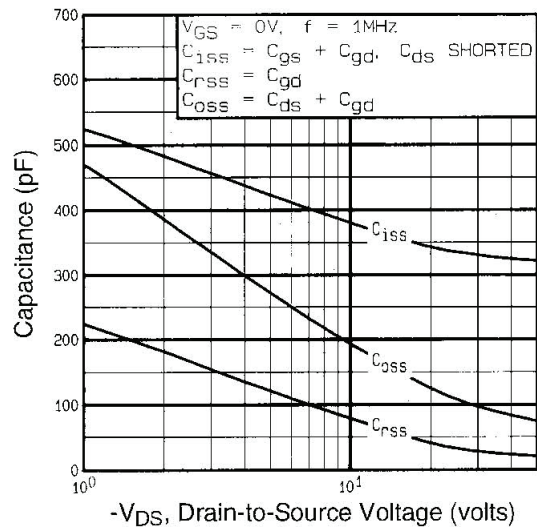


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

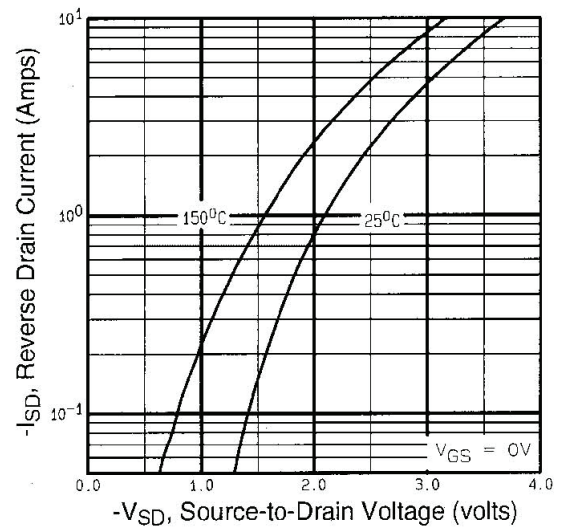


Fig. 7 - Typical Source-Drain Diode Forward Voltage

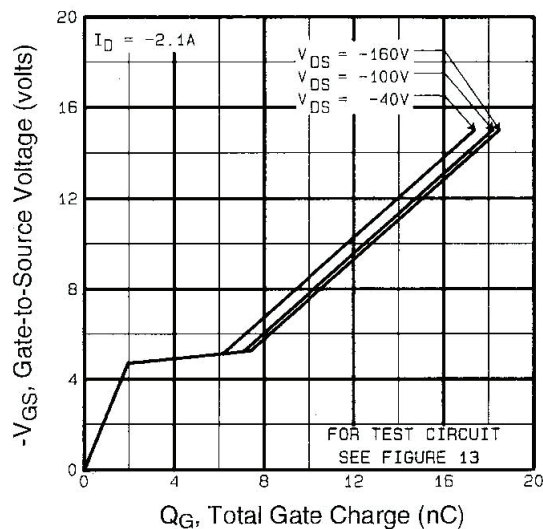


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

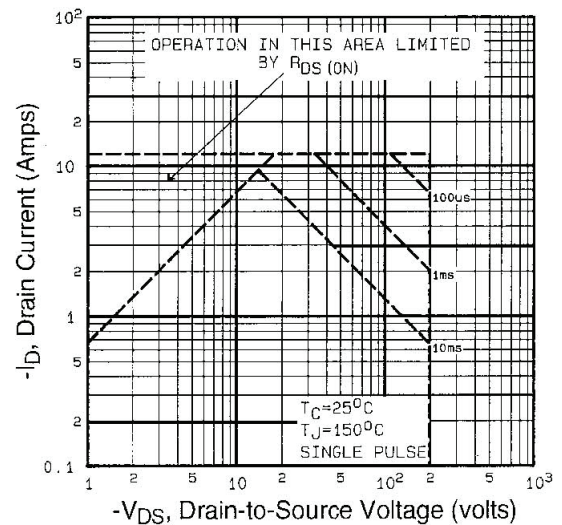


Fig. 8 - Maximum Safe Operating Area

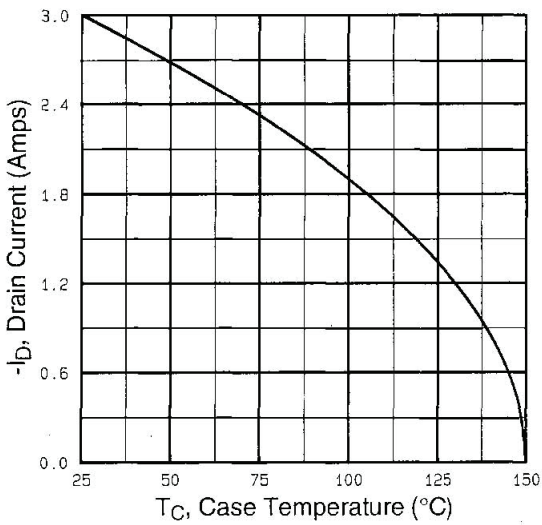


Fig. 9 - Maximum Drain Current vs. Case Temperature

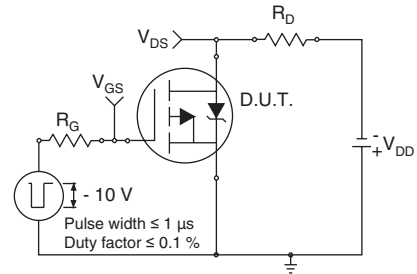


Fig. 10a - Switching Time Test Circuit

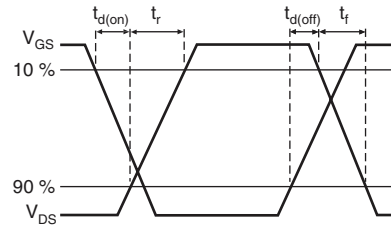


Fig. 10b - Switching Time Waveforms

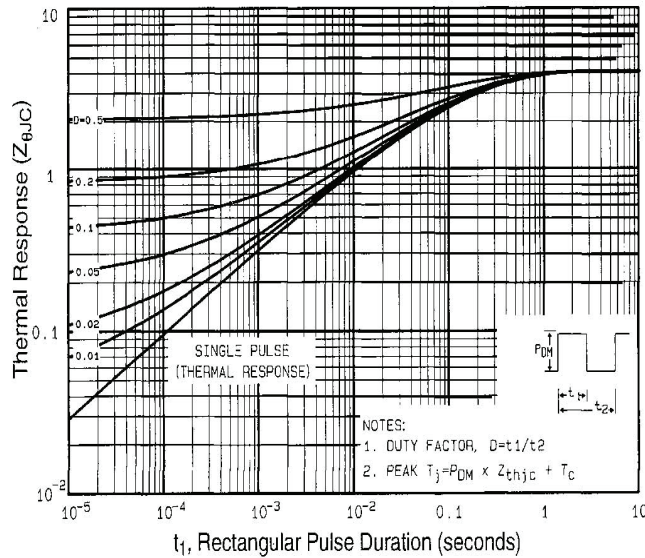


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

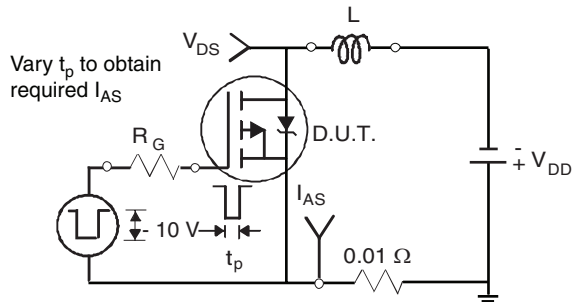


Fig. 12a - Unclamped Inductive Test Circuit

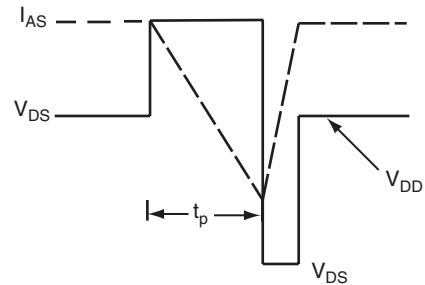


Fig. 12b - Unclamped Inductive Waveforms

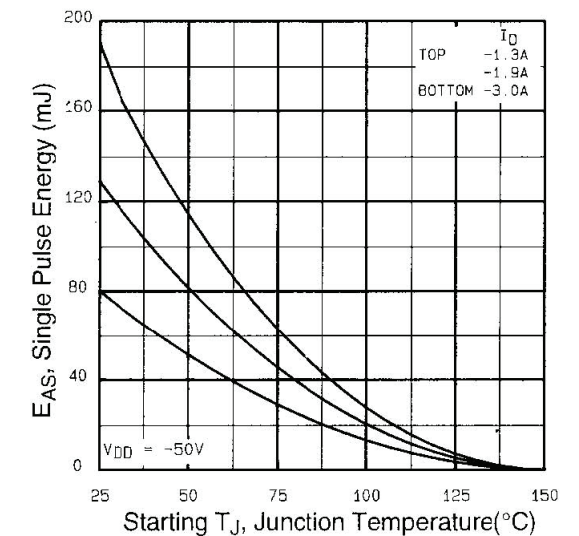


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

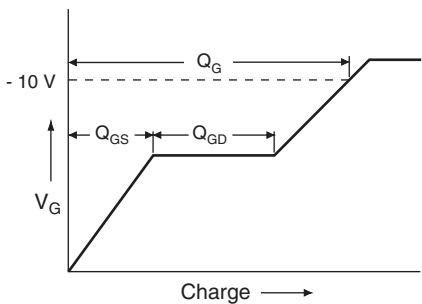


Fig. 13a - Basic Gate Charge Waveform

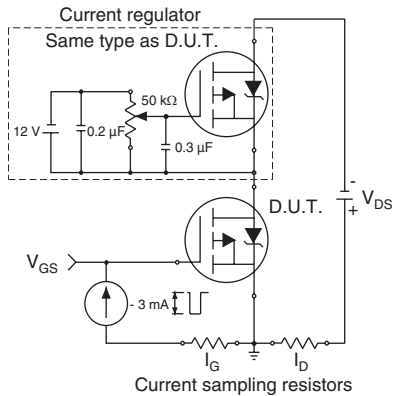
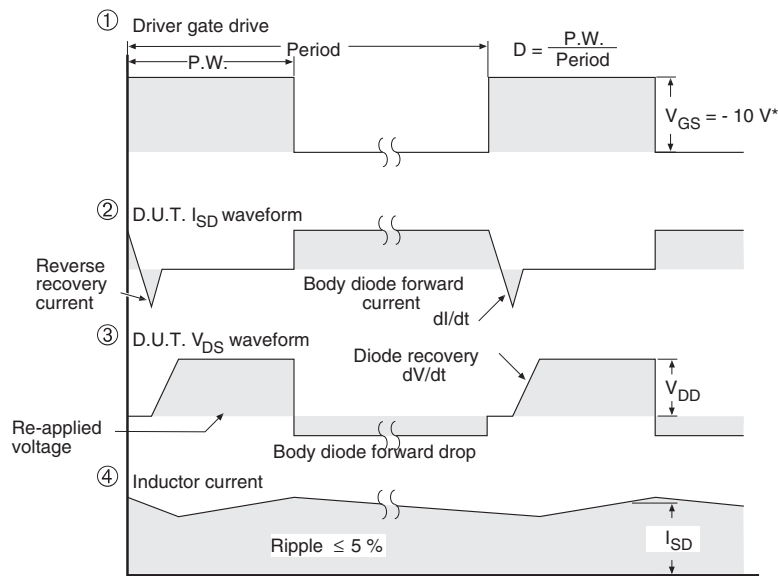
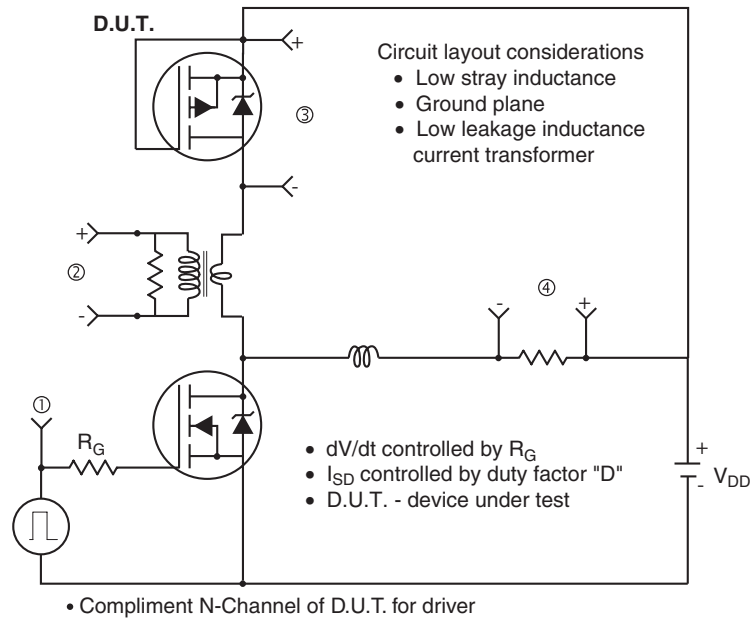


Fig. 13b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit



* $V_{GS} = -5 V$ for logic level and $-3 V$ drive devices

Fig. 14 - For P-Channel

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