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Please note: As part of the Fairchild Semiconductor integration, some of the Fairchild orderable part numbers will need to change in order to meet ON Semiconductor's system requirements. Since the ON Semiconductor product management systems do not have the ability to manage part nomenclature that utilizes an underscore (_), the underscore (_) in the Fairchild part numbers will be changed to a dash (-). This document may contain device numbers with an underscore (_). Please check the ON Semiconductor website to verify the updated device numbers. The most current and up-to-date ordering information can be found at www.onsemi.com. Please email any questions regarding the system integration to Fairchild_questions@onsemi.com.

April 2016

FDD4685_F085

P-Channel PowerTrench® MOSFET

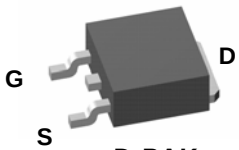
-40 V, -32 A, 35 mΩ

Features

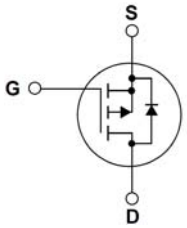
- Typical $R_{DS(on)}$ = 23 mΩ at V_{GS} = -10V, I_D = -8.4 A
- Typical $R_{DS(on)}$ = 30 mΩ at V_{GS} = -4.5V, I_D = -7 A
- Typical $Q_{g(tot)}$ = 19 nC at V_{GS} = -5V, I_D = -8.4 A
- UIS Capability
- RoHS Compliant
- Qualified to AEC Q101

Applications

- Inverter
- Power Supplies



D-PAK
(TO-252)



For current package drawing, please refer to the Fairchild web-site at http://www.fairchildsemi.com/package-drawings/TO/TO252A03.pdf.

MOSFET Maximum Ratings T_J = 25°C unless otherwise noted.

Symbol	Parameter		Ratings	Units
V_{DSS}	Drain-to-Source Voltage		-40	V
V_{GS}	Gate-to-Source Voltage		±20	V
I_D	Drain Current - Continuous (T_C < 90°C, V_{GS}=10)	(Note 1)	-32	A
	Pulsed Drain Current		See Figure 4	
E_{AS}	Single Pulse Avalanche Energy	(Note 2)	121	mJ
P_D	Power Dissipation		83	W
	Derate Above 25°C		0.56	W/°C
T_J, T_{STG}	Operating and Storage Temperature		-55 to + 175	°C
$R_{\theta JC}$	Thermal Resistance, Junction to Case		1.8	°C/W
$R_{\theta JA}$	Maximum Thermal Resistance, Junction to Ambient	(Note 3)	40	°C/W

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDD4685	FDD4685_F085	D-PAK(TO-252)	13”	12mm	2500units

Notes:
1. Current is limited by bondwire configuration.
2. Starting T_J = 25°C, L = 3mH, I_{AS} = 9A, V_{DD} = 40V during inductor charging and V_{DD} = 0V during time in avalanche.
3. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design, while $R_{\theta JA}$ is determined by the board design. The maximum rating presented here is based on mounting on a 1 in^2 pad of 2oz copper.
4. A suffix as “…F085P” has been temporarily introduced in order to manage a double source strategy as Fairchild has officially announced in Aug 2014.

Electrical Characteristics T_J = 25°C unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
Off Characteristics						
B_{VDSS}	Drain-to-Source Breakdown Voltage	I_D = -250μA, V_{GS} = 0V	-40	-	-	V
$\frac{\Delta B_{VDSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	ID = -250μA, referenced to 25°C	-	-33	-	mV/°C
I_{DSS}	Drain-to-Source Leakage Current	V_{DS} = -32V	-	-	-1	μA
I_{GSS}	Gate-to-Source Leakage Current	V_{GS} = ±20V	-	-	±100	nA
On Characteristics						
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = -250μA	-1	-1.6	-3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	ID = –250μA, referenced to 25°C	-	4.9	-	mV/°C
$R_{DS(on)}$	Drain to Source On Resistance	I_D = -8.4A, V_{GS}= -10V	-	23	27	mΩ
		I_D = -7A, V_{GS}= -4.5V	-	30	35	
		I_D = -8.4A, V_{GS}= -10V, T_J = 150°C	-	38	45	
g_{FS}	Forward Transconductance	ID = –8.4A, VDS = –5V	-	23	-	s
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = -20V, V_{GS} = 0V, f = 1MHz	-	1790	2380	pF
C_{oss}	Output Capacitance		-	260	345	pF
C_{rss}	Reverse Transfer Capacitance		-	140	205	pF
R_g	Gate Resistance	f = 1MHz	-	4	-	Ω
$Q_{g(ToT)}$	Total Gate Charge	V_{DD} = -20V, V_{GS} = -5V, I_D = -8.4A	-	19	27	nC
Q_{gs}	Gate-to-Source Gate Charge		-	5.6	-	nC
Q_{gd}	Gate-to-Drain “Miller“ Charge		-	6.1	-	nC
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay	V_{DD} = -20V, I_D = -8.4A, V_{GS} = -10V, R_{GEN} = 6Ω	-	8	16	ns
t_r	Rise Time		-	15	27	ns
$t_{d(off)}$	Turn-Off Delay		-	34	55	ns
t_f	Fall Time		-	14	26	ns
Drain-Source Diode Characteristics						
V_{SD}	Source-to-Drain Diode Voltage	I_{SD} = -8.4A, V_{GS} = 0V	-	-0.85	-1.2	V
t_{rr}	Reverse-Recovery Time	I_{SD} = -8.4A, dI_{SD}/dt = 100A/μs	-	30	45	ns
Q_{rr}	Reverse-Recovery Charge		-	31	47	nC

Typical Characteristics

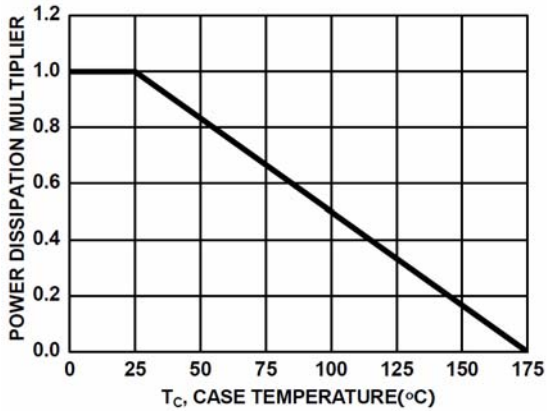


Figure 1. Normalized Power Dissipation vs. Case Temperature

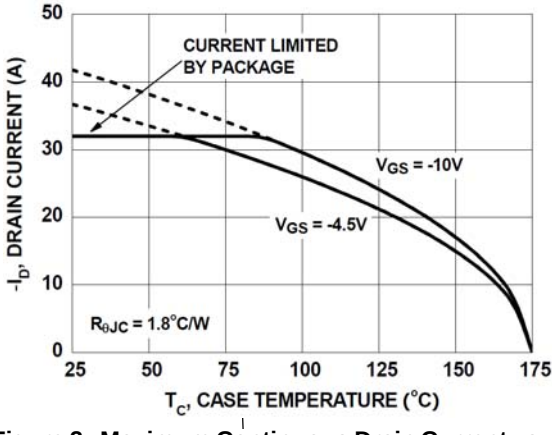


Figure 2. Maximum Continuous Drain Current vs. Case Temperature

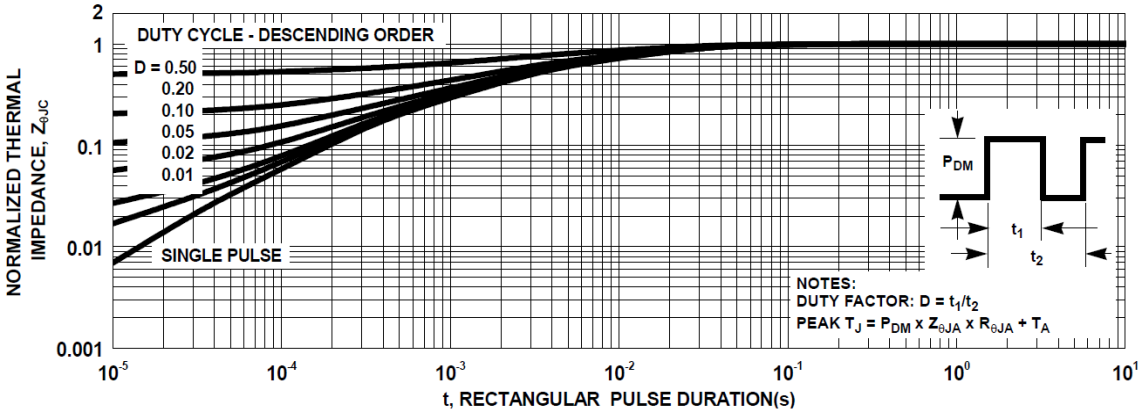


Figure 3. Normalized Maximum Transient Thermal Impedance

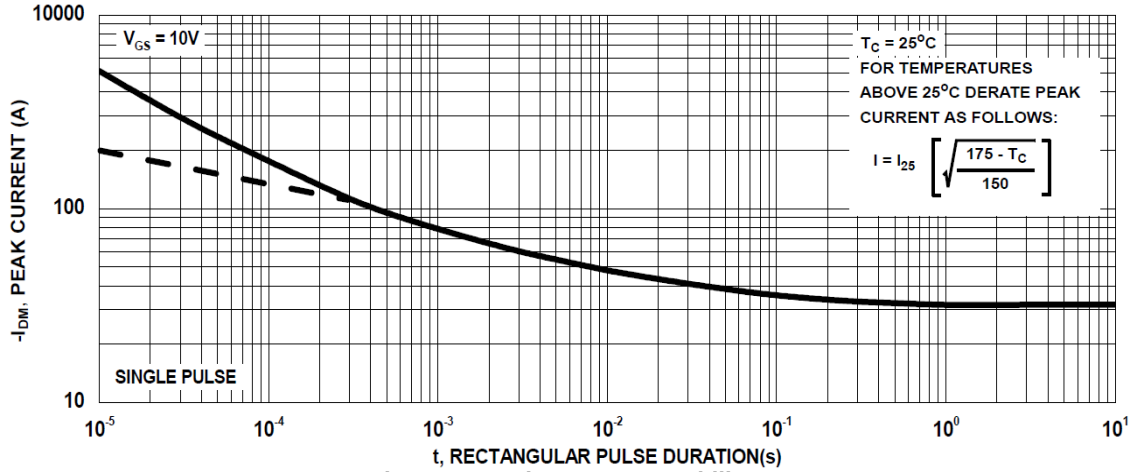


Figure 4. Peak Current Capability

Typical Characteristics

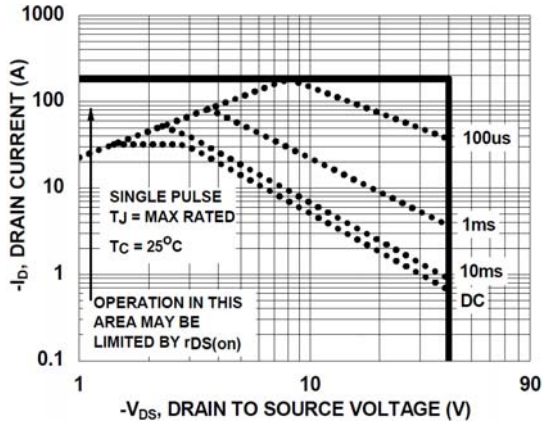
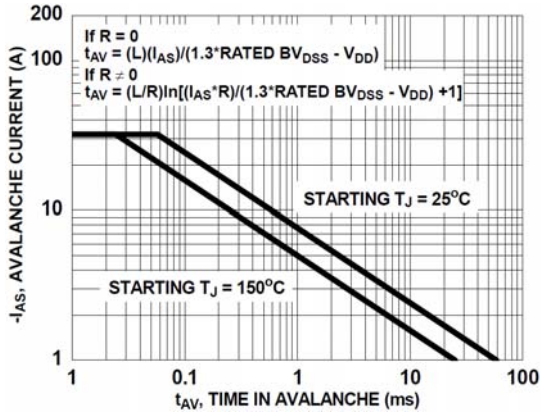


Figure 5. Forward Bias Safe Operating Area



NOTE: Refer to Fairchild Application Notes AN7514 and AN7515

Figure 6. Unclamped Inductive Switching Capability

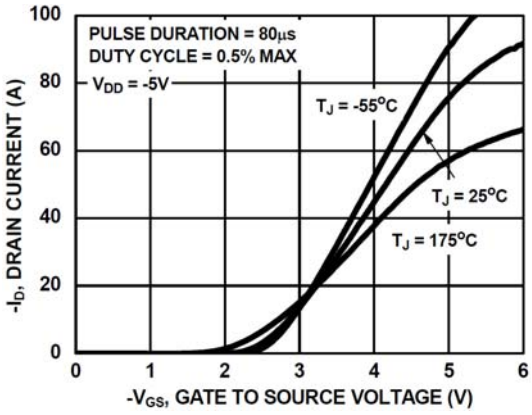


Figure 7. Transfer Characteristics

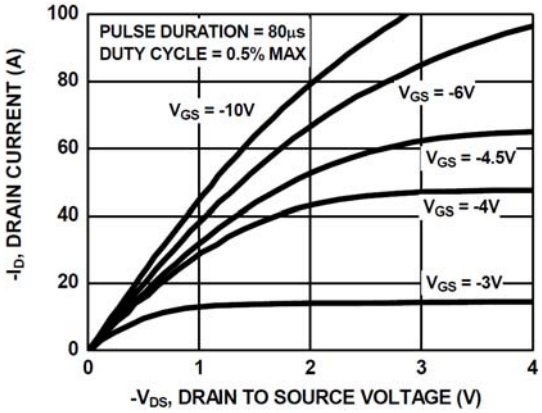


Figure 8. Saturation Characteristics

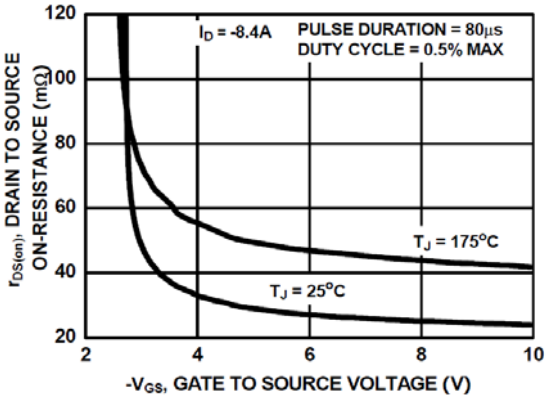


Figure 9. Drain to Source On-Resistance Variation vs. Gate to Source Voltage

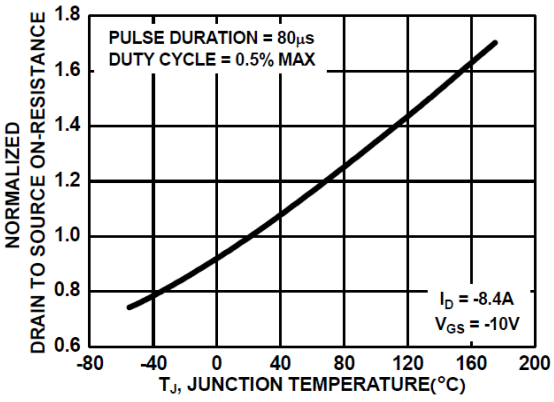


Figure 10. Normalized Drain to Source On Resistance vs. Junction Temperature

Typical Characteristics

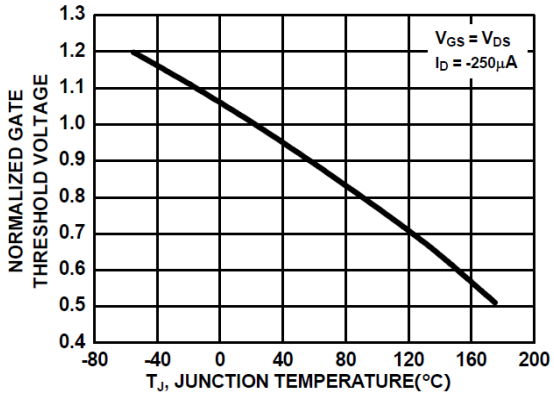


Figure 11. Normalized Gate Threshold Voltage vs. Junction Temperature

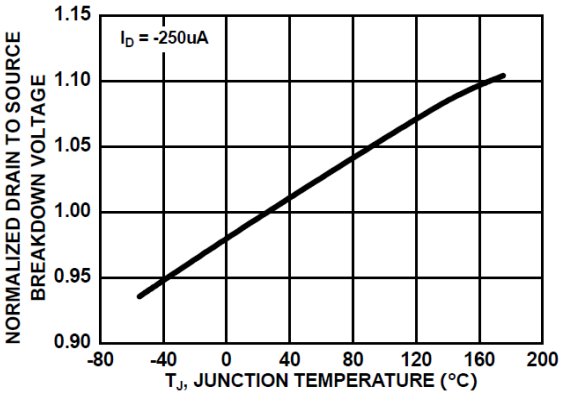


Figure 12. Normalized Drain to Source Breakdown Voltage vs. Junction Temperature

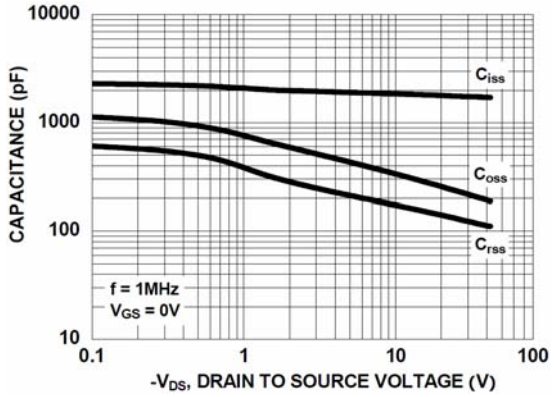


Figure 13. Capacitance vs. Drain to Source Voltage

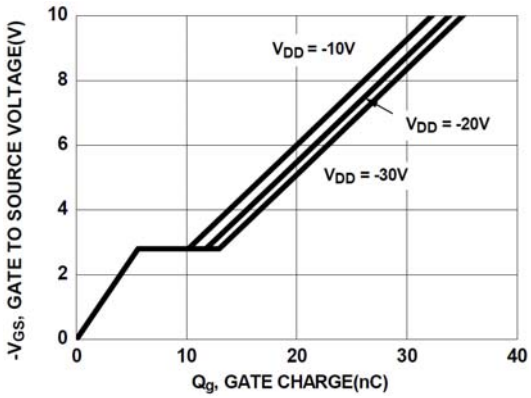
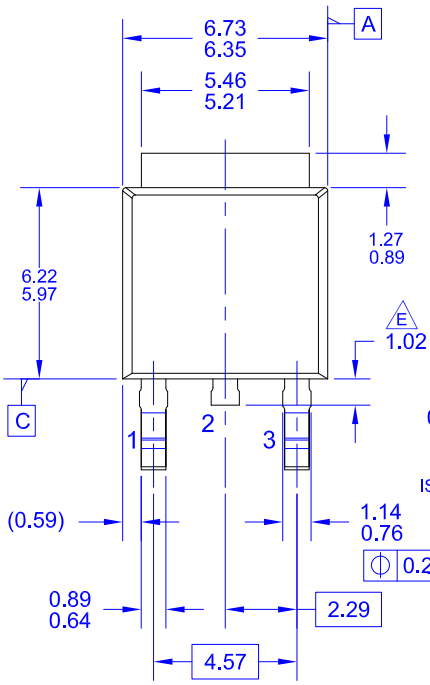
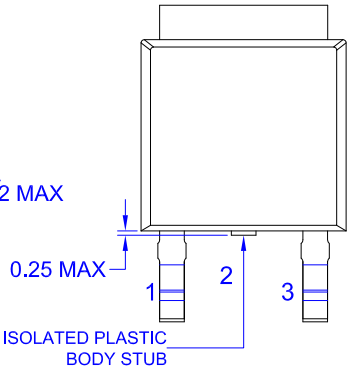


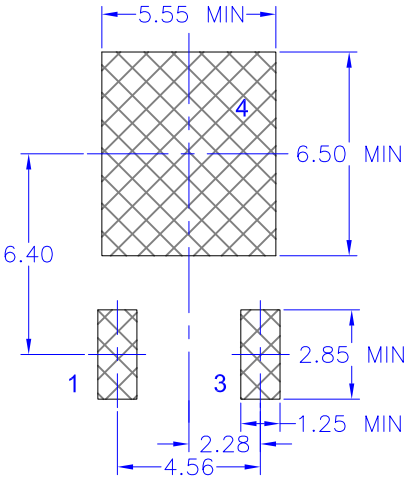
Figure 14. Gate charge vs. Gate to Source Voltage



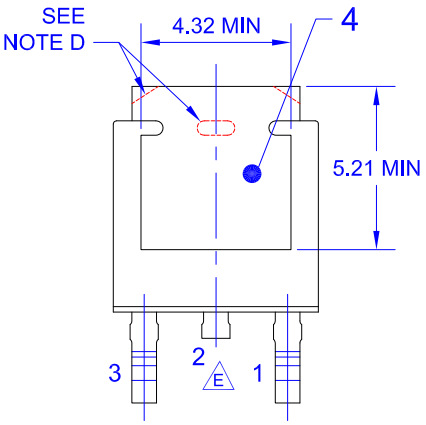
NON-DIODE PRODUCTS VERSION



DIODE PRODUCTS VERSION



LAND PATTERN RECOMMENDATION



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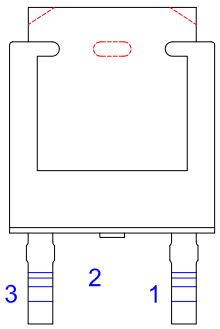

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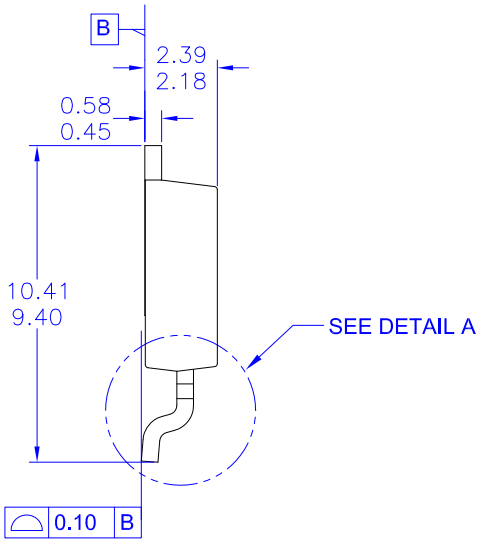
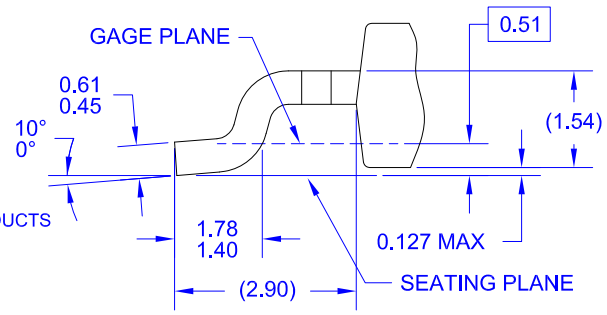


NOTES: UNLESS OTHERWISE SPECIFIED

A) THIS PACKAGE CONFORMS TO JEDEC, TO-252, ISSUE C, VARIATION AA.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
D) SUPPLIER DEPENDENT MOLD LOCKING HOLES OR CHAMFERED CORNERS OR EDGE PROTRUSION.
E) TRIMMED METAL CENTER LEAD IS PRESENT ON FOR NON-DIODE PRODUCTS
F) DIMENSIONS ARE EXCLUSIVE OF BURS, MOLD FLASH AND TIE BAR EXTRUSIONS.
G) LAND PATTERN RECOMMENDATION IS BASED ON IPC7351A STD TO228P991X239-3N.
H) DRAWING NUMBER AND REVISION: MKT-TO252A03REV11



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