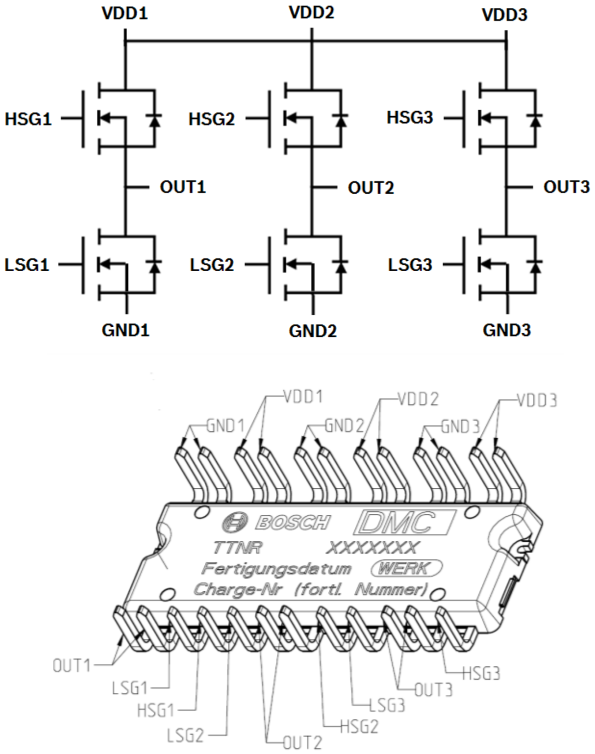
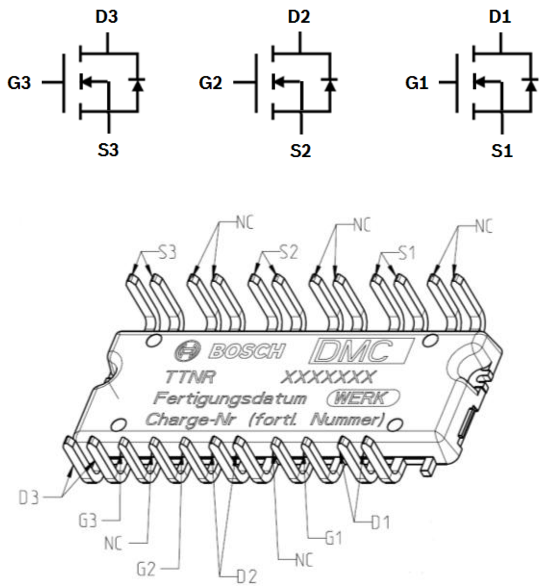
Features:

- 6 MOSFET power module (B6-bridge)
- Optimized R_{th}, Z_{th}
- N-channel
- Normal level
- 100% avalanche tested
- Pb-free plating and soldering
- Halogen-free (IEC61249-2-21)
- AEC-Q101 Stress Test Qualification

Overview		
V_{DS}	40	V
$R_{DS(on),\ max,\ Tj\ =\ 25°C}$	1.98	mΩ

Type:





B6-bridge-module (0 273 105 509)

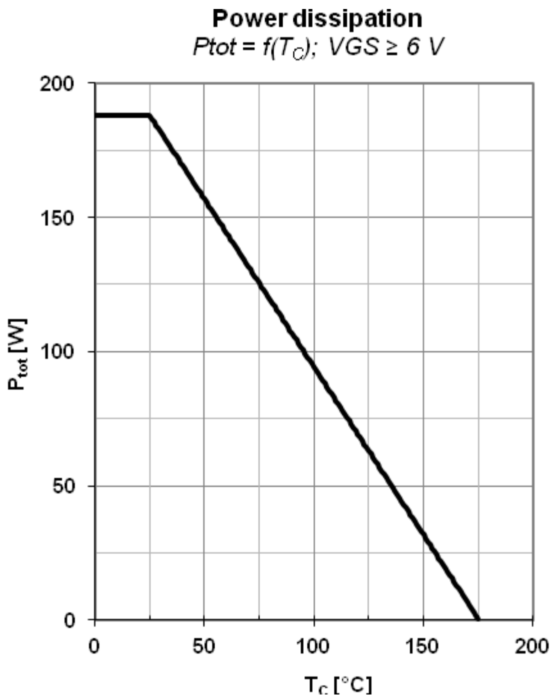
Phase-disconnect-module (0 273 105 510)

Maximum Ratings at T_j = 25 °C for a single MOSFET from pin-pin, unless otherwise specified

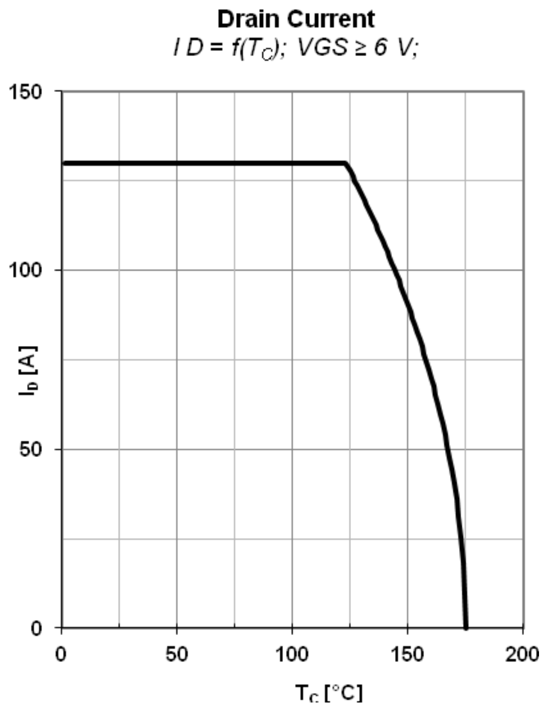
Parameter	Symbol	Conditions	Value	Unit
Continuous drain current [1] (junction-to-case)	$I_{D(J\text{-}C)}$	V_{GS}=10 V, T_C=25 °C	130	A
		V_{GS}=10 V, T_C=100 °C	130	A
Continuous drain current [2)] (junction-to-heat sink, for system design)	$I_{D(J\text{-}HS)}$	V_{GS}=10 V, T_{HS}=25 °C $R_{TH\ (J\text{-}HS)}$ = 3 K/W	100	A
		V_{GS}=10 V, T_{HS}=100 °C $R_{TH\ (J\text{-}HS)}$ = 3 K/W	70	A
Gate source voltage	V_{GS}		±20	V
Power dissipation) [2)] (junction-to-case)	$P_{TOT(J\text{-}C)}$	T_C=25 °C, $T_{J,\ max}$ = 175 °C, $R_{TH\ (J\text{-}C)}$ = 0.8 K/W,	180	W
Power dissipation [3)] (junction-to-heat sink, for system design)	$P_{TOT(J\text{-}HS)}$	T_C=25 °C, $T_{J,\ max}$ = 175 °C, $R_{TH\ (J\text{-}HS)}$ = 3 K/W	50	W
Avalanche energy single pulse	E_{AS}	I_D=52.6 A T_j = 150°C	276	mJ

Thermal Characteristics for a single MOSFET from pin-pin						
Parameter	**Symbol**	**Conditions**	**Value**			**Unit**
			Min	**Typ**	**Max**	
Thermal resistance, Junction-to-case [2]	$R_{TH\ (J\text{-}C)}$		-	0.65	0.8	K/W
Thermal resistance, Junction-to-heat sink[3]	$R_{TH\ (J\text{-}HS)}$		-	3	-	K/W
Junction temperature	T_j				175	°C

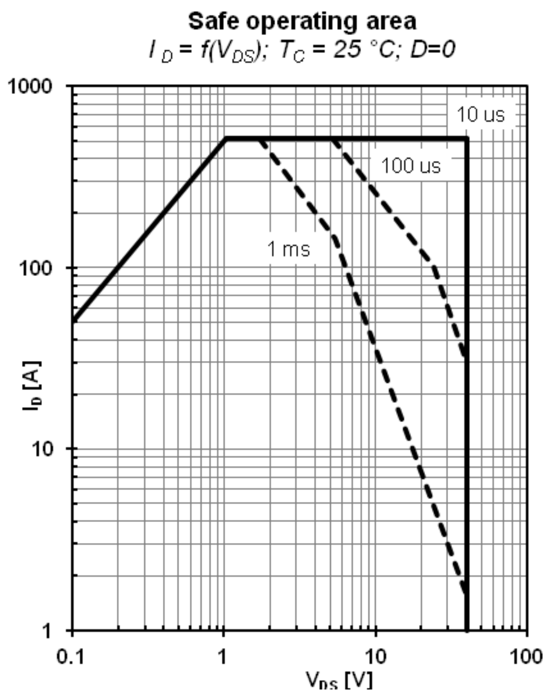
Electrical characteristics, at T_J = 25°C, for a single MOSFET from pin-pin, unless otherwise specified						
Parameter	**Symbol**	**Conditions**	**Value**			**Unit**
			Min	**Typ**	**Max**	
Static characteristics						
Drain-source breakdown voltage	$V_{(BR)DSS}$	V_{GS}=0 V, I_D=250 µA	40			V
Gate threshold voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=140 µA	2.00	3.00	4.00	V
Drain-source on-state resistance	$R_{DS(on)}$	V_{GS}=10 V, I_D=130 A	-	1.65	1.98	mΩ
Zero gate voltage drain current	I_{DSS}	V_{DS}=40V, V_{GS}=0V	-	0.03	1.00	µA
Gate-source leakage current	I_{GSS}	V_{GS}=20V, V_{DS}=0V	-	-	100	nA
Dynamic characteristics						
Input capacitance	C_{ISS}	V_{GS}=0 V, V_{DS}=25 V, f =1 MHz	-	6300	9500	pF
Output capacitance	C_{OSS}		-	870	1300	
Reverse transfer capacitance	C_{RSS}		-	350	630	
Gate charge characteristics						
Gate to source charge	Q_{GS}	V_{DS}=32 V, I_D=130 A, V_{GS}= 10 V	-	32	48	nC
Gate to drain charge	Q_{GD}		-	29	53	
Gate charge total	Q_G		-	110	165	
Gate plateau voltage	$V_{plateau}$		-	5.0	-	V
Reverse Diode						
Diode continuous forward current [1] (junction-to-case)	I_S	T_C = 25 °C			130	A
Diode forward voltage	V_{SD}	V_{GS}=0V, I_D=130A, T_J=25°C		0.9	1.5	V
ESD protection						
HBM: +/- 2kV; CDM: +- 500V						



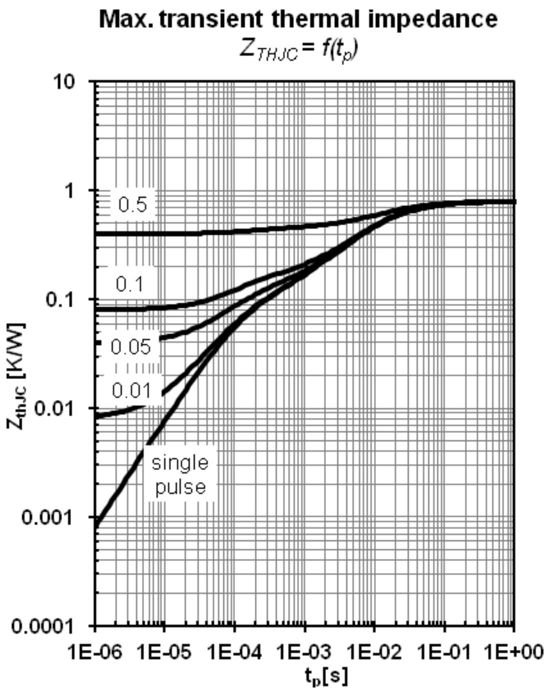
Power dissipation
Ptot = f(T_C); VGS ≥ 6 V
P_tot [W]
T_C [°C]
0
50
100
150
200



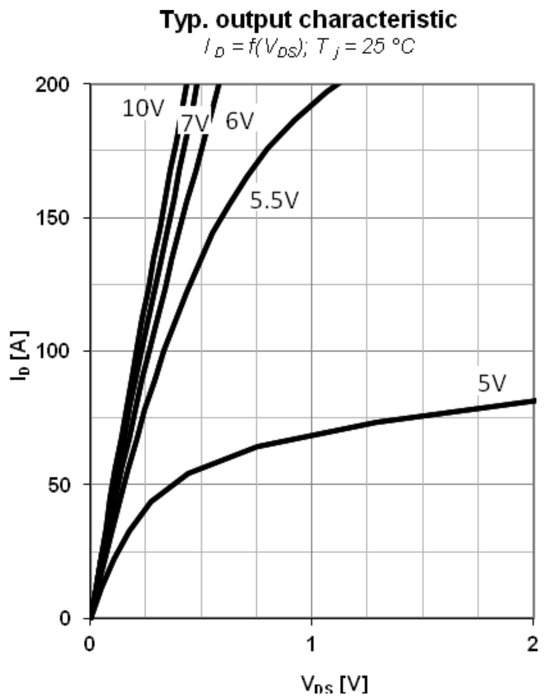
Drain Current
I D = f(T_C); VGS ≥ 6 V;
I_D [A]
T_C [°C]
0
50
100
150
200

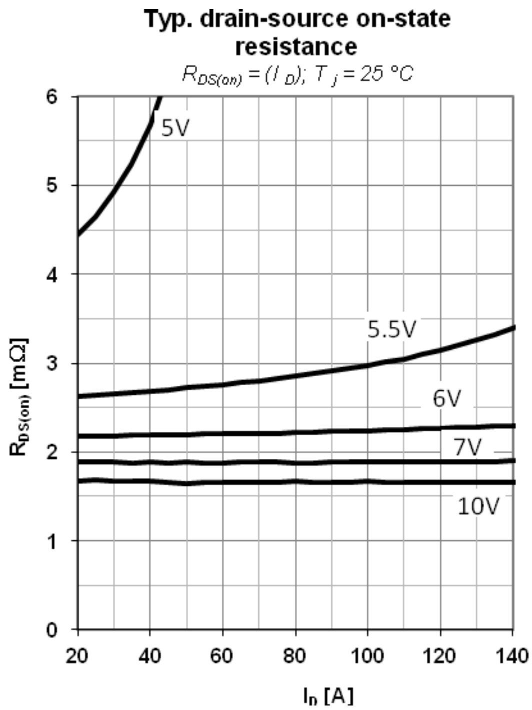


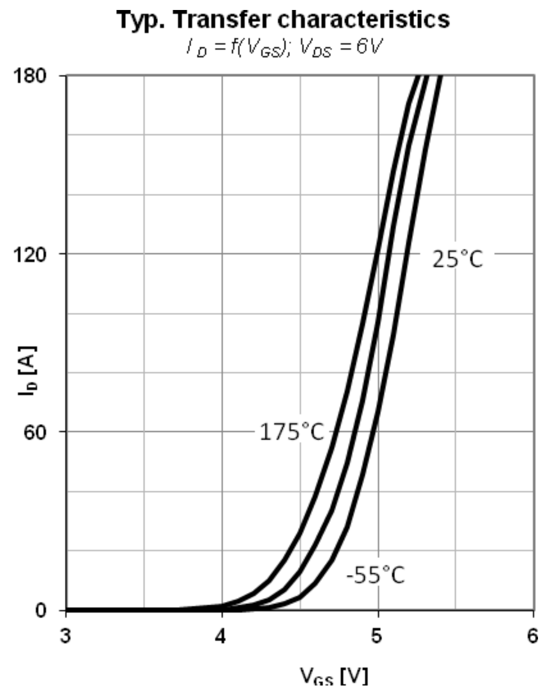
Safe operating area
I D = f(V_DS); T_C = 25 °C; D=0
10 us
100 us
1 ms
I_D [A]
V_DS [V]
1000
100
10
1
0.1

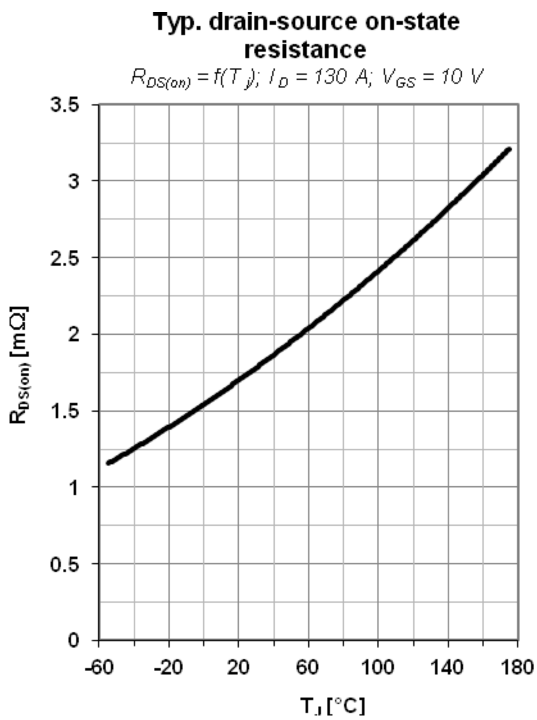


Max. transient thermal impedance
Z_THJC = f(t_p)
0.5
0.1
0.05
0.01
single pulse
Z_th,JC [K/W]
t_p [s]
10
1
0.1
0.01
0.001
0.0001
1E-06
1E-05
1E-04
1E-03
1E-02
1E-01
1E+00


Typ. output characteristic
$I_D = f(V_{DS})$; $T_j = 25\ °C$
200
150
100
50
0
0
1
2
I_D [A]
V_{DS} [V]
10V
7V
6V
5.5V
5V

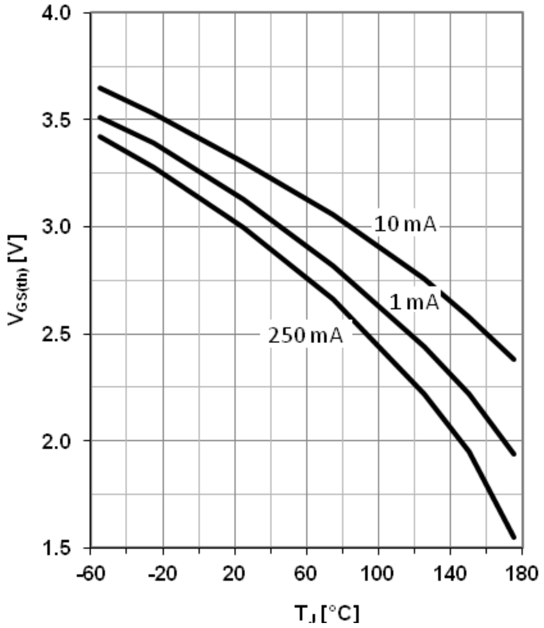

Typ. drain-source on-state resistance
$R_{DS(on)} = (I_D)$; $T_j = 25\ °C$
6
5
4
3
2
1
0
20
40
60
80
100
120
140
$R_{DS(on)}$ [mΩ]
I_D [A]
5V
5.5V
6V
7V
10V


Typ. Transfer characteristics
$I_D = f(V_{GS})$; $V_{DS} = 6V$
180
120
60
0
3
4
5
6
I_D [A]
V_{GS} [V]
25°C
175°C
-55°C


Typ. drain-source on-state resistance
$R_{DS(on)} = f(T_j)$; $I_D = 130\ A$; $V_{GS} = 10\ V$
3.5
3
2.5
2
1.5
1
0.5
0
-60
-20
20
60
100
140
180
$R_{DS(on)}$ [mΩ]
T_J [°C]

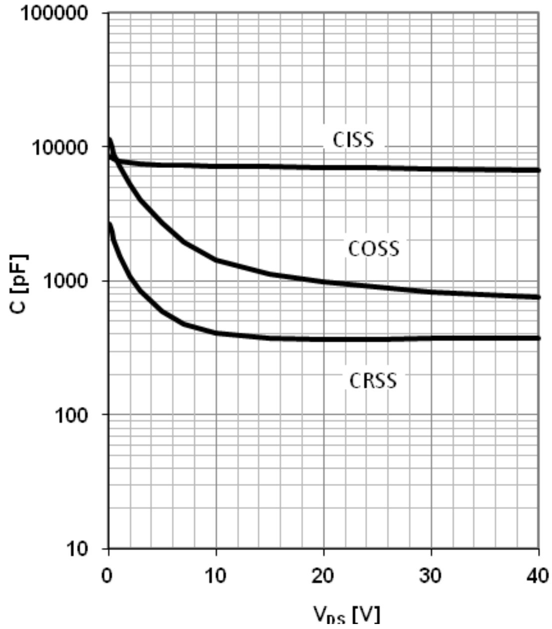
Typ. gate threshold voltage

$V_{GS(th)} = f(T_j)$; $V_{GS} = V_{DS}$



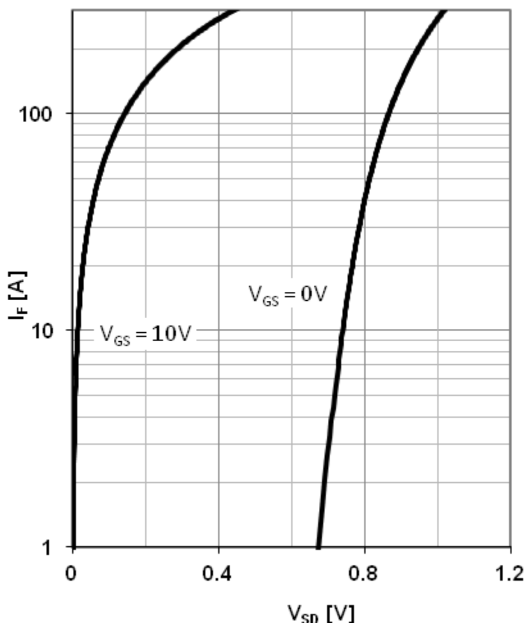
Typ. capacitances

$C = f(V_{DS})$; $V_{GS} = 0$ V; $f = 1$ MHz



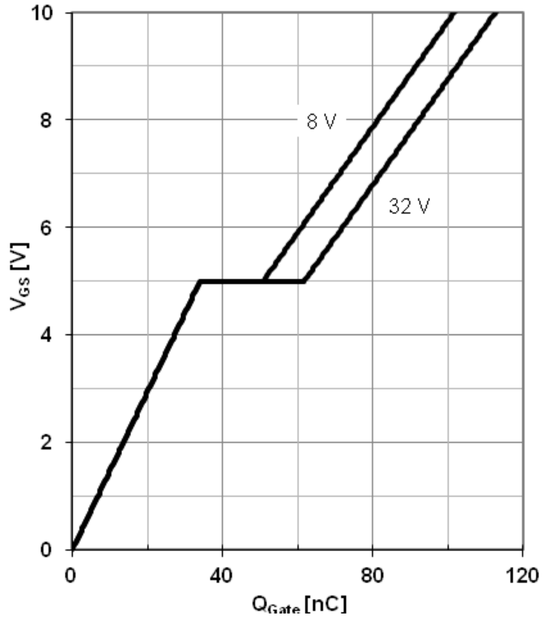
Typ. forward diode characterisitics

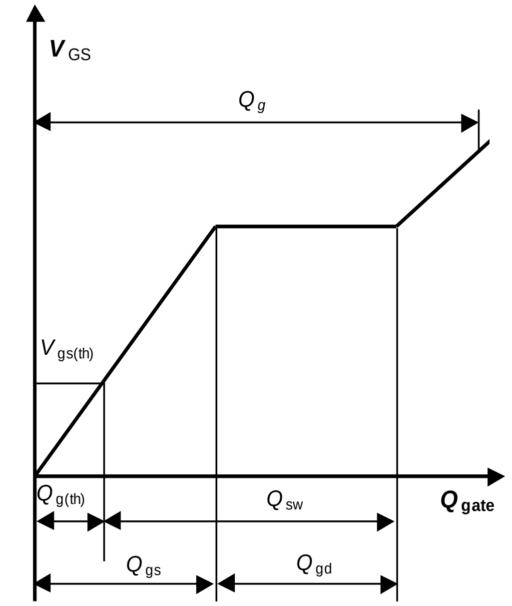
$IF = f(V_{SD})$



Typ. gate charge

$V_{GS} = f(Q_{gate})$; $I_D = 130$ A pulsed





1) Current is limited by assembly and interconnect technology and according to the following equation:

$$I_D = \sqrt{\frac{T_J - T_C}{R_{TH(J-C)} \cdot R_{DS(on)} @ T_{J(max)}}}$$

Considering RTH junction-to-heatsink, the maximum current is thermally limited according to the following equation:

$$I_D = \sqrt{\frac{T_J - T_{HS}}{R_{TH(J-HS)} \cdot R_{DS(on)} @ T_{j(max)}}}$$

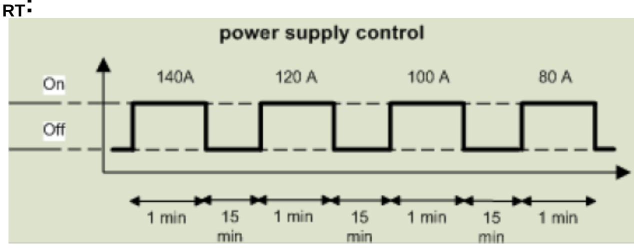
2) The RTH value is the equivalent RTH value for one chip. It is the sum of the RTH junction-to-case measured according to JEDEC JESD51-14 norm and the coupling RTH of the neighbor chips.

3) The 3 K/W thermal resistance junction-to-heatsink can be obtained by using typical silicon based thermal foils with a thickness of 200 µm. RTH values of 2.5 K/W can be obtained by using a 150 µm thick layer of thermal grease with a thermal conductivity of 3 W/mK.

Application notes:

Reverse Polarity Performance
For reverse polarity, the MOSFET body diodes heat up the complete MB0413A. Therefore, the junction carrying the maximum current will heat up also the other junctions (superior thermal cross coupling of MOSFETs), resulting in enhanced current capability.

Reverse voltage @ T_{RT}:

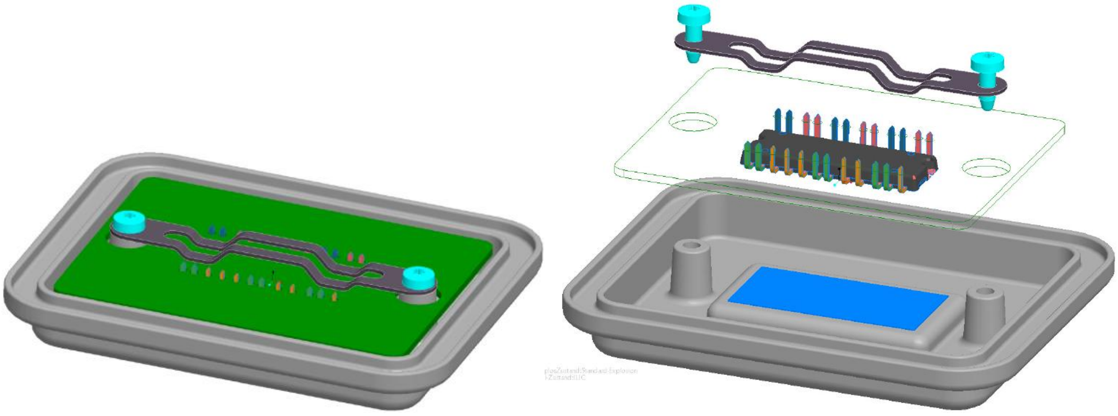


Mounting on PCB
1. Solder contacts are designed for through-hole technology (THT). Selective- or wave-soldering with Inno- or SAC-solder is recommended. Due to THT pins, high current leads can be contacted on all PCB layers without use of vias.
2. THT-Pins ensure high current capability of the MB0413A to inner PCB layers.

Fixation to heat sink
1. The MB0413A power module should be thermally contacted to a heat sink in order to achieve good thermal performance.
2. The thermal interface material (TIM) has to ensure electrical insulation of the module against the heatsink. Therefore no electrical conducting particles should be present between the module and the heatsink in order to avoid short circuits.
3. The fixture of the power module to a heatsink depends on the TIM used (see sketch below).
   a. Thermal glue, gap filler: typically no contact force (interface pressure) over life time needed. To ensure electrical insulation over life time, the use of spacers (for example glass beads) can be appropriate.
   b. Thermal grease: interface pressure according to TIM specification. To ensure electrical insulation, spacers (e.g. glass beads) can be used.
   c. Thermal pad: interface pressure according to TIM specification.

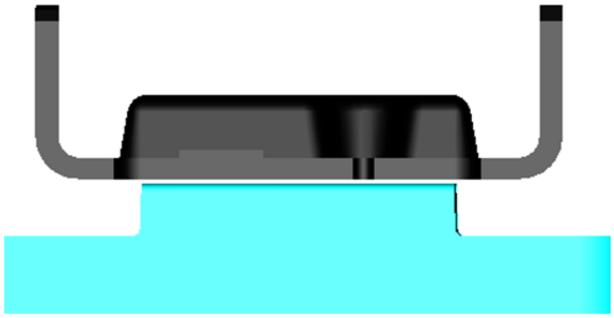
   In order to ensure good performance over life time, a constant pressure for all the working conditions should be applied on the module. This can be realized using a spring bar, fixed on the heatsink, and applying a force on the module as shown in the drawing below. The interface pressure should be chosen depending on the TIM.

Pressures around 100 PSI showed to give good results with typical materials. A maximum pressure of 2 N/mm^2 on the mold compound should not be exceeded.

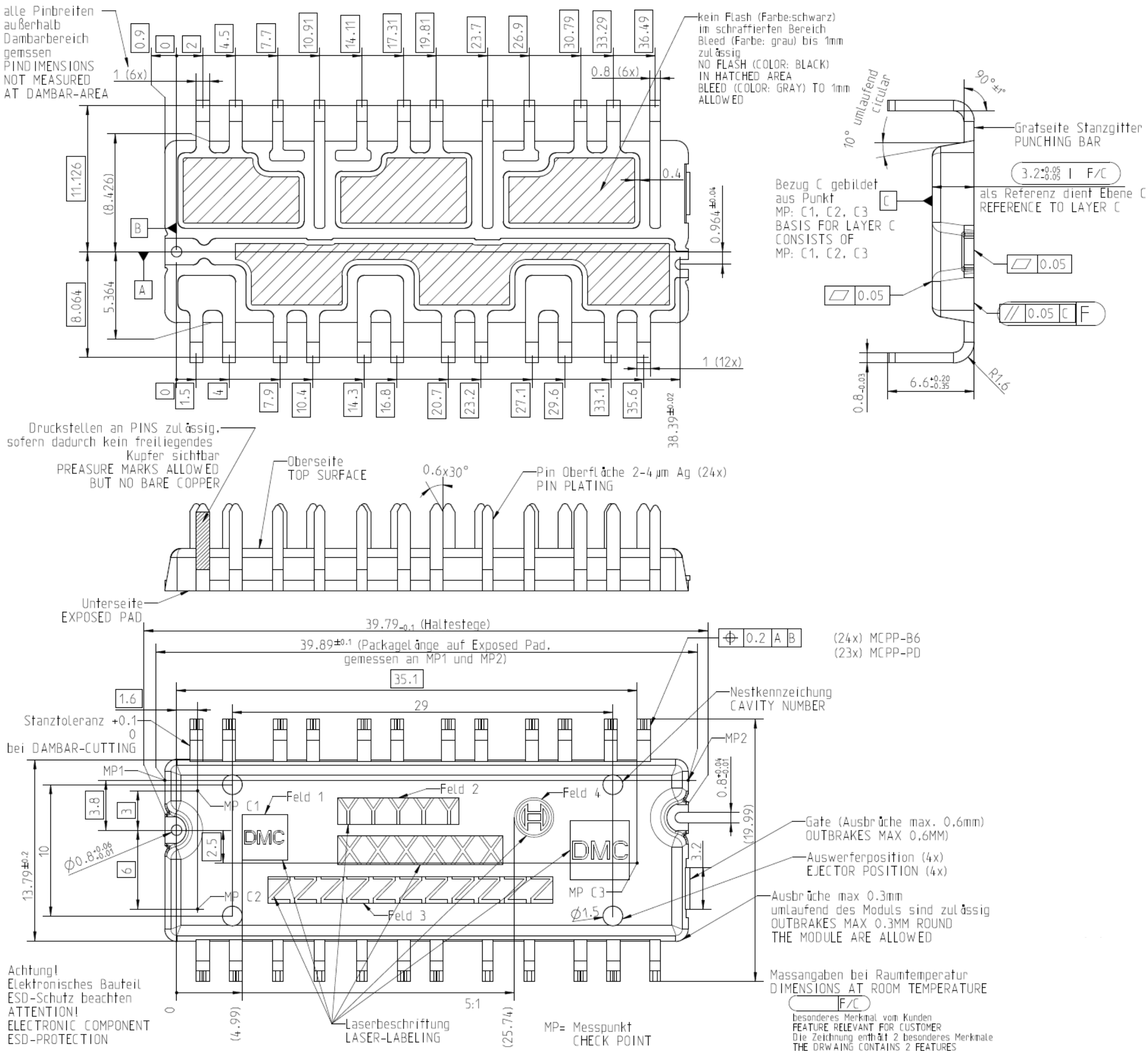


Design of heat sink

1. In case of possible humidity entry in combination with solder-flux-material between slug and heatsink activities against growth of dendrites should implemented e.g anodising of heatsink.
2. Other possibility is a step at heatsink. Area between heatsink and module must be filled complete with TIM.



Mechanical Dimensions:



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Data sheet version	Date	Changes
2.0	31.07.2013	First version
3.0	19.03.2015	Addition application notes, Tj, ESD protection, Rev. voltage test