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April 2016

# HUFA76413DK8T\_F085

## N-Channel Logic Level UltraFET® Power MOSFET

60V, 4.8A, 56mΩ

### General Description

These N-Channel power MOSFETs are manufactured using the innovative UltraFET® process. This advanced process technology achieves the lowest possible onresistance per silicon area, resulting in outstanding performance. This device is capable of withstanding high energy

in the avalanche mode and the diode exhibits very low reverse recovery time and stored charge. It was designed for use in applications where power efficiency is important, such as switching regulators, switching converters, motor drivers, relay drivers, low-voltage bus switches, and power management in portable and battery-operated products.

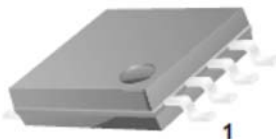


### Features

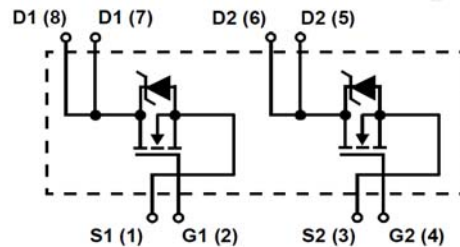
- 150°C Maximum Junction Temperature
- UIS Capability (Single Pulse and Repetitive Pulse)
- Ultra-Low On-Resistance  $r_{DS(ON)} = 0.049\Omega$ ,  $V_{GS} = 10V$
- Ultra-Low On-Resistance  $r_{DS(ON)} = 0.056\Omega$ ,  $V_{GS} = 5V$
- Qualified to AEC Q101
- RoHS Compliant

### Applications

- Motor and Load Control
- Powertrain Management



SO-8



### MOSFET Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Ratings	Units
$V_{DSS}$	Drain to Source Voltage	60	V
$V_{GS}$	Gate to Source Voltage	$\pm 16$	V
$I_D$	Drain Current -Continuous ( $T_C = 25^\circ\text{C}$ , $V_{GS} = 10V$ )	5.1	A
	-Continuous ( $T_C = 25^\circ\text{C}$ , $V_{GS} = 5V$ )	4.8	
	-Continuous ( $T_C = 125^\circ\text{C}$ , $V_{GS} = 5V$ , $R_{\theta JA} = 228^\circ\text{C/W}$ )	1	
	-Pulsed	Figure 4	
$E_{AS}$	Single Pulse Avalanche Energy (Note 1)	260	mJ
$P_D$	Power Dissipation	2.5	W
	Derate Above $25^\circ\text{C}$	0.02	W/ $^\circ\text{C}$
$T_J, T_{STG}$	Operating and Storage Temperature	-55 to +150	$^\circ\text{C}$

### Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance Junction to Ambient SO-8 (Note 2)	50	$^\circ\text{C/W}$
	Thermal Resistance Junction to Ambient SO-8 (Note 3)	191	
	Thermal Resistance Junction to Ambient SO-8 (Note 4)	228	

### Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
76413DK8	HUFA76413DK8T_F085	SO-8	330mm	12mm	2500 units

#### Notes:

- 1: Starting  $T_J = 25^\circ\text{C}$ ,  $L = 20\text{mH}$ ,  $I_{AS} = 5.1\text{A}$
- 2:  $R_{\theta JA}$  is  $50^\circ\text{C/W}$  when mounted on a  $0.5\text{ in}^2$  copper pad on FR-4 at 1 second.
- 3:  $R_{\theta JA}$  is  $191^\circ\text{C/W}$  when mounted on a  $0.027\text{ in}^2$  copper pad on FR-4 at 1000 seconds.
- 4:  $R_{\theta JA}$  is  $228^\circ\text{C/W}$  when mounted on a  $0.006\text{ in}^2$  copper pad on FR-4 at 1000 seconds.
- 5: A suffix as "...F085P" has been temporarily introduced in order to manage a double source strategy as Fairchild has officially announced in Aug 2014.

# Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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## Off Characteristics

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250\ \mu\text{A}$ , $V_{GS} = 0\ \text{V}$	60	-	-	V
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 55\ \text{V}$ , $V_{GS} = 0\ \text{V}$	-	-	1	$\mu\text{A}$
		$T_A = 150^\circ\text{C}$	-	-	250	
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 16\ \text{V}$	-	-	$\pm 100$	nA

## On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$ , $I_D = 250\ \mu\text{A}$	1	-	3	V
$r_{DS(on)}$	Static Drain to Source On Resistance	$I_D = 5.1\ \text{A}$ , $V_{GS} = 10\ \text{V}$	-	0.041	0.049	$\Omega$
		$I_D = 4.8\ \text{A}$ , $V_{GS} = 5\ \text{V}$	-	0.048	0.056	
		$I_D = 4.8\ \text{A}$ , $V_{GS} = 5\ \text{V}$ , $T_A = 150^\circ\text{C}$	-	0.091	0.106	

## Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = 25\ \text{V}$ , $V_{GS} = 0\ \text{V}$ , $f = 1\ \text{MHz}$	-	620	-	pF
$C_{oss}$	Output Capacitance		-	180	-	pF
$C_{rss}$	Reverse Transfer Capacitance		-	30	-	pF
$Q_{g(TOT)}$	Total Gate Charge at 10V	$V_{GS} = 0$ to $10\ \text{V}$	-	18	23	nC
$Q_{g(5)}$	Total Gate Charge at 5V	$V_{GS} = 0$ to $5\ \text{V}$	-	10	13	nC
$Q_{g(TH)}$	Threshold Gate Charge	$V_{GS} = 0$ to $1\ \text{V}$	-	0.6	0.8	nC
$Q_{gs}$	Gate to Source Charge	$V_{DD} = 30\ \text{V}$ , $I_D = 4.8\ \text{A}$ , $I_g = 1.0\ \text{mA}$	-	1.8	-	nC
$Q_{gd}$	Gate to Drain "Miller" Charge		-	5	-	nC

## Switching Characteristics ( $V_{GS}=5\text{V}$ )

$t_{on}$	Turn-On Time	$V_{DD} = 30\ \text{V}$ , $I_D = 1.0\ \text{A}$ , $V_{GS} = 5\ \text{V}$ , $R_{GS} = 16\ \Omega$	-	-	44	ns
$t_{d(on)}$	Turn-On Delay Time		-	10	-	ns
$t_r$	Rise Time		-	19	-	ns
$t_{d(off)}$	Turn-Off Delay Time		-	45	-	ns
$t_f$	Fall Time		-	27	-	ns
$t_{off}$	Turn-Off Time		-	-	108	ns

## Drain-Source Diode Characteristics

$V_{SD}$	Source to Drain Diode Forward Voltage	$I_{SD} = 4.8\ \text{A}$	-	-	1.25	V
		$I_{SD} = 2.4\ \text{A}$	-	-	1.0	
$t_{rr}$	Reverse Recovery Time	$I_{SD} = 4.8\ \text{A}$ , $dI_{SD}/dt = 100\ \text{A}/\mu\text{s}$	-	-	43	ns
$Q_{rr}$	Reverse Recovery Charge		-	-	55	nC

# Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

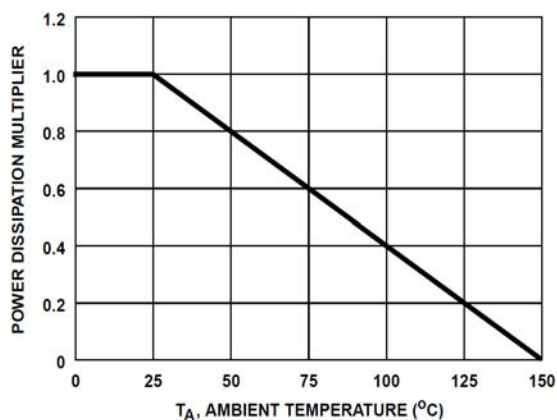


Figure 1. Normalized Power Dissipation vs. Ambient Temperature

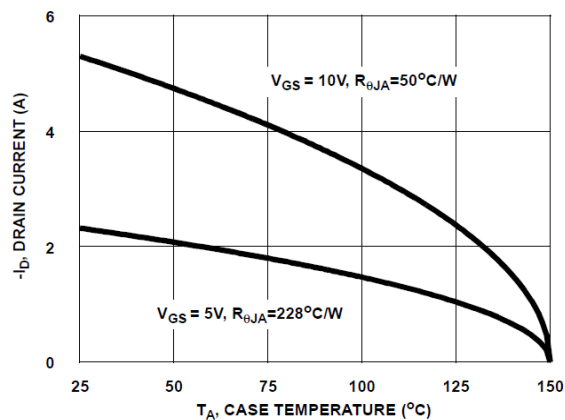


Figure 2. Maximum Continuous Drain Current vs. Case Temperature

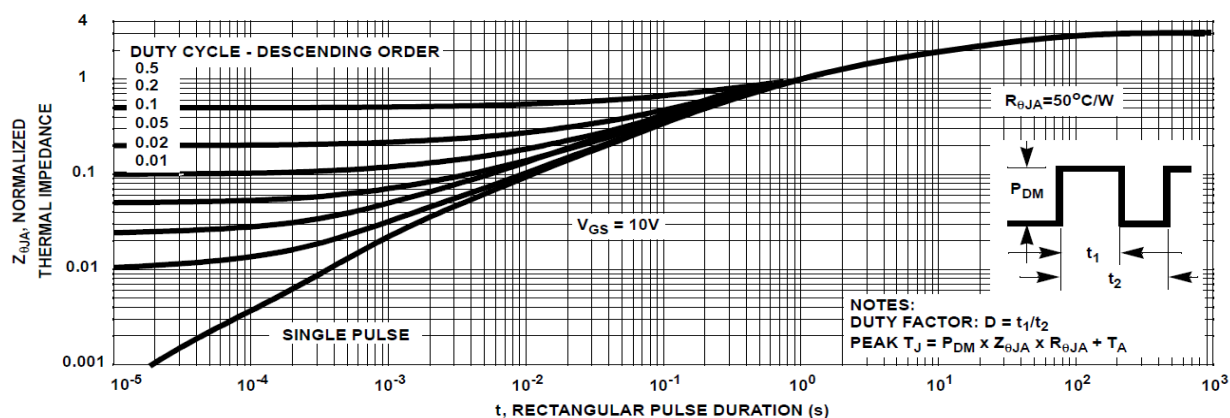


Figure 3. Normalized Maximum Transient Thermal Impedance

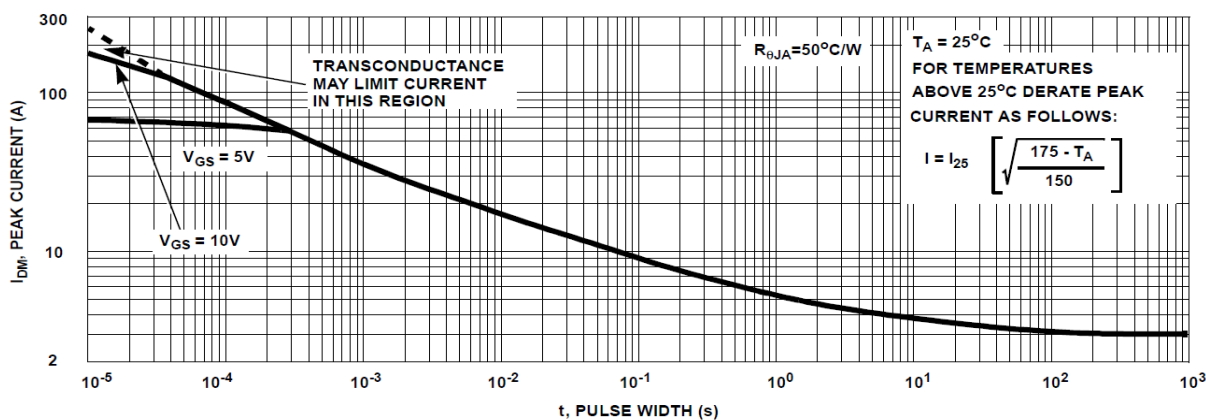


Figure 4. Peak Current Capability

# Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

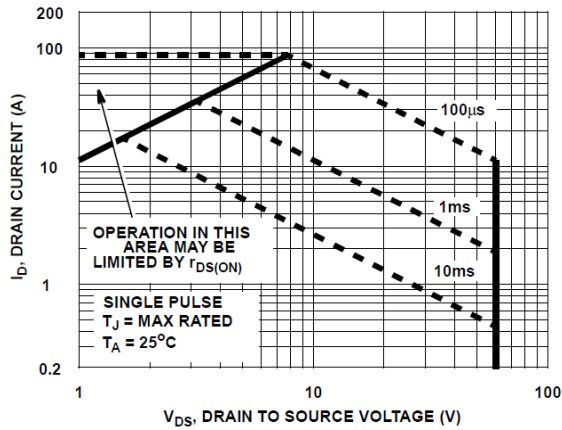


Figure 5. Forward Bias Safe Operating Area

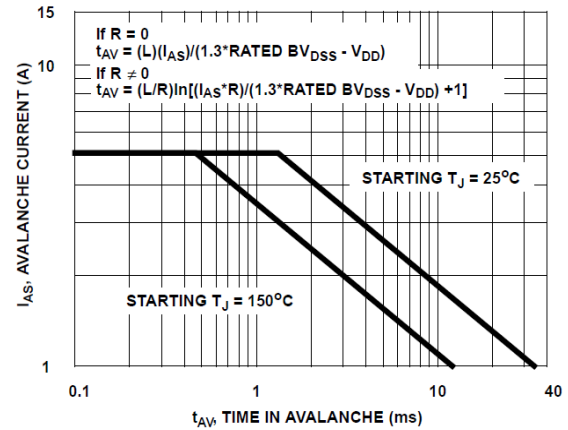


Figure 6. Unclamped Inductive Switching Capability

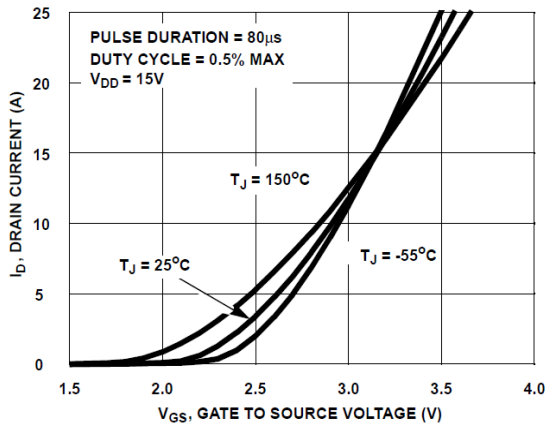


Figure 7. Transfer Characteristics

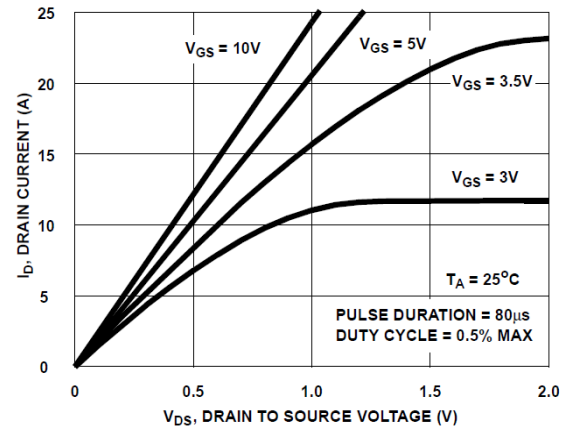


Figure 8. Saturation Characteristics

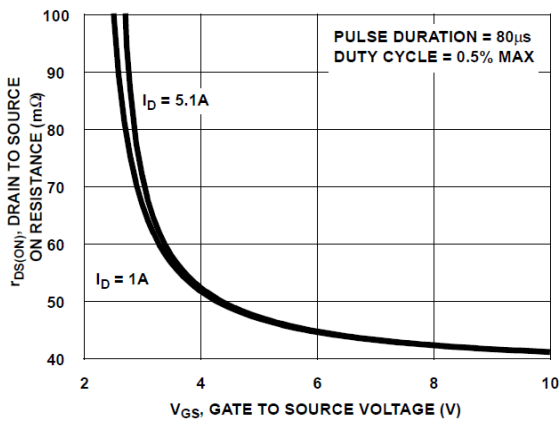


Figure 9. Drain to Source On Resistance vs. Gate Voltage and Drain Current

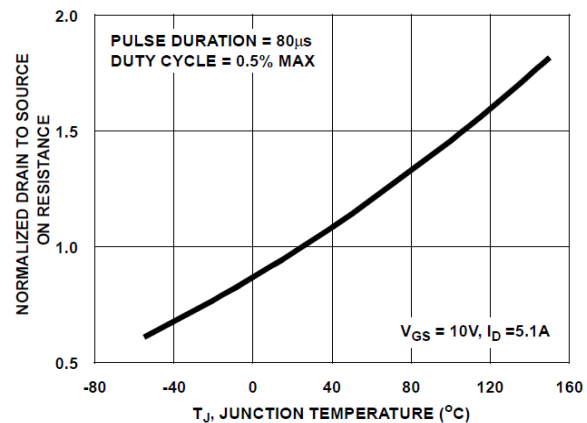


Figure 10. Normalized Drain to Source On Resistance vs. Junction Temperature

# Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

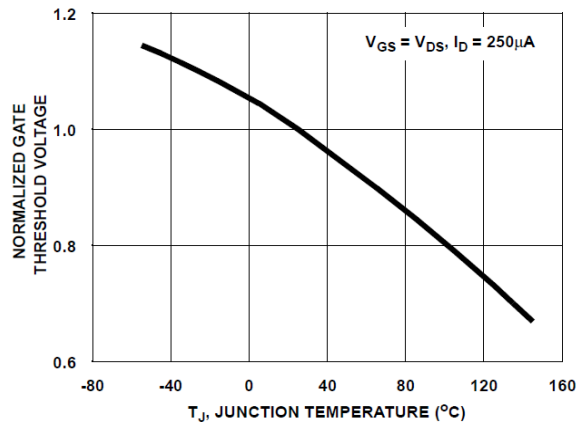


Figure 11. Normalized Gate Threshold Voltage vs. Junction Temperature

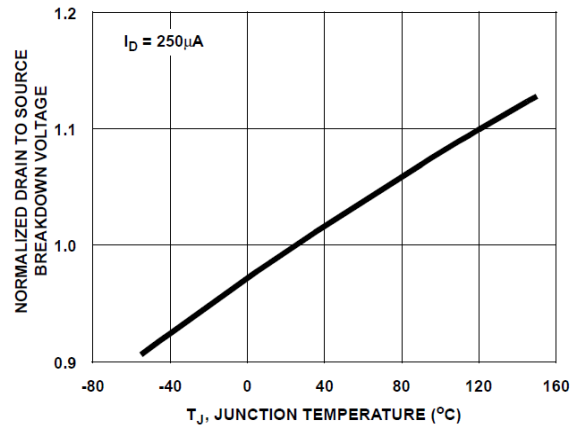


Figure 12. Normalized Drain to Source Breakdown Voltage vs. Junction Temperature

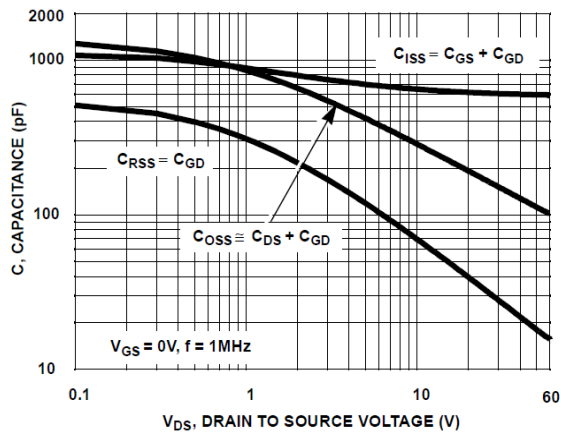


Figure 13. Capacitance vs. Drain to Source Voltage

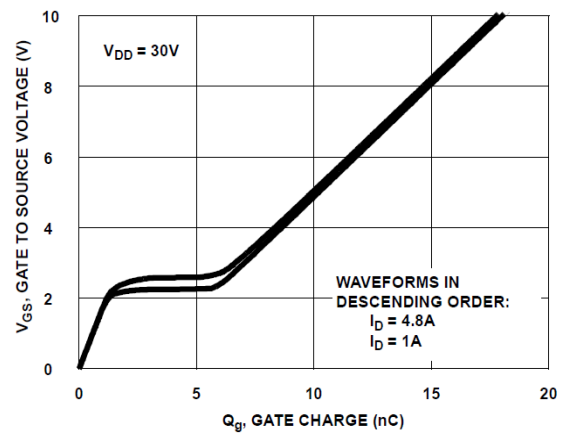


Figure 14. Gate Charge Waveforms for Constant Gate Currents

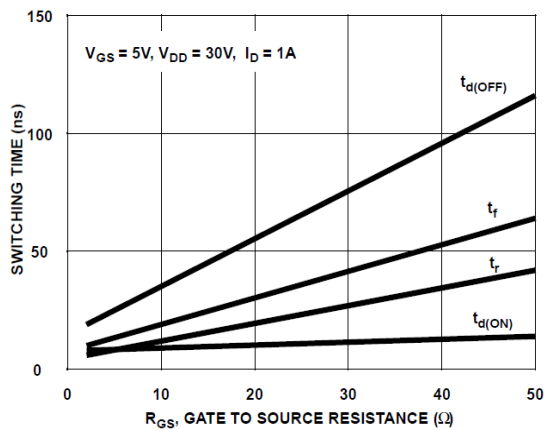
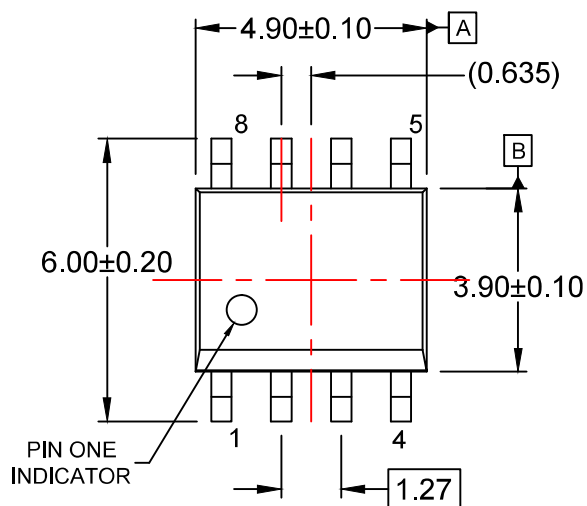
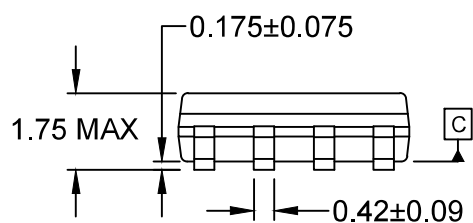
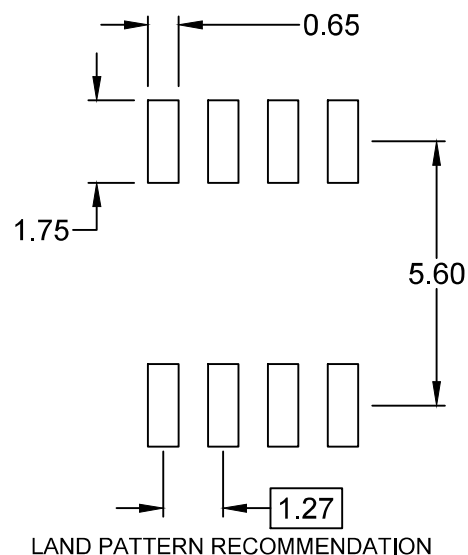


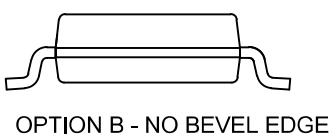
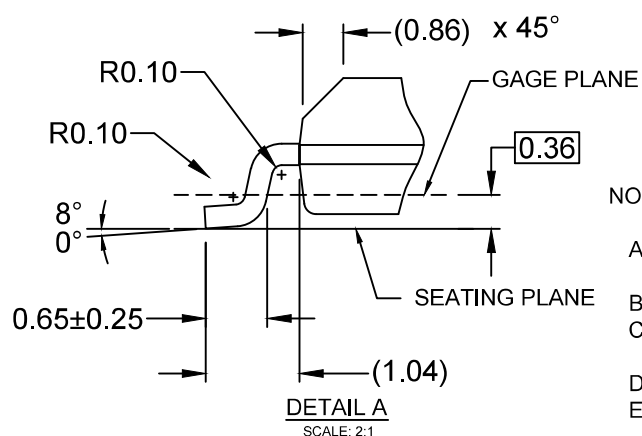
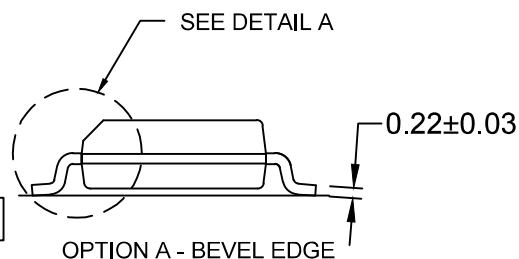
Figure 15. Switching Time vs Gate Resistance



$\oplus$  0.25(M) C B A



$\frac{1}{2}$  0.10



#### NOTES:

- A) THIS PACKAGE CONFORMS TO JEDEC MS-012, VARIATION AA.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.
- D) LANDPATTERN STANDARD: SOIC127P600X175-8M
- E) DRAWING FILENAME: M08Arev16



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