EL7584

4-Channel DC/DC Converter

FN7317
Rev 2.00
February 4, 2005

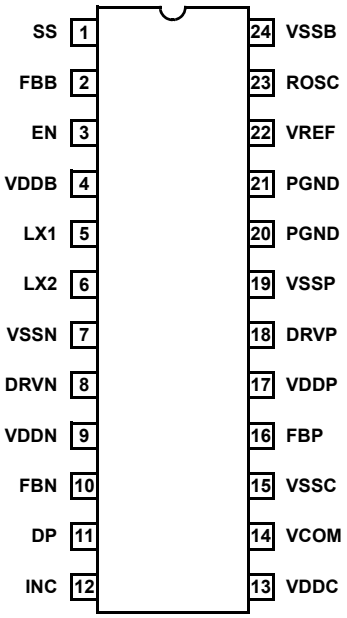
The EL7584 is a 4-channel DC/DC converter IC which is designed primarily for use in TFT-LCD applications. The boost converter has 2V to 14V input capability and provides 5V to 17V output, which powers the column drivers and provides up to 370mA @ 15V. A pair of charge pump control circuits provide outputs to allow the external generation of V_{ON} and V_{OFF} supplies at 5V to 40V and 0V to -40V, respectively, each at up to 60mA for V_{BOOST} = 15V. The V_{COM} buffer provides up to 50mA continuous output current from 2V to 13V.

The EL7584 features adjustable switching frequency and on-chip power sequence to simplify start-up operation. A separate input is available to externally increase the default delay of the positive charge pump. An over-temperature feature is provided to allow the IC to be automatically protected from excessive power dissipation.

The EL7584 is available in a 24-pin TSSOP package and is specified for operation over the full -40°C to +85°C temperature range.

Pinout

EL7584
(24-PIN TSSOP)
TOP VIEW



Features

- TFT-LCD display supply
  - Boost regulator
  - V_{COM} buffer
  - V_{ON} charge pump
  - V_{OFF} charge pump
- 2V to 14V V_{IN} supply
- 5V < V_{BOOST} < 17V
- 2V < V_{COM} < 13V
- 5V < V_{ON} < 40V
- -40V < V_{OFF} < 0V
- V_{BOOST} = 15V @ 370mA
- High frequency, small inductor DC/DC boost circuit
- Over 90% efficient DC/DC boost converter capability
- Built-in power-up sequence with adjustable V_{ON} delay
- Adjustable frequency
- Adjustable soft-start
- Adjustable outputs
- Over-temperature protection
- Small parts count
- Pb-free available (RoHS compliant)

Applications

- TFT-LCD panels
- PDAs

Ordering Information

PART NUMBER	PACKAGE	TAPE & REEL	PKG. DWG. #
EL7584IR	24-Pin TSSOP	-	MDP0044
EL7584IR-T7	24-Pin TSSOP	7”	MDP0044
EL7584IR-T13	24-Pin TSSOP	13”	MDP0044
EL7584IRZ (See Note)	24-Pin TSSOP (Pb-free)	-	MDP0044
EL7584IRZ-T7 (See Note)	24-Pin TSSOP (Pb-free)	7”	MDP0044
EL7584IRZ-T13 (See Note)	24-Pin TSSOP (Pb-free)	13”	MDP0044

NOTE: Intersil Pb-free products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Absolute Maximum Ratings (T_A = 25°C)

LX Pin Voltage 18V
V_{DDB}, V_{DDP}, V_{DDN} 18V
V_{DDC} 16.5V
Maximum Continuous V_{BOOST} Output Current. 800mA

Storage Temperature . . . . . .-65°C to +150°C
Ambient Operating Temperature . . . . . .-40°C to +85°C
Power Dissipation . . . . . See Curves

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typ values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

Electrical Specifications

V_{IN} = 3.3V, V_{BOOST} = 12V, R_{OSC} = 62kΩ, T_A = 25°C, Unless Otherwise Specified.

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
DC/DC BOOST CONVERTER						
IQ1_B	Quiescent Current - Shut-down	EN = 0V		0.8	10	µA
IQ2_B	Quiescent Current - Switching	EN = V_{DDB}		4.8	8	mA
V(FBB)	Feedback Voltage		1.275	1.300	1.325	V
V_{REF}	Reference Voltage		1.260	1.310	1.360	V
V_{ROSC}	Oscillator Set Voltage		1.260	1.325	1.390	V
I(FBB)	Feedback Input Bias Current			0.1		µA
V_{DDB}	Boost Converter Supply Range		2		17	V
D_{MAX}	Maximum Duty Cycle		85	92		%
$I(LX)_{MAX}$	Peak Internal FET Current			1.75		A
R_{DS-ON}	Switch On Resistance	at V_{BOOST} = 10V, I(LX) total = 350mA		0.22		Ω
$I_{LEAK-SWITCH}$	Switch Leakage Current	I(LX) total			1	µA
V_{BOOST}	Output Range	$V_{BOOST} > V_{IN} + V_{DIODE}$	5		17	V
$\Delta V_{BOOST}/\Delta V_{IN}$	Line Regulation	2.7V < V_{IN} < 13.2V, V_{BOOST} = 15V		0.1		%
$\Delta V_{BOOST}/\Delta I_{O1}$	Load Regulation	50mA < I_{O1} < 250mA		0.5		%
$F_{OSC-RANGE}$	Frequency Range	R_{OSC} range = 240kΩ to 60kΩ	200		1200	kHz
F_{OSC1}	Switching Frequency	R_{OSC} = 62kΩ	900	1000	1100	kHz
V_{COM} BUFFER						
V_{DDC}	Supply Voltage Range		6		15	V
IQ1, V_{DDC}	V_{DDC} Disable Current	V_{DDC} = 12V, EN = 0V		5.5	20	µA
IQ2, V_{DDC}	V_{DDC} Enable Current	V_{DDC} = 12V, V_{EN} = V_{DDB}, no load		1.7	5	mA
V_{COM}-offset	Accuracy of V_{COM} Output Voltage	2V < V_{COM} < (V_{DDC} - 2V)	-10		+10	mV
I(INC)	V_{COM} Input Bias Currents	Current magnitude	-0.1	0.01	0.1	µA
$R_O(V_{COM})$	V_{COM} Output Impedance	V_{DDC} = V_{BOOST} = 12V, V_{COM} = 6V with -100mA < I_{LOAD} < 100mA C_{LOAD} for V_{COM} > 0.47µF, MLCC		0.25		Ω
I_{COM}(max)	Output Current Limit			150		mA
PSRR	Supply Voltage Rejection	V_{INC} = $V_{DDC/2}$, 9V < V_{DDC} < 15V	60	102		dB
CMRR	Common Mode Voltage Rejection	V_{DDC} = 12V, 2V < V_{INC} < 10V	60	93		dB

Electrical Specifications V_{IN} = 3.3V, V_{BOOST} = 12V, R_{OSC} = 62kΩ, T_A = 25°C, Unless Otherwise Specified. **(Continued)**

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
POSITIVE REGULATED CHARGE PUMP (V_{ON}) Most positive V_{ON} output depends on the magnitude of the V_{DDP} input voltage (normally connected to V_{BOOST}) and the external component configuration (doubler or tripler)						
V_{DDP}	Supply Input for Positive Charge Pump	Usually connected to V_{BOOST} output	5		17	V
$IQ1(V_{DDP})$	Quiescent Current - Shut-down	EN = 0V		11.5	20	µA
$IQ2(V_{DDP})$	Quiescent Current - Switching	EN = V_{DDB}		2.3	5	mA
I_{DP1}	Disable Charge Current	EN = 0V, DP = 0V	1.5	1.9	2.5	mA
I_{DP2}	Enable Discharge Current	EN = V_{DDB}, DP = 5V	100	200	300	nA
V(FBP)	Feedback Reference Voltage		1.245	1.310	1.375	V
I(FBP)	Feedback Input Bias Current			0.1		µA
I(DRVP)	RMS DRVP Output Current	V_{DDP} = 12V		60		mA
		V_{DDP} = 6V	15			mA
ILR_V_{ON}	Load Regulation	5mA < I_L < 15mA	-0.5	0.03	0.5	%/mA
F_{PUMP}	Charge Pump Frequency	Frequency set by R_{OSC} - see boost section		$0.5*F_{OSC}$		
NEGATIVE REGULATED CHARGE PUMP (V_{OFF}) Most negative V_{OFF} output depends on the magnitude of the V_{DDN} input voltage (normally connected to V_{BOOST}) and the external component configuration (doubler or tripler)						
V_{DDN}	Supply Input for Negative Charge Pump	Usually connected to V_{BOOST} output	5		17	V
$IQ1(V_{DDN})$	Quiescent Current - Shut-down	ENBN = 0V		4.5	20	µA
$IQ2(V_{DDN})$	Quiescent Current - Switching	ENBN = V_{DDB}		2.3	5	mA
V(FBN)	Feedback Reference Voltage		-80	0	+80	mV
I(FBN)	Feedback Input Bias Current	Magnitude of input bias		0.1		µA
I(DRVN)	RMS DRVN Output Current	V_{DDN} = 12V		60		mA
		V_{DDN} = 6V	15			mA
ILR_V_{OFF}	Load Regulation	-15mA < I_L < -5mA	-0.5	0.03	0.5	%/mA
F_{PUMP}	Charge Pump Frequency	Frequency set by R_{OSC} - see boost section		$0.5*F_{OSC}$		
ENABLE CONTROL LOGIC						
V_{HI}-EN	Enable Input High Threshold		1.6			V
V_{LO}-EN	Enable Input Low Threshold				0.5	V
I(EN)	Enable Input Bias Current	V_{EN} = 5V		3.7	7.5	µA
OVER-TEMPERATURE PROTECTION						
T_{OT}	Over-temperature Threshold			130		°C
T_{HYS}	Over-temperature Hysteresis			40		°C

Pin Descriptions

I = Input, O = Output, S = Supply

PIN NUMBER	PIN NAME	PIN TYPE	PIN FUNCTION
1	SS	I	Soft-Start input: a capacitor determines the current limit ramp time.
2	FBB	I	Voltage feedback input determines the value of V_{BOOST}.
3	EN	I	Starts internal power sequencing of V_{BOOST}, V_{OFF}, V_{COM} and V_{ON} outputs (See Applications Information) ; active HIGH input.
4	VDDB	P	Positive supply for V_{BOOST} DC/DC controller.
5	LX1	O	Boost inductor saturating MOSFET #1.
6	LX2	O	Boost inductor saturating MOSFET #2.
7	VSSN*	P	Ground return for V_{OFF} regulator.
8	DRVN	O	Pump capacitor driver for V_{OFF} regulator.
9	VDDN	P	Positive supply for V_{OFF} regulator.
10	FBN	I	Voltage feedback input determines the value of V_{OFF}.
11	DP	I	An external capacitor increases V_{ON} power up delay time.
12	INC	I	V_{COM} Buffer input.
13	VDDC	P	Positive supply for V_{COM} Buffer.
14	VCOM	O	V_{COM} Buffer output.
15	VSSC*	P	Ground return for V_{COM} Buffer.
16	FBP	I	Voltage feedback input determines the value of V_{ON}.
17	VDDP	P	Positive supply for V_{ON} regulator.
18	DRVP	O	Pump capacitor driver for V_{ON} regulator.
19	VSSP*	P	Ground return for V_{ON} regulator.
20	PGND*	P	Ground return for MOSFET #1.
21	PGND*	P	Ground return for MOSFET #2.
22	VREF	O	Voltage reference for V_{OFF} feedback .
23	ROSC	I	An external resistor sets the DC/DC switching frequency.
24	VSSB*	P	Ground return for V_{BOOST} DC/DC controller.

NOTE: *VSSB, VSSC, VSSN, VSSP, and PGND (2) are shorted internally to the device substrate.

Typical Performance Curves

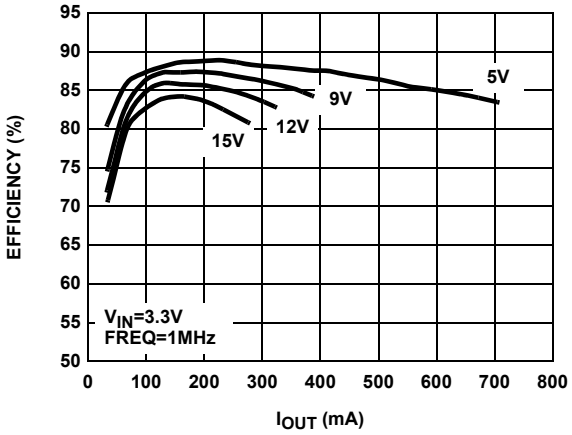


FIGURE 1. EFFICIENCY vs I_{OUT}

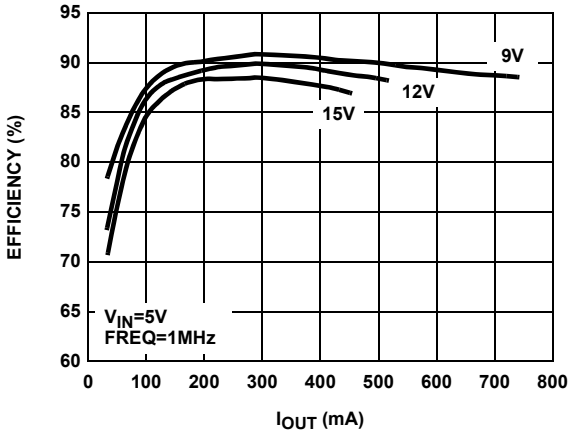


FIGURE 2. EFFICIENCY vs I_{OUT}

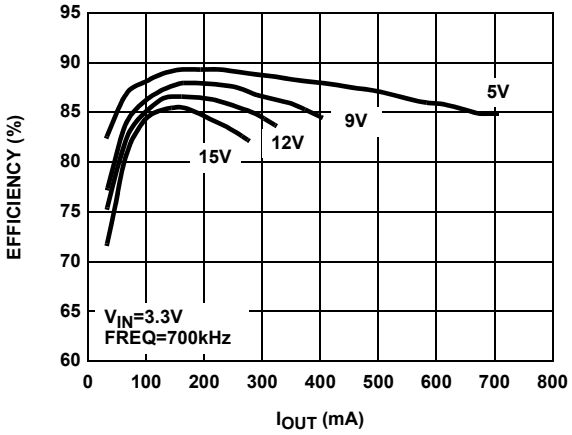


FIGURE 3. EFFICIENCY vs I_{OUT}

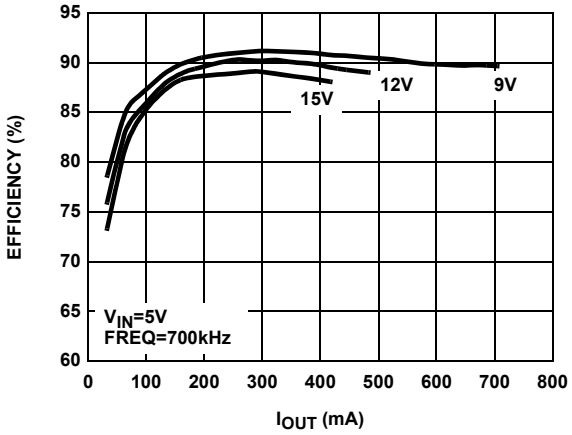


FIGURE 4. EFFICIENCY vs I_{OUT}

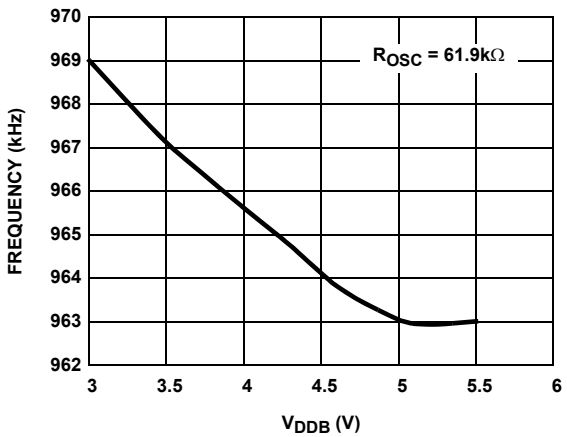


FIGURE 5. F_S vs V_{DDB}

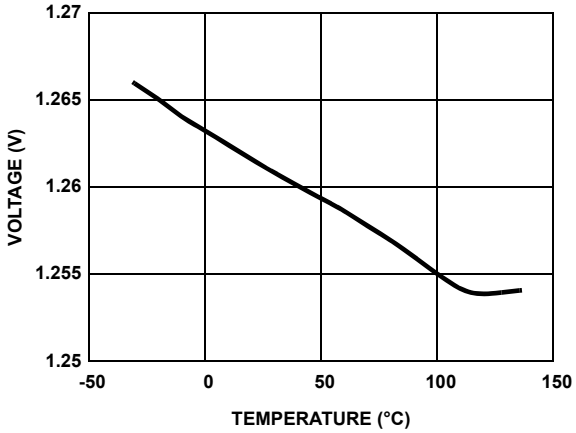


FIGURE 6. V_{REF} vs TEMPERATURE

Typical Performance Curves (Continued)

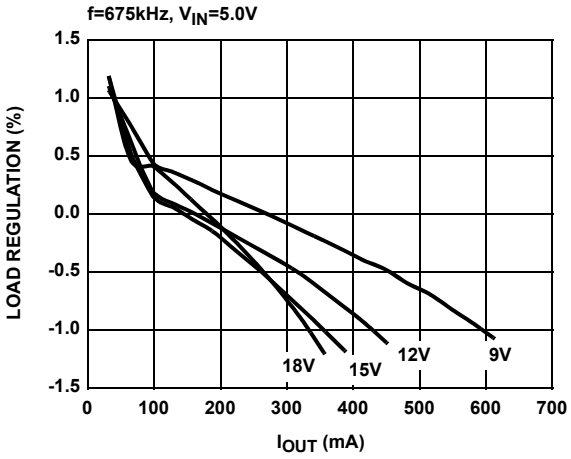


FIGURE 7. LOAD REGULATION vs I_{OUT}

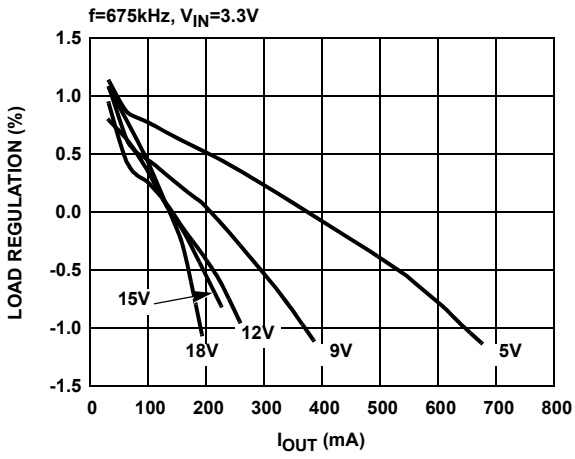


FIGURE 8. LOAD REGULATION vs I_{OUT}

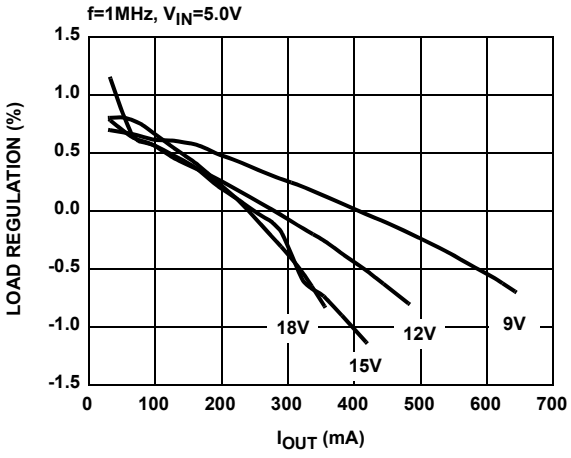


FIGURE 9. LOAD REGULATION vs I_{OUT}

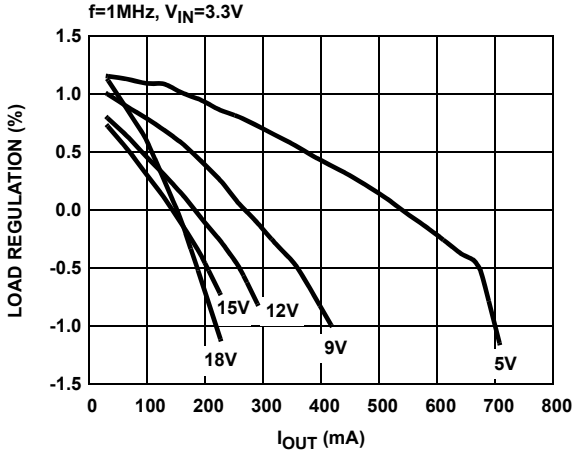


FIGURE 10. LOAD REGULATION vs I_{OUT}

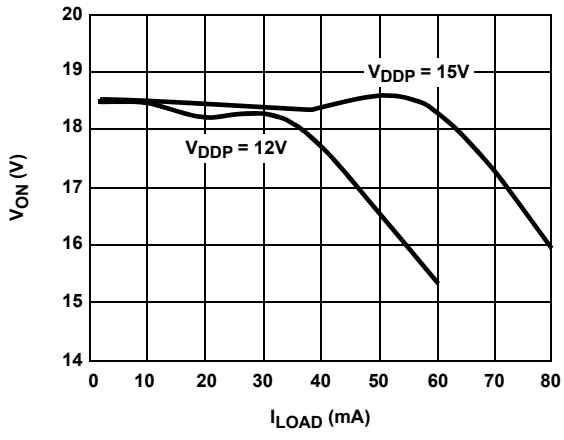


FIGURE 11. V_{ON} vs I_{ON}

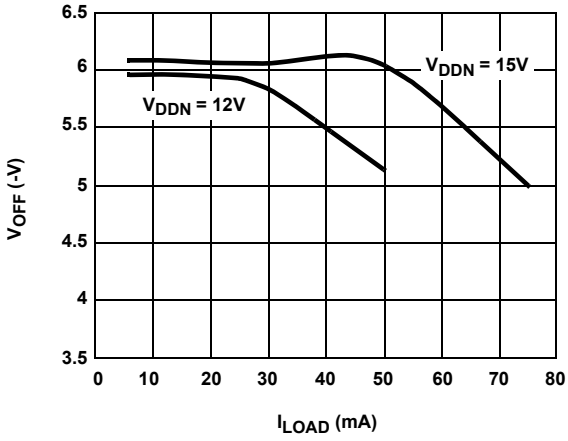


FIGURE 12. V_{OFF} vs I_{OFF}

Typical Performance Curves (Continued)

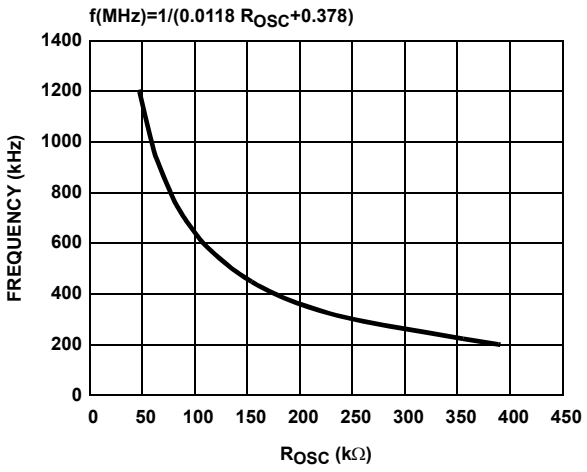


FIGURE 13. F_S vs R_{OSC}

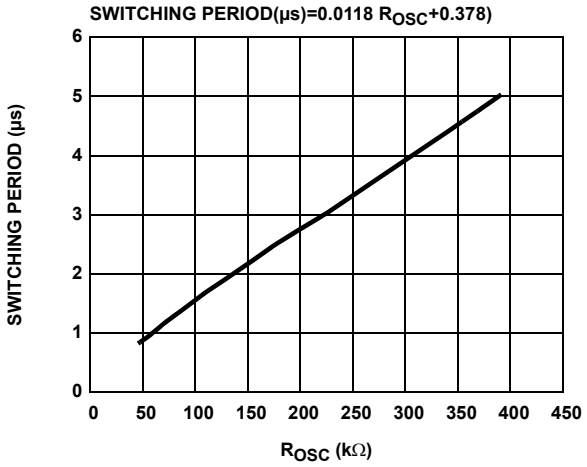


FIGURE 14. F_S vs R_{OSC}

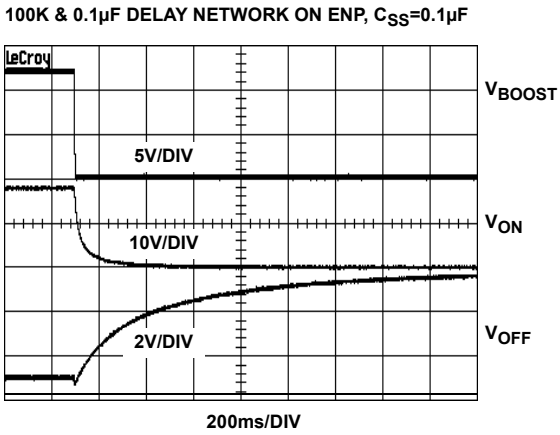


FIGURE 15. POWER-DOWN

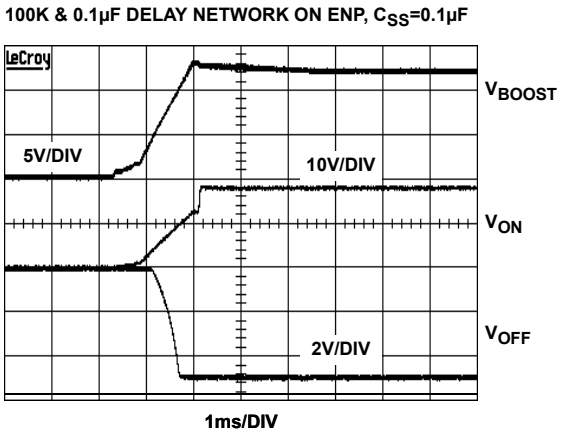


FIGURE 16. POWER-UP

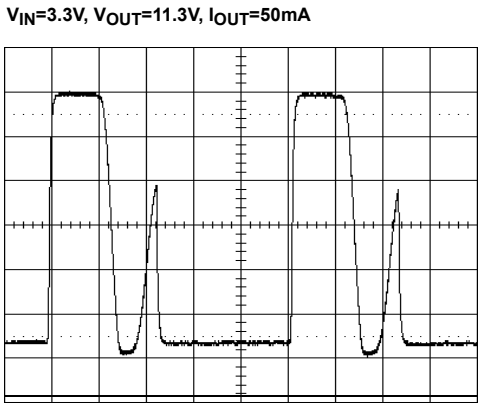


FIGURE 17. LX WAVEFORM - DISCONTINUOUS MODE

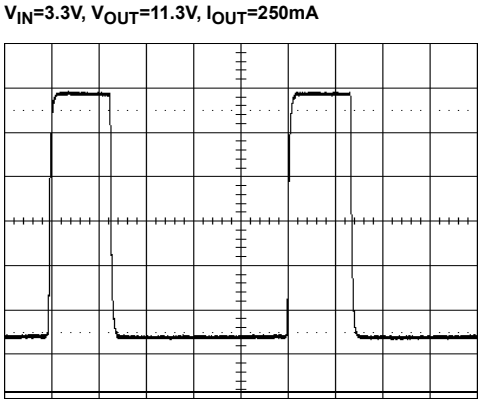


FIGURE 18. LX WAVEFORM - CONTINUOUS MODE

Typical Performance Curves (Continued)

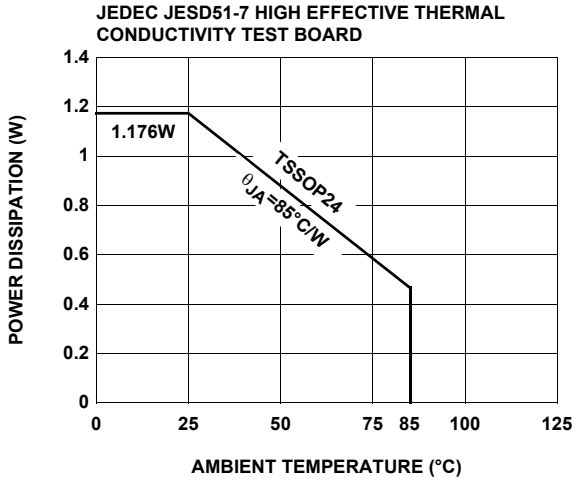


FIGURE 19. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

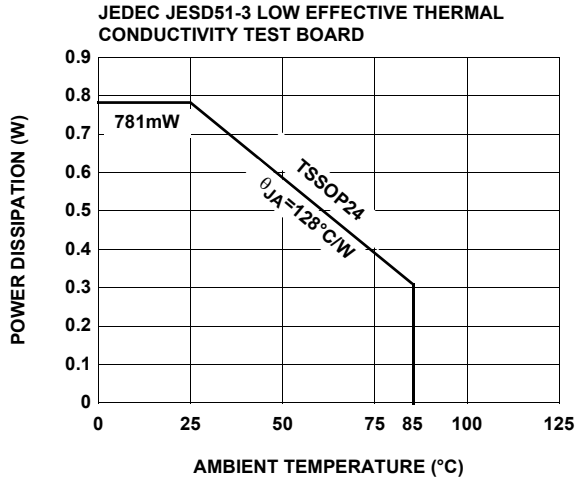
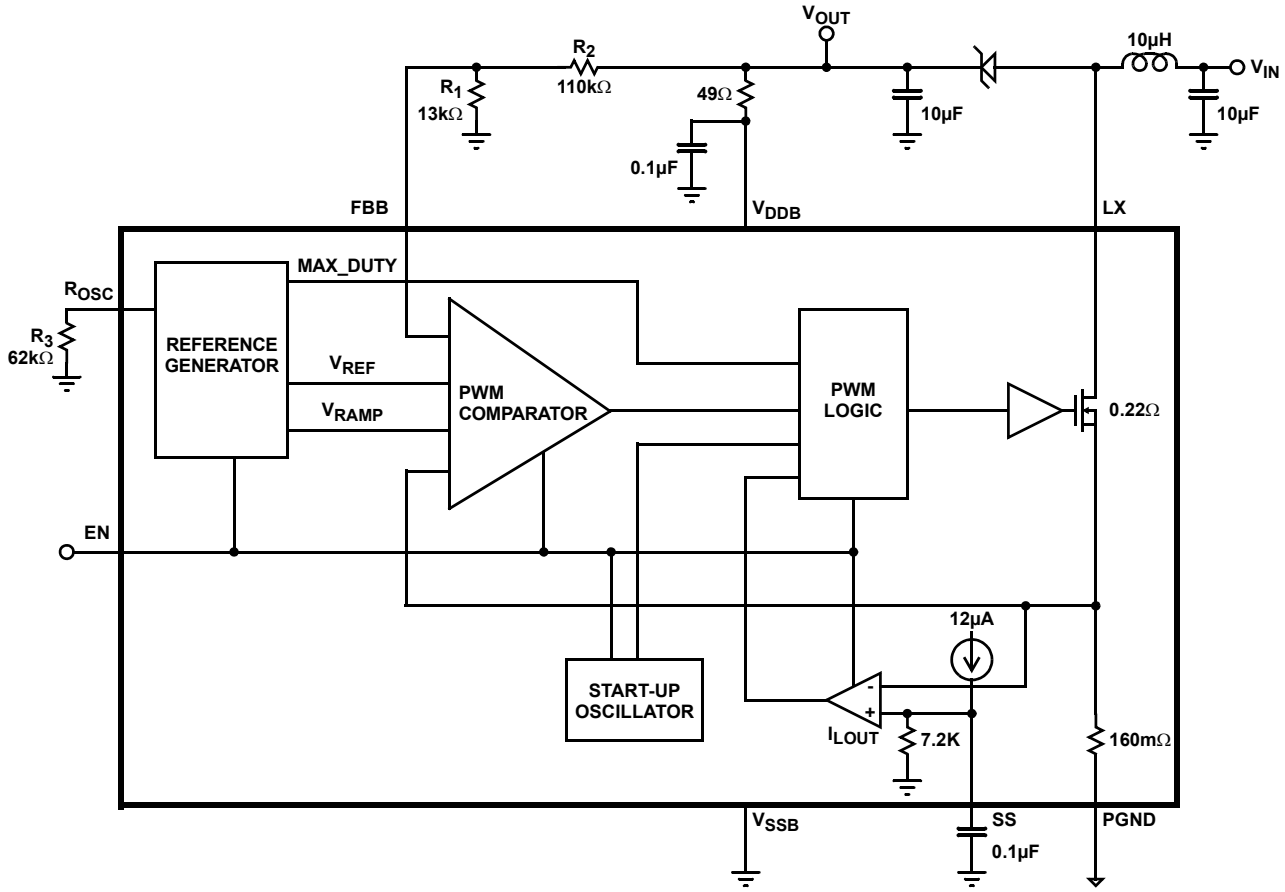


FIGURE 20. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

Functional Block Diagram



Applications Information

The EL7584 is high efficiency multiple output power solution designed specifically for thin-film transistor (TFT) liquid crystal display (LCD) applications. The device contains one high current boost converter and two low power charge pumps (V_{ON} and V_{OFF}).

The boost converter contains an integrated N-channel MOSFET to minimize the number of external components. The converter output voltage can be set from 5V to 18V with external resistors. The V_{ON} and V_{OFF} charge pumps are independently regulated to positive and negative voltages using external resistors. Output voltages as high as 40V can be achieved with additional capacitors and diodes.

Boost Converter

The boost converter operates in constant frequency pulse-width-modulation (PWM) mode. Quiescent current for the EL7584 is only 5mA when enabled, and since only the low side MOSFET is used, switch drive current is minimized. 90% efficiency is achieved in most common application operating conditions.

A functional block diagram with typical circuit configuration is shown on previous page. Regulation is performed by the PWM comparator which regulates the output voltage by comparing a divided output voltage with an internal reference voltage. The PWM comparator outputs its result to the PWM logic. The PWM logic switches the MOSFET on and off through the gate drive circuit. Its switching frequency is external adjustable with a resistor from timing control pin (R_{OSC}) to ground. The boost converter has 200kHz to 1.2MHz operating frequency range.

Start-Up

After V_{DDB} reaches a threshold of about 2V, the power MOSFET is controlled by the start-up oscillator, which generates fixed duty-ratio of 0.5 - 0.7 at a frequency of several hundred kilohertz. This will boost the output voltage, providing the initial output current load is not too great (<250mA).

When V_{DDB} reaches about 3.7V, the PWM comparator takes over the control. The duty ratio will be decided by the multiple-input direct summing comparator, Max_Duty signal (about 90% duty-ratio), and the Current Limit Comparator, whichever is the smallest.

The soft-start is provided by the current limit comparator. As the internal 12µA current source charges the external soft-start capacitor, the peak MOSFET current is limited by the voltage on the capacitor. This in turn controls the rising rate of output voltage.

The regulator goes through the start-up sequence as well after the EN signal is pulled to HI.

Steady-State Operation

When the output reaches the preset voltage, the regulator operates at steady state. Depending on the input/output condition and component, the inductor operates at either continuous-conduction mode or discontinuous-conduction mode.

In the continuous-conduction mode, the inductor current is a triangular waveform and LX voltage a pulse waveform. In the discontinuous-conduction mode, the inductor current is completely 'dried-out' before the MOSFET is turned on again. The input voltage source, the inductor, and the MOSFET and output diode parasitic capacitors forms a resonant circuit. Oscillation will occur in this period. This oscillation is normal and will not affect the regulation.

At very low load, the MOSFET will skip pulse sometimes. This is normal.

Current Limit

The MOSFET is current limited to <1.75Amps (nominal). This restricts the maximum output current I_{OMAX} based on the following formula:

$$I_{OMAX} = \left(I_{LMT} - \frac{\Delta I_L}{2}\right) \times \frac{V_{IN}}{V_O}$$

where:

- ΔI_L is the inductor peak-to-peak current ripple and is decided by:

$$\Delta I_L = \frac{V_{IN}}{L} \times \frac{D}{F_S}$$

- D is the MOSFET turn-on radio and is decided by:

$$D = \frac{V_O - V_{IN}}{V_O}$$

- F_S is the switching frequency.

The following table gives typical values:
(Margins are considered 10%, 3%, 20%, 10%, and 15% on V_{IN}, V_O, L, F_S, and I_{LMT}, respectively)

TABLE 1. MAXIMUM CONTINUOUS OUTPUT CURRENT

V_{IN} (V)	V_O (V)	L (MH)	F_S (kHz)	I_{OMAX} (mA)
3.3	9	10	1000	430
3.3	12	10	1000	320
3.3	15	10	1000	250
5	9	10	1000	650
5	12	10	1000	470
5	15	10	1000	370
12	18	10	1000	830

Component Considerations

Input Capacitor

It is recommended that C_{IN} is larger than 10µF. Theoretically, the input capacitor has ripple current of ΔI_L. Due to high-frequency noise in the circuit, the input current ripple may exceed the theoretical value. Larger capacitor will reduce the ripple further.

Boost Inductor

The inductor has peak and average current decided by:

$$I_{LPK} = I_{LAVG} + \frac{\Delta I_L}{2}$$

$$I_{LAVG} = \frac{I_O}{1 - D}$$

The inductor should be chosen to be able to handle this current. Furthermore, due to the fixed internal compensation, it is recommended that maximum inductance of 10µH and 15µH to be used in the 5V and 12V or higher output voltage, respectively.

The output diode has average current of I_O, and peak current the same as the inductor's peak current. Schottky diode is recommended and it should be able to handle those currents.

Feedback Resistor Network

An external resistor divider is required to divide the output voltage down to the nominal reference voltage. Current drawn by the resistor network should be limited to maintain the overall converter efficiency. The maximum value of the resistor network is limited by the feedback input bias current and the potential for noise being coupled into the feedback pin. A resistor network in the order of 200kΩ is recommended. The boost converter output voltage is determined by the following relationship:

$$V_{BOOST} = \frac{R_1 + R_2}{R_1} \times V_{FBB}$$

where V_{FBB} is 1.300V.

Schottky Diode

Speed, forward voltage drop, and reverse current are the three most critical specifications for selecting the Schottky diode. The entire output current flows through the diode, so the diode average current is the same as the average load current and the peak current is the same as the inductor peak current. When selecting the diode, one must consider the forward voltage drop at the peak diode current. On the Elantec demo board, MBRM120 is selected. Its forward voltage drop is 450mV at 1A forward current.

Output Capacitor

The EL7584 is specially compensated to be stable with capacitors which have a worst-case minimum value of 10µF at the particular V_{OUT} being set. Output ripple voltage requirements also determine the minimum value and the type of capacitors. Output ripple voltage consists of two components - the voltage drop caused by the switching current though the ESR of the output capacitor and the charging and discharging of the output capacitor:

$$V_{RIPPLE} = I_{LPK} \times ESR + \frac{V_{OUT} - V_{IN}}{V_{OUT}} \times \frac{I_{OUT}}{C_{OUT} \times FS}$$

For low ESR ceramic capacitors, the output ripple is dominated by the charging/discharging of the output capacitor.

In addition to the voltage rating, the output capacitor should also be able to handle the RMS current is given by:

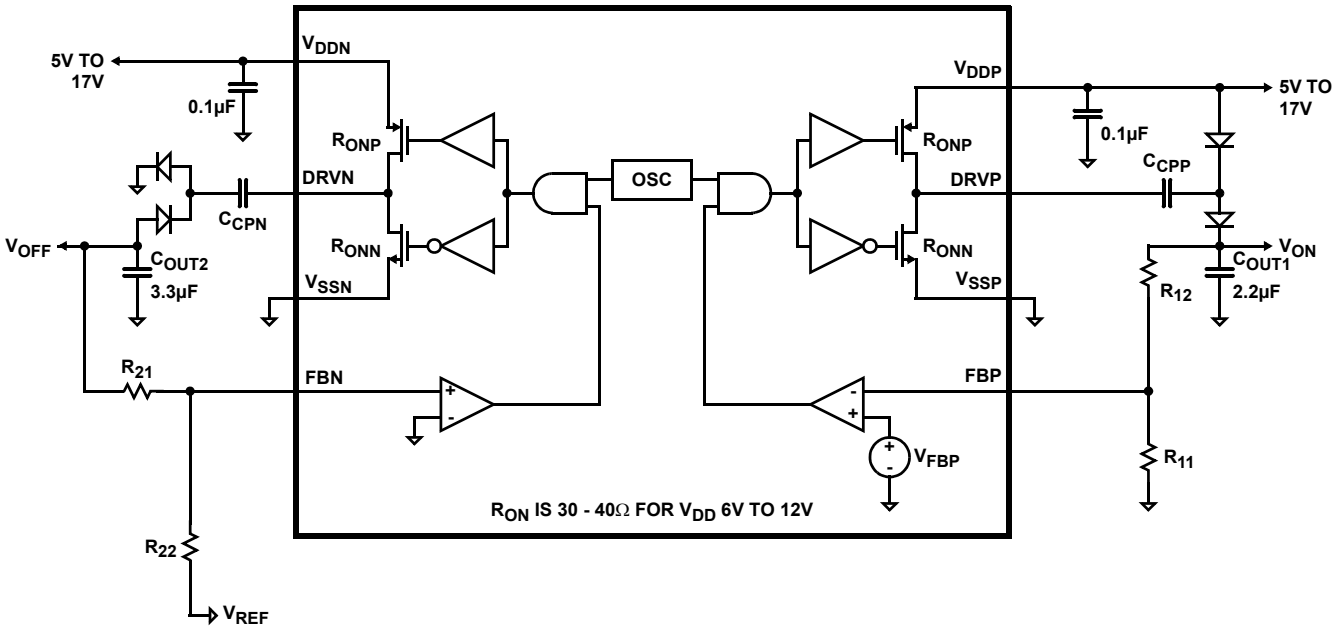
$$I_{CORMS} = \sqrt{(1 - D) \times \left(D + \frac{\Delta I_L^{\,2}}{I_{LAVG}^{\,2}} \times \frac{1}{12} \right)} \times I_{LAVG}$$

Positive and Negative Charge Pump (V_{ON} and V_{OFF})

The EL7584 contains two independent charge pumps (see charge pump block and connection diagram.) The negative charge pump inverts the V_{DDN} supply voltage and provides a regulated negative output voltage. The positive charge pump doubles the V_{DDP} supply voltage and provides a regulated positive output voltage. The regulation of both the negative and positive charge pumps is generated by the internal comparator that senses the output voltage and compares it with and internal reference. The switching frequency of the charge pump is set to ½ the boost converter switching frequency.

The pumps use pulse width modulation to adjust the pump period, depending on the load present. The pumps are short-circuit protected to 180mA at 12V supply and can provide 15mA to 60mA for 6V to 12V supply.

Single Stage Charge Pump



Positive Charge Pump Design Considerations

A single stage charge pump is shown above. The maximum V_{ON} output voltage is determined by the following equation:

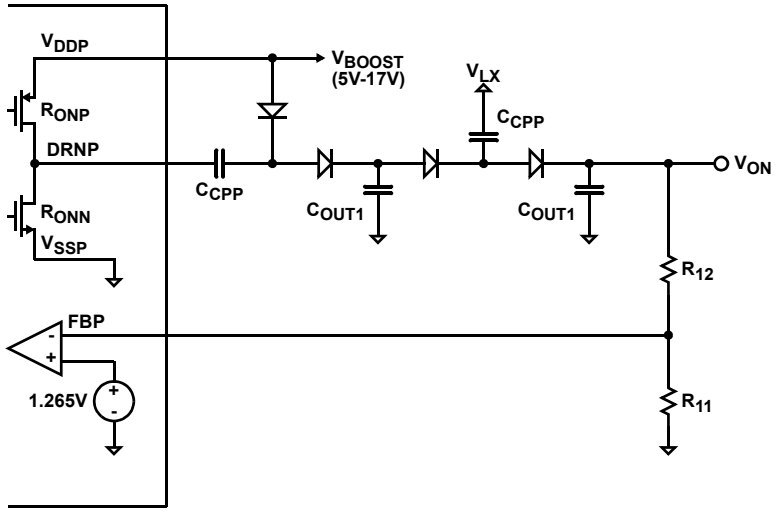
$$V_{ON}(max) \leq 2 \times V_{DDCPP} - I_{OUT} \times 2 \times (R_{ONN} + R_{ONP}) - 2 \times V_{DIODE} - I_{OUT} \times \frac{1}{0.5 \times F_S \times C_{CPP}} - I_{OUT} \times \frac{1}{0.5 \times F_S \times C_{OUT1}}$$

where:

- R_{ONN} and R_{ONP} resistance values depend on the V_{DDP} voltage levels. For 12V supply, R_{ON} is typically 33Ω. For 6V supply, R_{ON} is typically 45Ω.

If additional stage is required, the LX switching signal is recommended to drive the additional charge pump diodes. The drive impedance at the LX switching is typically 150mΩ. The figure below illustrates an implementation for two-stage positive charge pump circuit.

Two-Stage Positive Charge Pump Circuit



The maximum V_{ON} output voltage for N+1 stage charge pump is:

$$V_{ON}(max) \leq 2 \times V_{DDP} - I_{OUT} \times 2 \times (R_{ONN} + R_{ONP}) - 2 \times V_{DIODE} - I_{OUT} \times \frac{1}{0.5 \times F_S \times C_{CPP}} - I_{OUT} \times \frac{1}{0.5 \times F_S \times C_{OUT1}} + N \times V_{LX}(max) - N \times \left(2 \times V_{DIODE} + I_{OUT} \times \frac{1}{0.5 \times F_S \times C_{CPP}} + I_{OUT} \times \frac{1}{0.5 \times F_S \times C_{OUT1}}\right)$$

R_{11} and R_{12} set the V_{ON} output voltage:

$$V_{ON} = V_{FBP} \times \frac{R_{11} + R_{12}}{R_{11}}$$

where V_{FBP} is 1.310V.

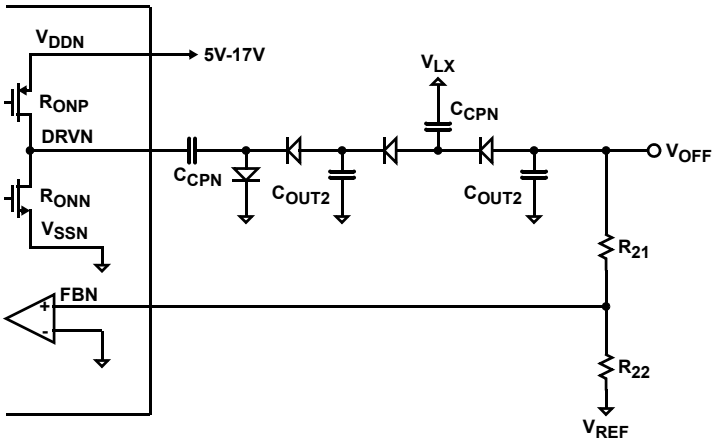
Negative Charge Pump Design Considerations

The criteria for the negative charge pump is similar to the positive charge pump. For a single stage charge pump, the maximum V_{OFF} output voltage is:

$$V_{OFF}(max) \geq I_{OUT} \times 2 \times (R_{ONN} + R_{ONP}) + 2 \times V_{DIODE} - I_{OUT} \times \frac{1}{0.5 \times F_S \times C_{CPN}} - I_{OUT} \times \frac{1}{0.5 \times F_S \times C_{OUT2}} - V_{DDN}$$

Similar to positive charge pump, if additional stage is required, the LX switching signal is recommended to drive the additional charge pump diodes. The figure on the next page shows a two stage negative charge pump circuit.

Two-Stage Negative Charge Pump Circuit



The maximum V_{OFF} output voltage for N+1 stage charge pump is:

$$V_{OFF}(max) \geq I_{OUT} \times 2 \times (R_{ONN} + R_{ONP}) + 2 \times V_{DIODE} - I_{OUT} \times \frac{1}{0.5 \times F_S \times C_{CPN}} - I_{OUT} \times \frac{1}{0.5 \times F_S \times C_{OUT2}} - V_{DDN} - N \times V_{LX}(max) + N \times \left(2 \times V_{DIODE} + I_{OUT} \times \frac{1}{0.5 \times F_S \times C_{CPN}} + I_{OUT} \times \frac{1}{0.5 \times F_S \times C_{OUT2}}\right)$$

R_{21} and R_{22} determine V_{OFF} output voltage:

$$V_{OFF} = -V_{REF} \times \frac{R_{21}}{R_{22}}$$

where V_{REF} is 1.310V.

The V_{COM} Buffer

The V_{COM} buffer is designed to control the voltage on the back plane of an LCD display. This plane is capacitively coupled to the pixel drive voltage which alternately cycles positive and negative at the line rate for the display. Thus the amplifier must be capable of sourcing and sinking capacitive pulses of current, which can occasionally be quite large (a few 100mA for typical applications).

The use of the V_{COM} Buffer is illustrated in Figure 21. Here, a voltage, corresponding to the mid-DAC potential, is generated by a resistive divider and buffered by the amplifier. The amplifier's stability is designed to be dominated by the load capacitance, thus for very short duration pulses (< 1µs) the output capacitor supplies the current. For longer pulses the V_{COM} buffer supplies the current. By virtue of its high transconductance which progressively increases as more current is drawn, it can maintain regulation within 5mV as currents up to 50mA are drawn, while consuming only 1.5mA of quiescent current.

If V_{BOOST} exceeds 15V, V_{DDC} must be protected from over-voltage by including a zener diode between V_{BOOST} and V_{DDC}.

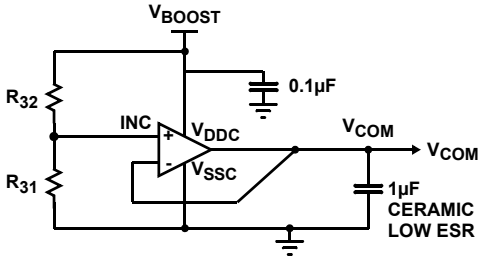


FIGURE 21. V_{COM} USED AS A VOLTAGE BUFFER

As with any high performance buffer, there are several design issues that must be considered when using the part. These are summarized below.

Good Decoupling of Power Supplies

This is essential for this component and 1µF ceramic low ESR decoupling capacitors are recommended. These should be placed close to the pins.

Choice of Output Capacitor

A 1µF ceramic capacitor with low ESR (X5R or X7R type) is recommended for this amplifier. This capacitor determines the stability of the amplifier. Reducing it will make the amplifier less stable, and should be avoided. With a 1µF capacitor, the unity gain bandwidth of the amplifier is close to

500kHz when reasonable currents are being drawn. (For lower load currents, the gain and hence bandwidth progressively decreases.) This means the active transconductance is:

$$2\pi \times 1\mu F \times 500kHz = 3.14S$$

This high transconductance indicates why it is important to have a low ESR capacitor.

If:

- ESR * 3.14 > 1

then the capacitor will not force the gain to roll off below unity, and subsequent poles can affect stability. The recommended capacitor has an ESR of 10mΩ, but to this must be added the resistance of the board trace between the capacitor and the V_{COM} pin, where the sense connection is made internally - therefore this should be kept short. Also ground resistance between the capacitor and the base of R_2 must be kept to a minimum. These constraints should be considered when laying out the PCB.

If the capacitor is increased above 1µF, stability is generally improved and short pulses of current will cause a smaller "perturbation" on the V_{COM} voltage. The speed of response of the amplifier is however degraded as its bandwidth is decreased. At capacitor values around 10µF, a subtle interaction with internal DC gain boost circuitry will decrease the phase margin and may give rise to some overshoot in the response. The amplifier will remain stable, though.

Response to High Current Spikes

The V_{COM} amplifier's output current is limited to 180mA. This limit level, which is roughly the same for sourcing and sinking, is included to maintain reliable operation of the part. It does not necessarily prevent a large temperature rise if the current is maintained. (In this case the whole chip may be shut down by the thermal trip to protect functionality.) If the display occasionally demands current pulses higher than this limit, the reservoir capacitor will provide the excess and the amplifier will top the reservoir capacitor back up once the pulse has stopped. This will happen on the µs time scale in practical systems and for pulses 2 or 3 times the current limit, the V_{COM} voltage will have settled again before the next line is processed.

Power-Up Sequencing

With the components shown in the application diagram the on-chip power-up sequencing operates as follows.

When the EN pin is taken to logic 1, the following sequence is followed by on-chip functions:

1. The boost circuit and negative charge pumps are enabled. V_{BOOST} rises at a rate set by the boost load capacitor, the external load, and the boost's current limit (controlled by the SS pin input.) Similarly, V_{OFF} falls in voltage determined by the load capacitor, the V_{OFF} load, and the current capability of these negative charge pumps (which is rising as V_{BOOST} and hence V_{DDN} rises.)
2. When V_{BOOST} reaches a voltage such that V(FBB)> 1.13V and V_{OFF} first reaches its required regulation voltage, the V_{COM} regulator is enabled and V_{COM} rises at a rate determined by the V_{COM} load capacitor, the load on V_{COM}, and the current limit of the V_{COM} amplifier.
3. When V_{COM} rises to within 100mV of V(INC), an internal delay circuit triggers and, for V_{DDP} = 12V, a default delay of approximately 3.5ms is introduced before the positive charge pump is then enabled. This delay can be increased externally by connecting a capacitor between DP and V_{SSP}. A 1nF capacitor will typically increase the delay before V_{ON} becomes enabled to 80ms.

The enabled states of the on-chip functions become independent of V_{BOOST}, V_{OFF}, V_{COM}, and V_{ON} once each is triggered. The chip may be reset by forcing EN to logic 0 and allowing sufficient time for the various supplies to discharge sufficiently before taking EN to 1 again.

Over-Temperature Protection

An internal temperature sensor continuously monitors the die temperature. In the event that die temperature exceeds the thermal trip point, the device will shut down and disable itself. The upper and lower trip points are typically set to 130°C and 90°C respectively.

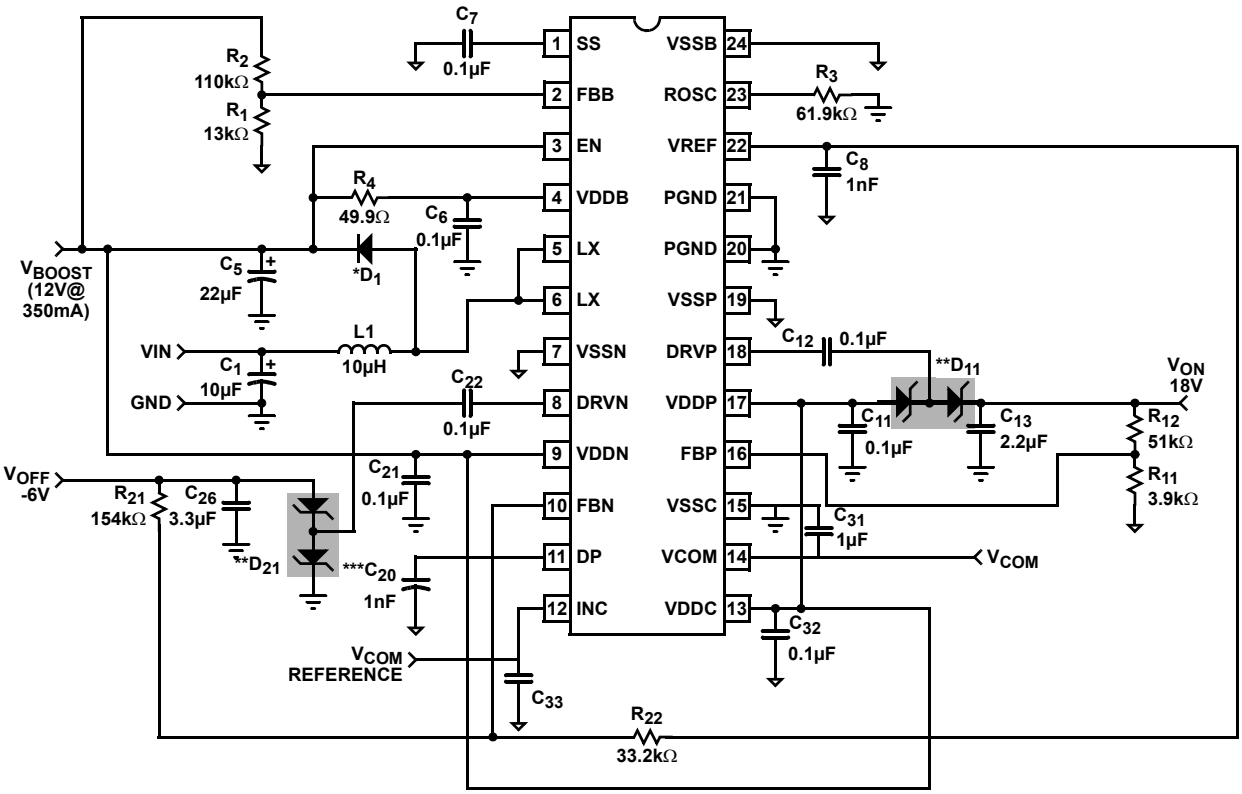
PCB Layout Guidelines

Careful layout is critical in the successful operation of the application. The following layout guidelines are recommended to achieve optimum performance.

1. V_{REF} and V_{DDB} bypass capacitors should be placed next to the pins.
2. Place the boost converter diode and inductor close to the LX pins.
3. Place the boost converter output capacitor close to the PGND pins.
4. Locate feedback dividers close to their respected feedback pins to avoid switching noise coupling into the high impedance node.
5. Place the charge pump feedback resistor network after the diode and output capacitor node to avoid switching noise.
6. All low-side feedback resistors should be connected directly to V_{SSB}. V_{SSB} should be connected to the power ground at one point only.

A demo board is available to illustrate the proper layout implementation.

Typical Application Circuit

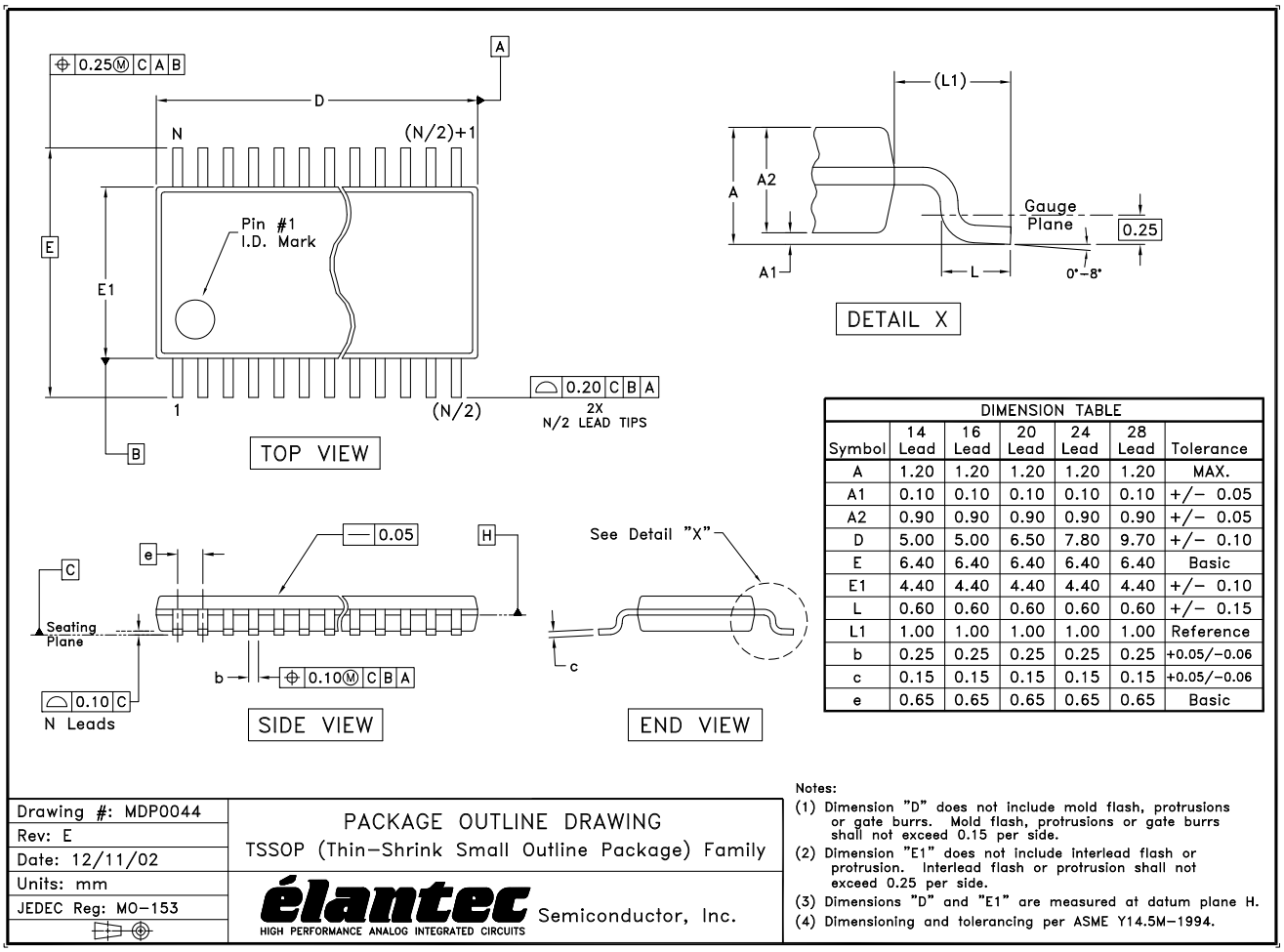


* MBRM120LT3

** BAT54S

*** C_{20} is optional if extended V_{ON} delay is required

Package Outline Drawing



DIMENSION TABLE						
Symbol	14 Lead	16 Lead	20 Lead	24 Lead	28 Lead	Tolerance
A	1.20	1.20	1.20	1.20	1.20	MAX.
A1	0.10	0.10	0.10	0.10	0.10	+/– 0.05
A2	0.90	0.90	0.90	0.90	0.90	+/– 0.05
D	5.00	5.00	6.50	7.80	9.70	+/– 0.10
E	6.40	6.40	6.40	6.40	6.40	Basic
E1	4.40	4.40	4.40	4.40	4.40	+/– 0.10
L	0.60	0.60	0.60	0.60	0.60	+/– 0.15
L1	1.00	1.00	1.00	1.00	1.00	Reference
b	0.25	0.25	0.25	0.25	0.25	+0.05/–0.06
c	0.15	0.15	0.15	0.15	0.15	+0.05/–0.06
e	0.65	0.65	0.65	0.65	0.65	Basic

Drawing #: MDP0044	PACKAGE OUTLINE DRAWING
Rev: E	TSSOP (Thin–Shrink Small Outline Package) Family
Date: 12/11/02	élantec Semiconductor, Inc.
Units: mm	HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS
JEDEC Reg: MO–153	

Notes:
(1) Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 per side.
(2) Dimension "E1" does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25 per side.
(3) Dimensions "D" and "E1" are measured at datum plane H.
(4) Dimensioning and tolerancing per ASME Y14.5M–1994.

NOTE: The package drawing shown here may not be the latest version. To check the latest revision, please refer to the Intersil website at <http://www.intersil.com/design/packages/index.asp>