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Please note: As part of the Fairchild Semiconductor integration, some of the Fairchild orderable part numbers will need to change in order to meet ON Semiconductor's system requirements. Since the ON Semiconductor product management systems do not have the ability to manage part nomenclature that utilizes an underscore (_), the underscore (_) in the Fairchild part numbers will be changed to a dash (-). This document may contain device numbers with an underscore (_). Please check the ON Semiconductor website to verify the updated device numbers. The most current and up-to-date ordering information can be found at www.onsemi.com. Please email any questions regarding the system integration to Fairchild_questions@onsemi.com.

April 2016

FDS8449_F085

N-Channel PowerTrench® MOSFET
40V, 7.6A, 29mΩ

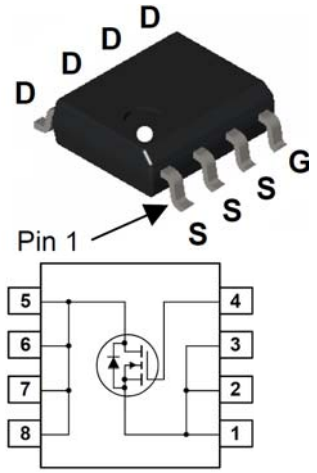
Features

- Typ $R_{DS(on)}$ = 21mΩ at V_{GS} = 10V, I_D = 7.6A
- Typ $R_{DS(on)}$ = 26mΩ at V_{GS} = 4.5V, I_D = 6.8A
- Typ $Q_{g(5)}$ = 7.7nC at V_{GS} = 5V, I_D = 7.6A
- RoHS Compliant
- Qualified to AEC Q101

Applications

- Inverter
- Power Supplies

SO-8



MOSFET Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DSS}	Drain to Source Voltage	40	V
V_{GS}	Gate to Source Voltage	±20	V
I_D	Drain Current Continuous (V_{GS} = 10V)	7.6	A
	Pulsed	50	
E_{AS}	Single Pulse Avalanche Energy (Note 1)	27	mJ
P_D	Power Dissipation	5	W
	Derate above 25°C	0.04	W/°C
T_J, T_{STG}	Operating and Storage Temperature	-55 to +150	°C
$R_{\theta JC}$	Thermal Resistance Junction to Case	25	°C/W
$R_{\theta JA}$	Thermal Resistance Junction to Ambient, 1in^2 copper pad area	50	°C/W

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDS8449	FDS8449_F085	SO-8	13”	12mm	2500 units

Notes:
1: Starting T_J = 25°C, L = 1mH, I_{AS} = 7.3A, V_{DD} = 40V.
2: A suffix as “…F085P” has been temporarily introduced in order to manage a double source strategy as Fairchild has officially announced in Aug 2014.

Electrical Characteristics T_A = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
B_{VDSS}	Drain to Source Breakdown Voltage	I_D = 250μA, V_{GS} = 0V	40	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 32V, V_{GS} = 0V	-	-	1	μA
		V_{DS} = 32V, V_{GS} = 0V, T_A = 150°C	-	-	250	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±20V	-	-	±100	nA
On Characteristics						
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250μA	1	1.9	3	V
$r_{DS(on)}$	Drain to Source On Resistance	I_D = 7.6A, V_{GS}= 10V	-	21	29	mΩ
		I_D = 6.8A, V_{GS}= 4.5V	-	26	36	mΩ
		I_D = 7.6A, V_{GS}= 10V, T_J = 125°C	-	29	43	mΩ
g_{FS}	Forward Transconductance	V_{DS}= 10V, I_D = 7.6A	-	21	-	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 20V, V_{GS} = 0V, f = 1MHz	-	760	-	pF
C_{oss}	Output Capacitance		-	100	-	pF
C_{rss}	Reverse Transfer Capacitance		-	60	-	pF
R_G	Gate Resistance	f = 1MHz	-	1.2	-	Ω
$Q_{g(TOT)}$	Total Gate Charge at 10V	V_{GS} = 0 to 5V, V_{DD} = 20V, I_D = 7.6A	-	7.7	11	nC
Q_{gs}	Gate to Source Gate Charge		-	2.4	-	nC
Q_{gd}	Gate to Drain “Miller“ Charge		-	2.8	-	nC

Switching Characteristics

t_{on}	Turn-On Time	V_{DD} = 20V, I_D = 1A, V_{GS} = 10V, R_{GEN} = 6Ω	-	-	21	ns
$t_{d(on)}$	Turn-On Delay Time		-	9	-	ns
t_r	Rise Time		-	5	-	ns
$t_{d(off)}$	Turn-Off Delay Time		-	23	-	ns
t_f	Fall Time		-	3	-	ns
t_{off}	Turn-Off Time		-	-	39	ns
Drain-Source Diode Characteristics						
V_{SD}	Source to Drain Diode Voltage	I_{SD} = 2.1A	-	0.76	1.2	V
t_{rr}	Reverse Recovery Time	I_{SD} = 7.6A, dI_{SD}/dt = 100A/μs	-	17	-	ns
Q_{rr}	Reverse Recovery Charge		-	7	-	nC

Typical Characteristics

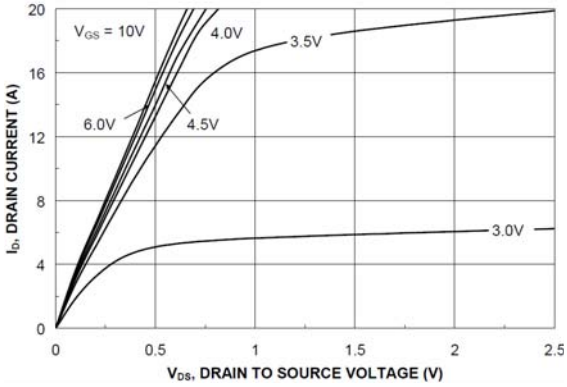


Figure 1. On-Region Characteristics

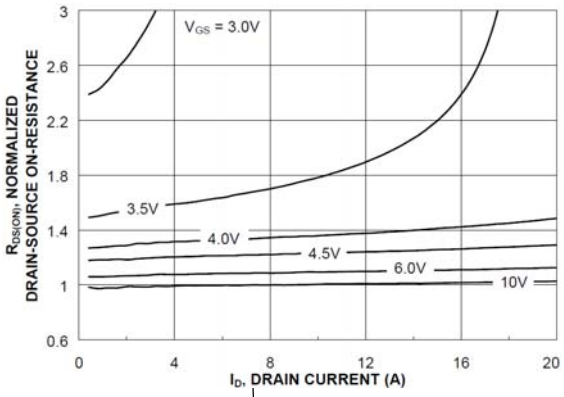


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage

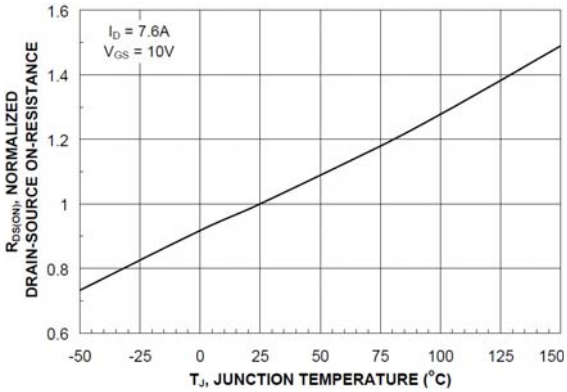


Figure 3. On-Resistance Variation with Temperature

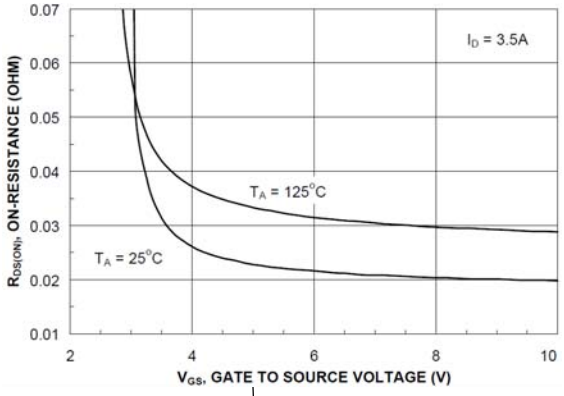


Figure 4. On-Resistance Variation with Gate-to-Source Voltage

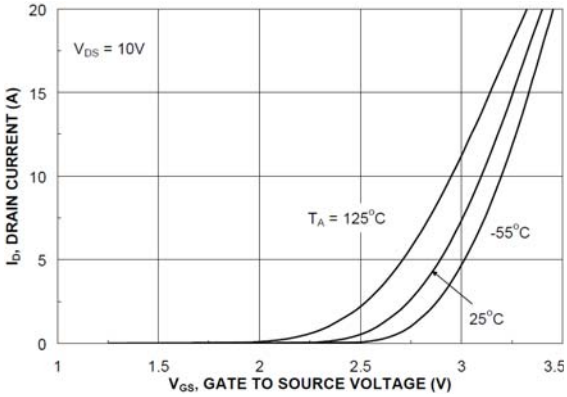


Figure 5. Transfer Characteristics

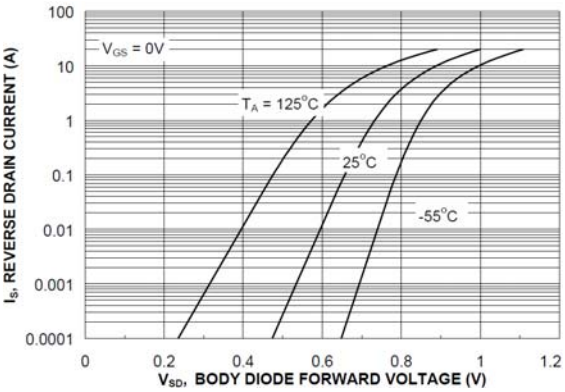


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature

Typical Characteristics

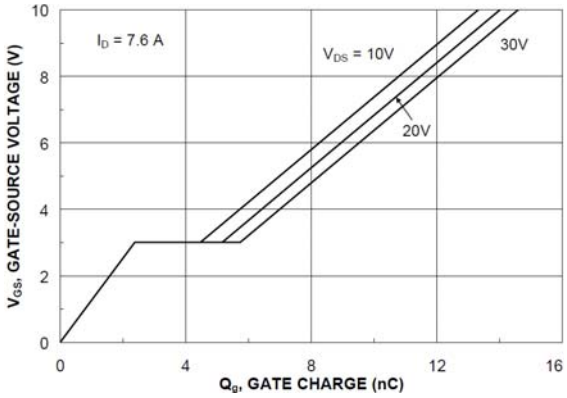


Figure 7. Gate Charge Characteristics

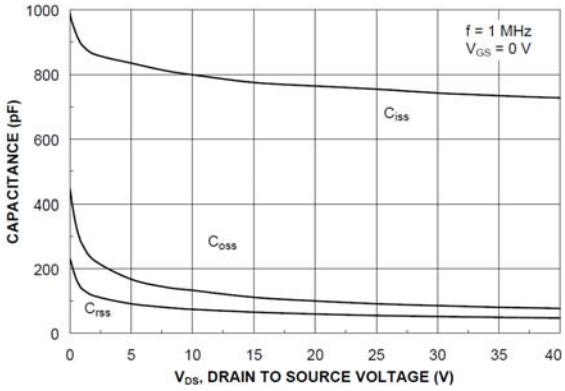


Figure 8. Capacitance Characteristics

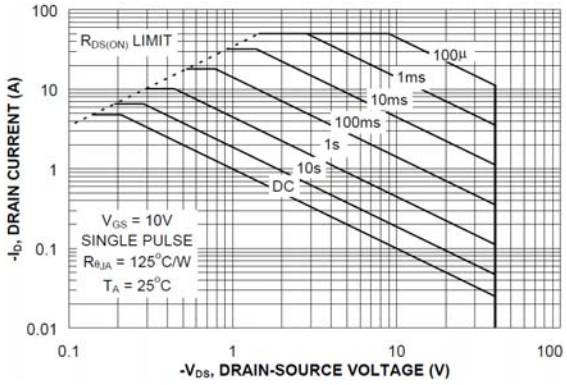


Figure 9. Maximum Safe Operating Area

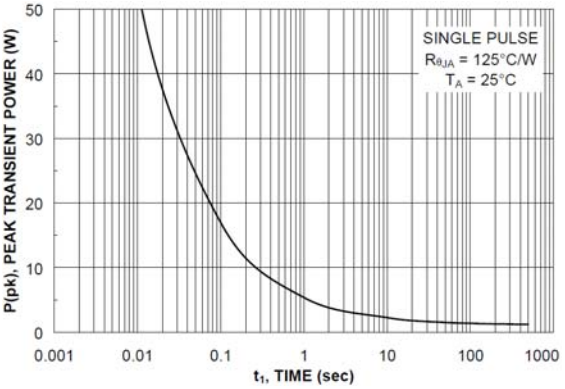


Figure 10. Single Pulse Maximum Power Dissipation

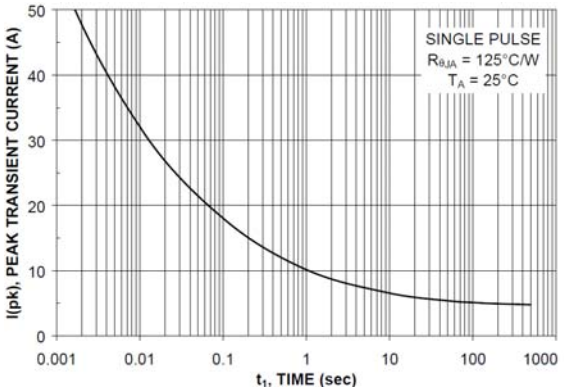


Figure 11. Single Pulse Maximum Peak Current

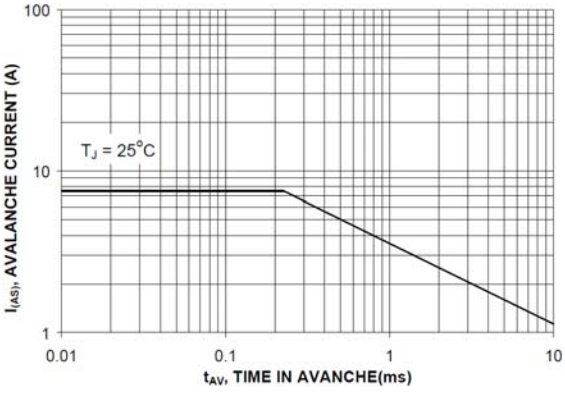


Figure 12. Unclamped Inductive Switching Capability

Typical Characteristics

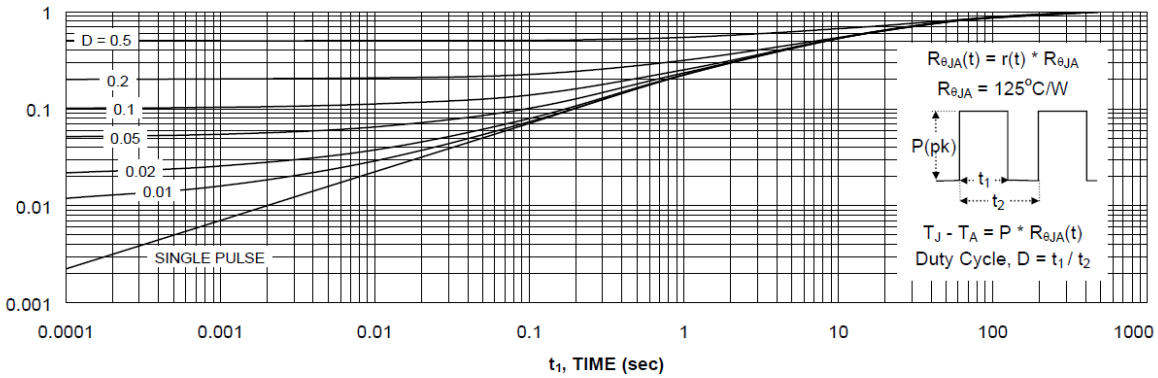
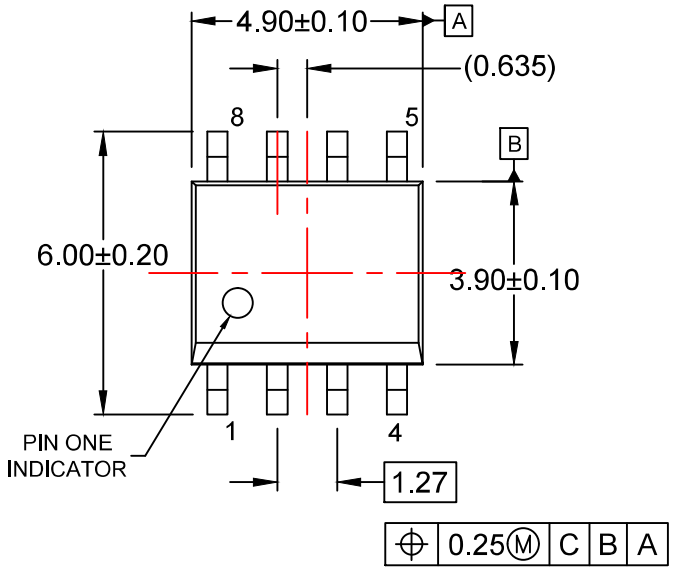
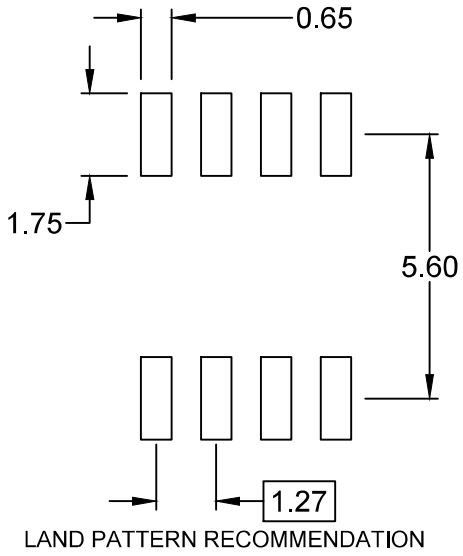
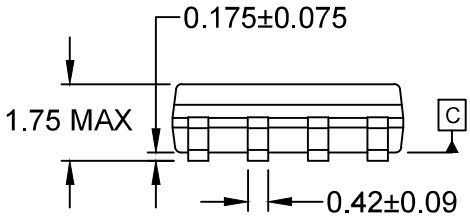


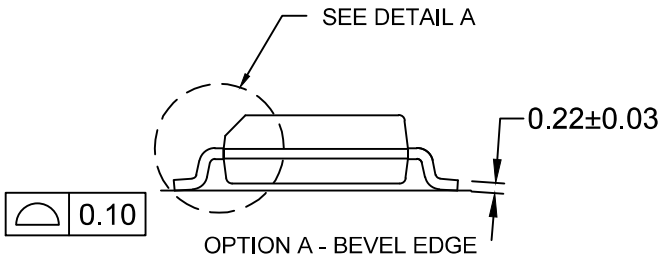
Figure 13. Transient Thermal Response Curve



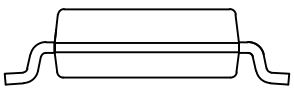


LAND PATTERN RECOMMENDATION

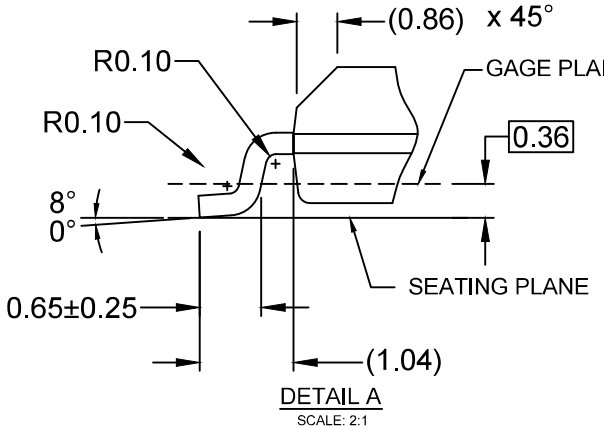




OPTION A - BEVEL EDGE



OPTION B - NO BEVEL EDGE



DETAIL A
SCALE: 2:1

NOTES:

A) THIS PACKAGE CONFORMS TO JEDEC MS-012, VARIATION AA.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.
D) LANDPATTERN STANDARD: SOIC127P600X175-8M
E) DRAWING FILENAME: M08Arev16

FAIRCHILD.

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