

# N-Channel 25-V (D-S) MOSFET

PRODUCT SUMMARY					
V <sub>DS</sub> (V)	$R_{DS(on)}\left(\Omega\right)$	I <sub>D</sub> (A) <sup>a</sup>	Q <sub>g</sub> (Typ.)		
25	0.004 at V <sub>GS</sub> = 10 V	28.6	29 nC		
	0.0052 at V <sub>GS</sub> = 4.5 V	25.6	29110		

# SO-8 S 1 8 D S 2 7 D S 3 6 D Top View

Ordering Information: Si4654DY-T1-E3 (Lead (Pb)-free)

Si4654DY-T1-GE3 (Lead (Pb)-free and Halogen-free)

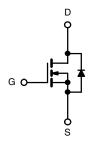
# **FEATURES**

- Halogen-free According to IEC 61249-2-21 Available
- TrenchFET® Power MOSFET
- 100 % R<sub>q</sub> Tested
- 100 % UIS Tested

# ROHS COMPLIANT HALOGEN FREE Available

# **APPLICATIONS**

- Synchronous Buck-Low Side
   Notebook, Game Console
- Synchronous Rectifier-POL



N-Channel MOSFET

Parameter	Symbol	Limit	Unit		
Drain-Source Voltage	V <sub>DS</sub> V <sub>GS</sub>	25	V		
Gate-Source Voltage		± 16	v		
	T <sub>C</sub> = 25 °C		28.6		
Continuous Drain Current (T <sub>.1</sub> = 150 °C)	T <sub>C</sub> = 70 °C	1 . [	23		
Communication Current (1) = 100 O)	T <sub>A</sub> = 25 °C	I <sub>D</sub>	18.6 <sup>b, c</sup>		
	T <sub>A</sub> = 70 °C	1 -	14.9 <sup>b, c</sup>	Α	
Pulsed Drain Current		I <sub>DM</sub>	70	A	
Continuous Source-Drain Diode Current	T <sub>C</sub> = 25 °C		5.1		
Continuous Source-Drain Diode Current	T <sub>A</sub> = 25 °C	I <sub>S</sub>	2.2 <sup>b, c</sup>		
Single Pulse Avalanche Current	L = 0.1 mH	I <sub>AS</sub>	30		
Avalanche Energy		E <sub>AS</sub>	45	mJ	
	T <sub>C</sub> = 25 °C		5.9		
Maximum Dawar Dissination	T <sub>C</sub> = 70 °C		3.8	w	
Maximum Power Dissipation	T <sub>A</sub> = 25 °C	$P_{D}$	2.5 <sup>b, c</sup>	VV	
	T <sub>A</sub> = 70 °C	1	1.6 <sup>b, c</sup>		
Operating Junction and Storage Temperature	T <sub>J</sub> , T <sub>stg</sub>	- 55 to 150	°C		

THERMAL RESISTANCE RATINGS							
Parameter	Symbol	Typical	Maximum	Unit			
Maximum Junction-to-Ambient <sup>b, d</sup>	t ≤ 10 s	$R_{thJA}$	37	50	°C/W		
Maximum Junction-to-Foot (Drain)	Steady State	$R_{thJF}$	17	21	O/ <b>VV</b>		

## Notes:

- a. Based on  $T_C = 25$  °C.
- b. Surface Mounted on 1" x 1" FR4 board.
- c. t = 10 s.
- d. Maximum under Steady State conditions is 85 °C/W.

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Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit	
Static			<u>I</u>		1		
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	25			V	
V <sub>DS</sub> Temperature Coefficient	$\Delta V_{DS}/T_{J}$	J 050 A		26		mV/°C	
V <sub>GS(th)</sub> Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	I <sub>D</sub> = 250 μA		- 5.6			
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}$ , $I_{D} = 250 \mu\text{A}$	1.0		2.5	V	
Gate-Source Leakage	I <sub>GSS</sub>	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 16 \text{ V}$			± 100	nA	
7 0 1 1/1 5 1 0 1	I <sub>DSS</sub>	V <sub>DS</sub> = 25 V, V <sub>GS</sub> = 0 V			1		
Zero Gate Voltage Drain Current		$V_{DS} = 25 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 55 ^{\circ}\text{C}$			10	μΑ	
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	$V_{DS} \ge 5 \text{ V}, V_{GS} = 10 \text{ V}$	30			Α	
		V <sub>GS</sub> = 10 V, I <sub>D</sub> = 15 A		0.0032	0.004		
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DS(on)</sub>	$V_{GS} = 4.5 \text{ V}, I_D = 10 \text{ A}$		0.004	0.0052	Ω	
Forward Transconductance <sup>a</sup>	9 <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 15 A		100		S	
Dynamic <sup>b</sup>			L	L			
Input Capacitance	C <sub>iss</sub>			3770		pF	
Output Capacitance	C <sub>oss</sub>	$V_{DS} = 15 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$		560			
Reverse Transfer Capacitance	C <sub>rss</sub>			255			
Total Cata Chausa	$V_{DC} = 15 \text{ V}, V_{CC} = 10 \text{ V}, I_{D} = 10 \text{ A}$		63	100			
Total Gate Charge	$Q_{g}$	Q <sub>g</sub>		29	45	20	
Gate-Source Charge	$Q_{gs}$	$V_{DS} = 15 \text{ V}, V_{GS} = 4.5 \text{ V}, I_{D} = 10 \text{ A}$		8.5		nC	
Gate-Drain Charge	Q <sub>gd</sub>			7.2			
Gate Resistance	$R_g$	f = 1 MHz		0.9	1.8	Ω	
Turn-On Delay Time	t <sub>d(on)</sub>			30	50		
Rise Time	t <sub>r</sub>	$V_{DD}$ = 15 V, $R_L$ = 3 $\Omega$		10	20	ns	
Turn-Off Delay Time	t <sub>d(off)</sub>	$I_D\cong 5$ A, $V_{GEN}=4.5$ V, $R_g=1$ $\Omega$		50	90		
Fall Time	t <sub>f</sub>			10	20		
Turn-On Delay Time	t <sub>d(on)</sub>			12	24		
Rise Time	t <sub>r</sub>	$V_{DD}$ = 15 V, $R_L$ = 3 $\Omega$		8	16		
Turn-Off Delay Time	t <sub>d(off)</sub>	$I_D\cong$ 5 A, $V_{GEN}$ = 10 V, $R_g$ = 1 $\Omega$		38	70		
Fall Time	t <sub>f</sub>			8	16		
<b>Drain-Source Body Diode Characterist</b>	ics						
Continuous Source-Drain Diode Current	I <sub>S</sub>	T <sub>C</sub> = 25 °C			5.1	А	
Pulse Diode Forward Current <sup>a</sup>	I <sub>SM</sub>				70		
Body Diode Voltage	$V_{SD}$	I <sub>S</sub> = 3 A		0.73	1.1	V	
Body Diode Reverse Recovery Time	t <sub>rr</sub>			32	60	ns	
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>	I <sub>F</sub> = 5 A, dl/dt = 100 A/μs, T <sub>.l</sub> = 25 °C		26	55	nC	
Reverse Recovery Fall Time	t <sub>a</sub>	$_{1F} = 5 \text{ A}$ , $_{100} = 100 \text{ A/} \mu \text{s}$ , $_{13} = 25 \text{ C}$		16			
Reverse Recovery Rise Time	t <sub>b</sub>			16		ns	

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

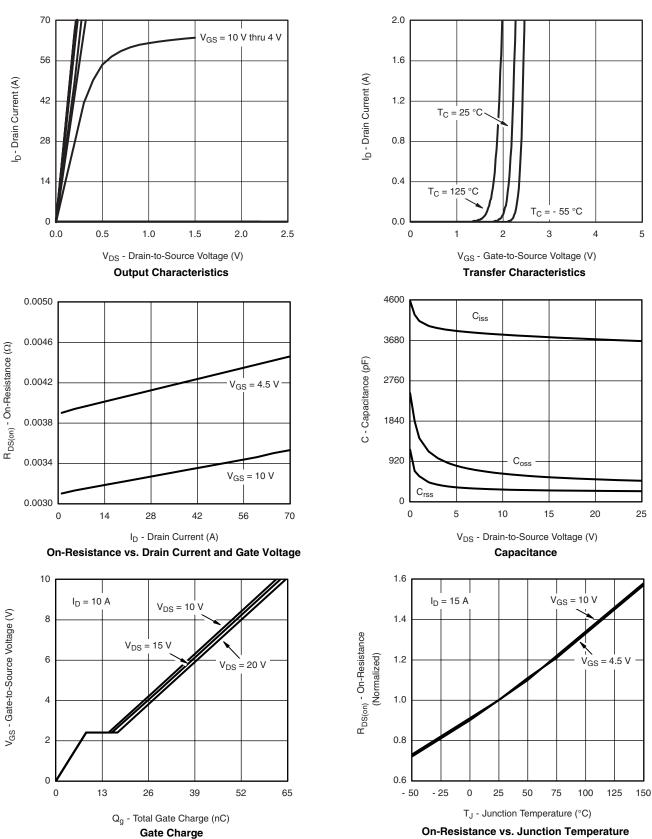
a. Pulse test; pulse width  $\leq$  300  $\mu s,$  duty cycle  $\leq$  2 %

b. Guaranteed by design, not subject to production testing.



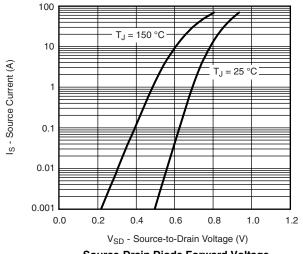


# TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

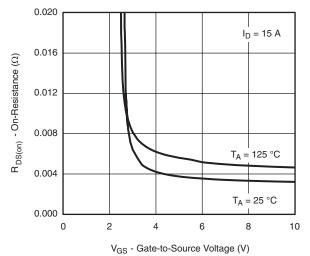


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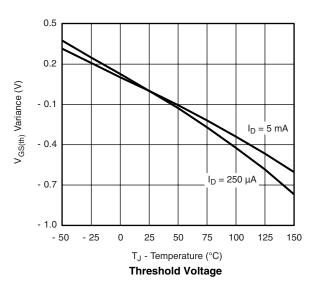
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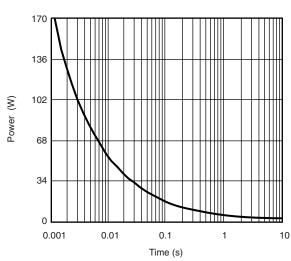


Source-Drain Diode Forward Voltage

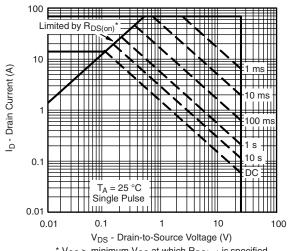


On-Resistance vs. Gate-to-Source Voltage





Single Pulse Power, Junction-to-Ambient

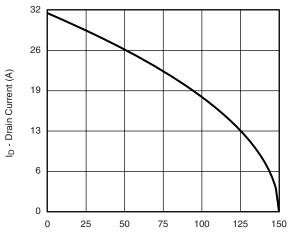


\*  $V_{GS}$  > minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified

Safe Operating Area, Junction-to-Ambient

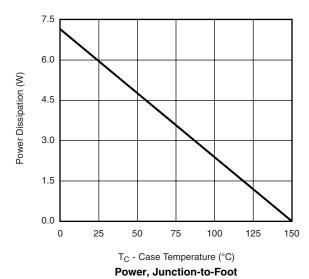


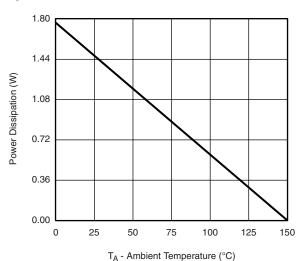
# TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



T<sub>C</sub> - Case Temperature (°C)

# Current Derating\*





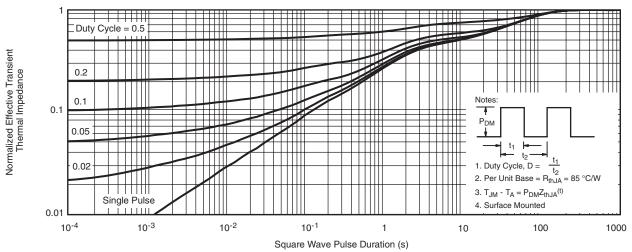
Power, Junction-to-Ambient

<sup>\*</sup> The power dissipation  $P_D$  is based on  $T_{J(max)} = 150$  °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

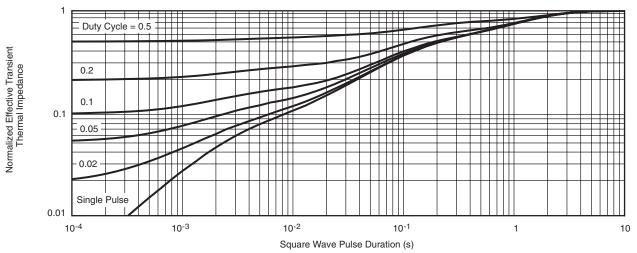
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# TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Foot

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SOIC (NARROW): 8-LEAD JEDEC Part Number: MS-012







	MILLIM	IETERS	INCHES			
DIM	Min	Max	Min	Max		
Α	1.35	1.75	0.053	0.069		
A <sub>1</sub>	0.10	0.20	0.004	0.008		
В	0.35	0.51	0.014	0.020		
С	0.19	0.25	0.0075	0.010		
D	4.80	5.00	0.189	0.196		
Е	3.80	4.00	0.150	0.157		
е	1.27	BSC	0.050	0.050 BSC		
Н	5.80	6.20	0.228	0.244		
h	0.25	0.50	0.010	0.020		
L	0.50	0.93	0.020	0.037		
q	0°	8°	0°	8°		
S	0.44	0.64	0.018	0.026		
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DWG: 5498

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# **RECOMMENDED MINIMUM PADS FOR SO-8**



Recommended Minimum Pads Dimensions in Inches/(mm)

Return to Index

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