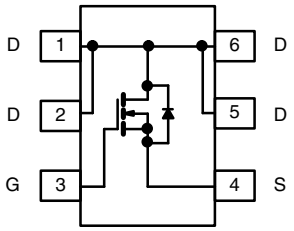
Si1442DH

Vishay Siliconix

N-Channel 12 V (D-S) MOSFET

PRODUCT SUMMARY			
V_{DS} (V)	$R_{DS(on)}$ (Ω) (Max.)	I_D (A)[a]	Q_g (Typ.)
12	0.020 at V_{GS} = 4.5 V	4	13.1 nC
	0.024 at V_{GS} = 2.5 V	4	
	0.030 at V_{GS} = 1.8 V	4	

SOT-363
SC-70 (6-LEADS)



Top View

Ordering Information:
Si1442DH-T1-GE3 (Lead (Pb)-free and Halogen-free)

FEATURES

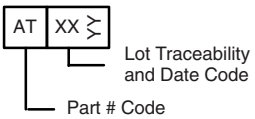
- TrenchFET® Power MOSFET
- 100 % R_g Tested
- Material categorization:
  For definitions of compliance please see www.vishay.com/doc?99912

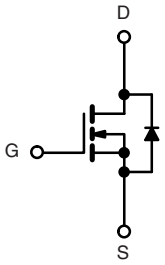
Pb-free
RoHS COMPLIANT
HALOGEN FREE

APPLICATIONS

- Load Switch and Battery Switch for Portable Devices
- DC/DC Converters
- Low On-Resistance for Low Voltage Drop

Marking Code





N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)				
Parameter		**Symbol**	**Limit**	**Unit**
Drain-Source Voltage		V_{DS}	12	V
Gate-Source Voltage		V_{GS}	± 8	
Continuous Drain Current (T_J = 150 °C)	T_F = 25 °C	I_D	4[a]	A
	T_F = 70 °C		4[a]	
	T_A = 25 °C		4[a, b, c]	
	T_A = 70 °C		4[a, b, c]	
Pulsed Drain Current (t = 300 µs)		I_{DM}	20	
Continuous Source-Drain Diode Current	T_F = 25 °C	I_S	2.3	
	T_A = 25 °C		1.3[b, c]	
Maximum Power Dissipation	T_F = 25 °C	P_D	2.8	W
	T_F = 70 °C		1.8	
	T_A = 25 °C		1.56[b, c]	
	T_A = 70 °C		1[b, c]	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	- 55 to 150	°C
Soldering Recommendations (Peak Temperature)			260	

THERMAL RESISTANCE RATINGS					
Parameter		**Symbol**	**Typical**	**Maximum**	**Unit**
Maximum Junction-to-Ambient[b, d]	t ≤ 5 s	R_{thJA}	60	80	°C/W
Maximum Junction-to-Foot (Drain)	Steady State	R_{thJF}	34	45	

Notes:
a. T_F = 25 °C, package limited.
b. Surface mounted on 1" x 1" FR4 board.
c. t = 5 s.
d. Maximum under steady state conditions is 125 °C/W.

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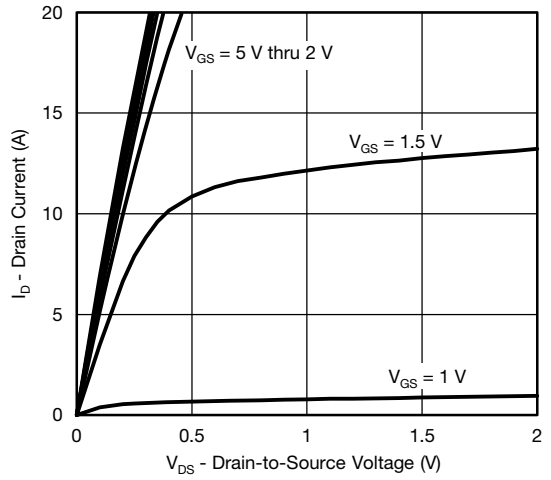
SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)						
Parameter	**Symbol**	**Test Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
Static						
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = 250 µA	12			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	I_D = 250 µA		5		mV/°C
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			- 2.7		
Gate-Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	0.4		1	V
Gate-Source Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 8 V			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 12 V, V_{GS} = 0 V			1	µA
		V_{DS} = 12 V, V_{GS} = 0 V, T_J = 55 °C			10	
On-State Drain Current[a]	$I_{D(on)}$	$V_{DS} \geq$ 5 V, V_{GS} = 4.5 V	15			A
Drain-Source On-State Resistance[a]	$R_{DS(on)}$	V_{GS} = 4.5 V, I_D = 6 A		0.017	0.020	Ω
		V_{GS} = 2.5 V, I_D = 5 A		0.019	0.024	
		V_{GS} = 1.8 V, I_D = 3 A		0.023	0.030	
Forward Transconductance[a]	g_{fs}	V_{DS} = 6 V, I_D = 6 A		33		S
Dynamic[b]						
Input Capacitance	C_{iss}	V_{DS} = 6 V, V_{GS} = 0 V, f = 1 MHz		1010		pF
Output Capacitance	C_{oss}			323		
Reverse Transfer Capacitance	C_{rss}			305		
Total Gate Charge	Q_g	V_{DS} = 6 V, V_{GS} = 8 V, I_D = 7 A		21.8	33	nC
		V_{DS} = 6 V, V_{GS} = 4.5 V, I_D = 7 A		13.1	20	
Gate-Source Charge	Q_{gs}			2		
Gate-Drain Charge	Q_{gd}			2.7		
Gate Resistance	R_g	f = 1 MHz	0.3	1.6	3.2	Ω
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 6 V, R_L = 1.07 Ω $I_D \cong$ 5.6 A, V_{GEN} = 4.5 V, R_g = 1 Ω		8	16	ns
Rise Time	t_r			13	20	
Turn-Off Delay Time	$t_{d(off)}$			22	33	
Fall Time	t_f			9	18	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 6 V, R_L = 1.07 Ω $I_D \cong$ 5.6 A, V_{GEN} = 8 V, R_g = 1 Ω		6	12	
Rise Time	t_r			12	18	
Turn-Off Delay Time	$t_{d(off)}$			22	33	
Fall Time	t_f			8	16	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	T_C = 25 °C			4	A
Pulse Diode Forward Current	I_{SM}				20	
Body Diode Voltage	V_{SD}	I_S = 5.6 A, V_{GS} = 0 V		0.75	1.2	V
Body Diode Reverse Recovery Time	t_{rr}	I_F = 5.6 A, dI/dt = 100 A/µs, T_J = 25 °C		19	30	ns
Body Diode Reverse Recovery Charge	Q_{rr}			7	14	nC
Reverse Recovery Fall Time	t_a			13		ns
Reverse Recovery Rise Time	t_b			6		

Notes:
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.
b. Guaranteed by design, not subject to production testing.

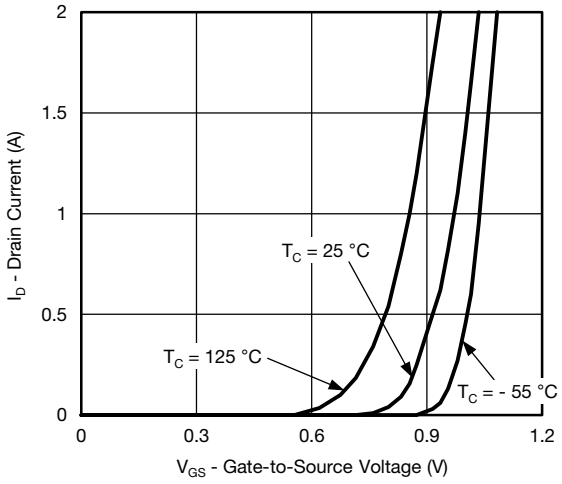
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

For technical support, please contact: pmostechsupport@vishay.com
Document Number: 63772
S12-0546-Rev. A, 12-Mar-12
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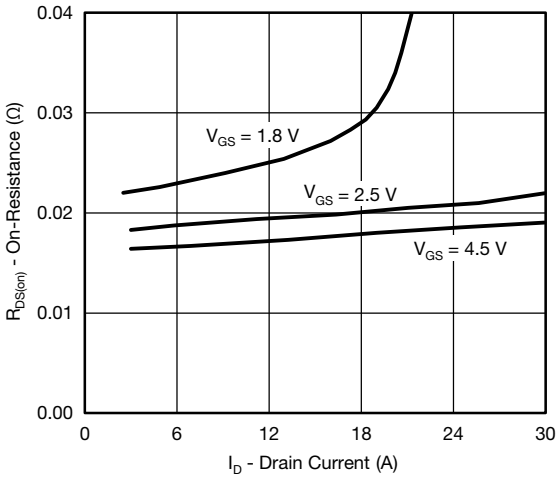
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



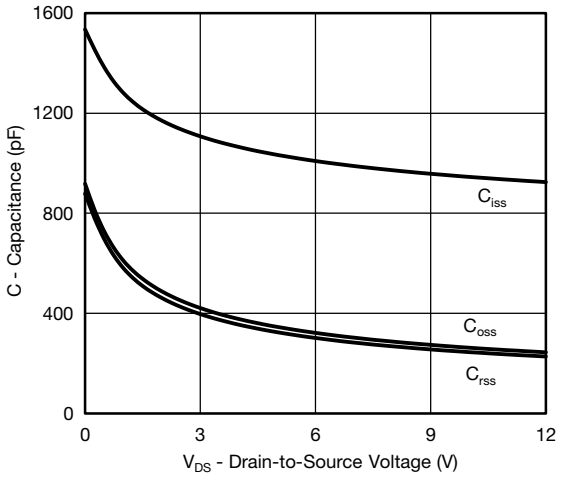
Output Characteristics



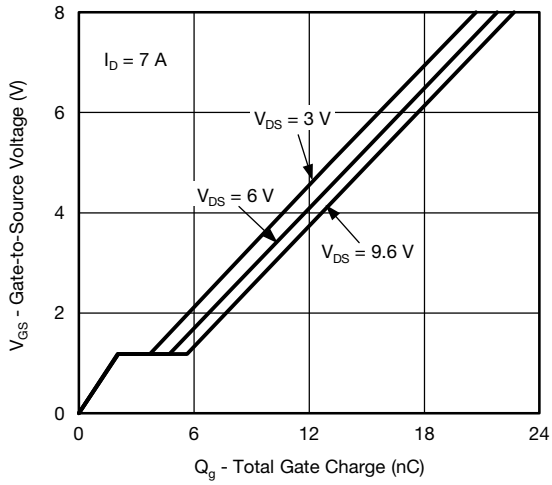
Transfer Characteristics



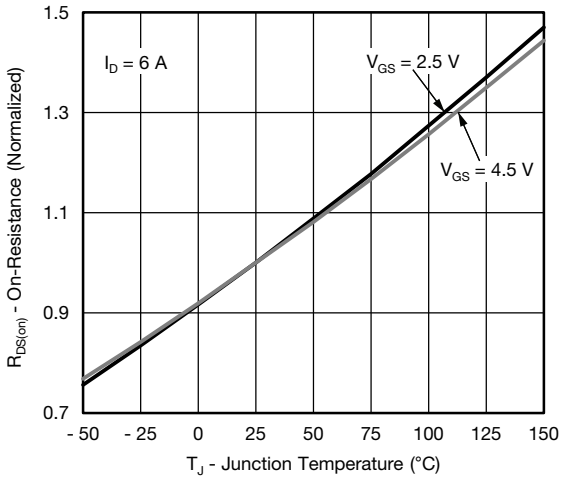
On-Resistance vs. Drain Current



Capacitance



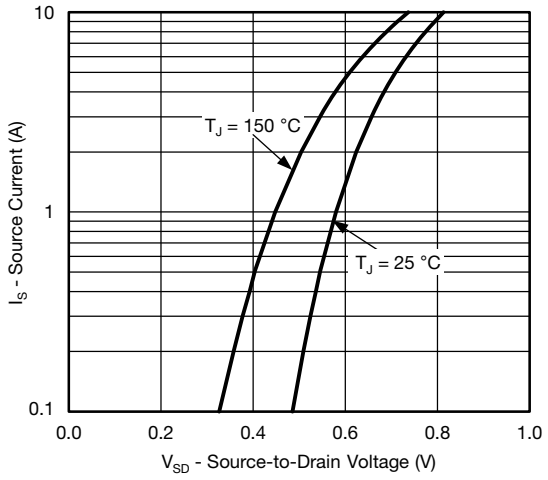
Gate Charge



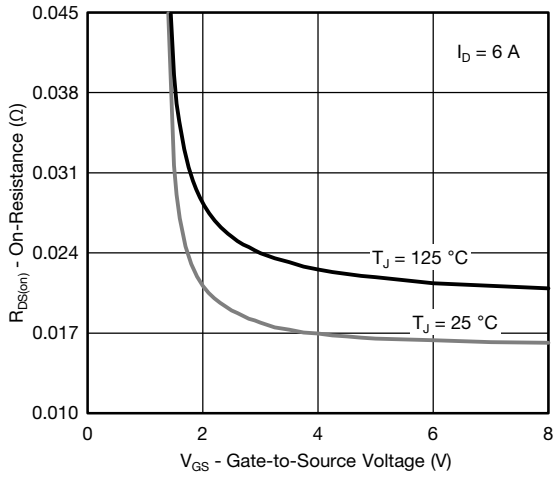
On-Resistance vs. Junction Temperature

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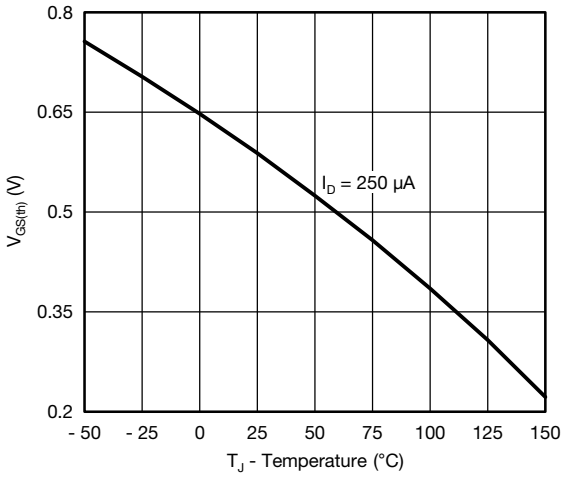
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



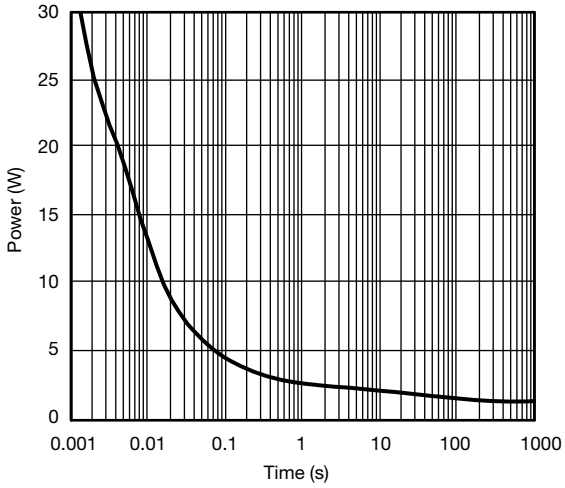
Soure-Drain Diode Forward Voltage



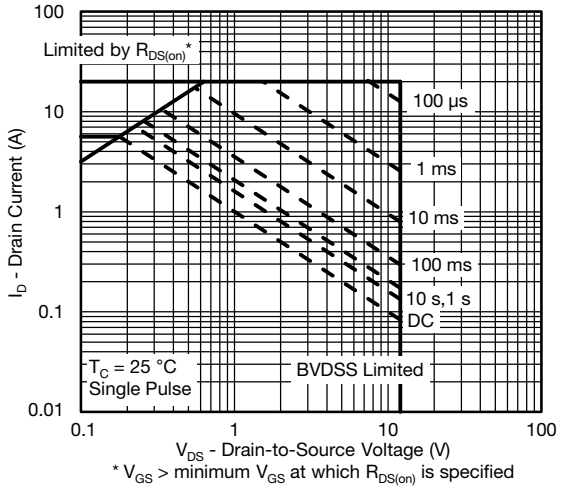
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



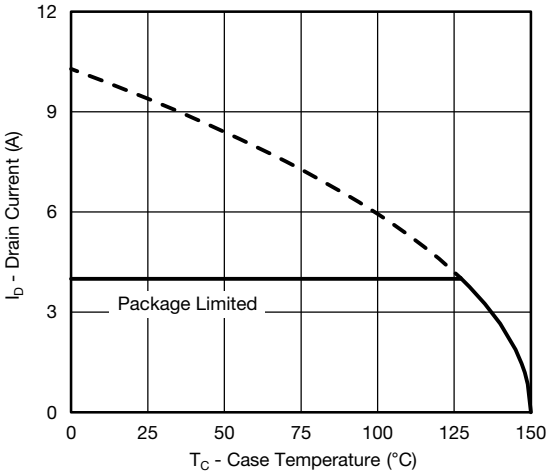
Single Pulse Power, Junction-to-Ambient



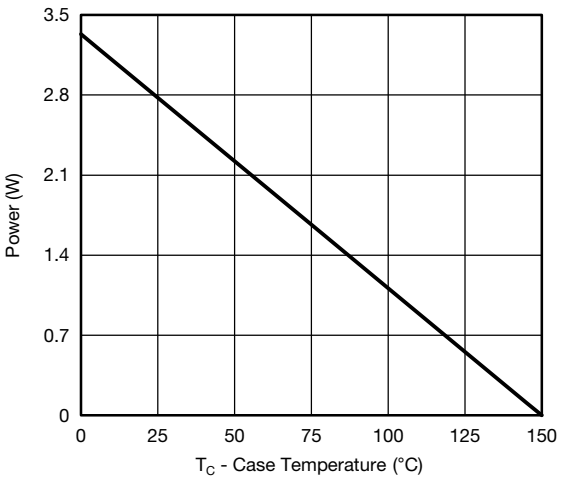
Safe Operating Area, Junction-to-Ambient

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S12-0546-Rev. A, 12-Mar-12
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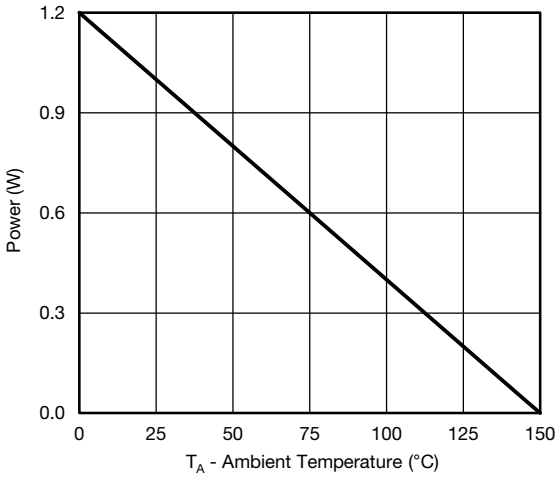
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Current Derating*



Power Junction-to-Case

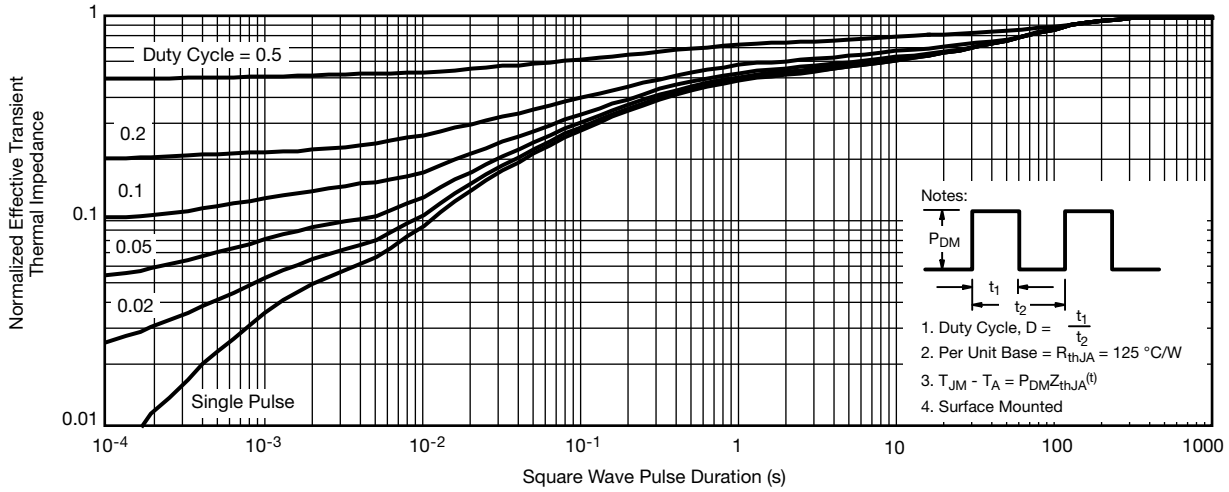


Power Junction-to-Ambient

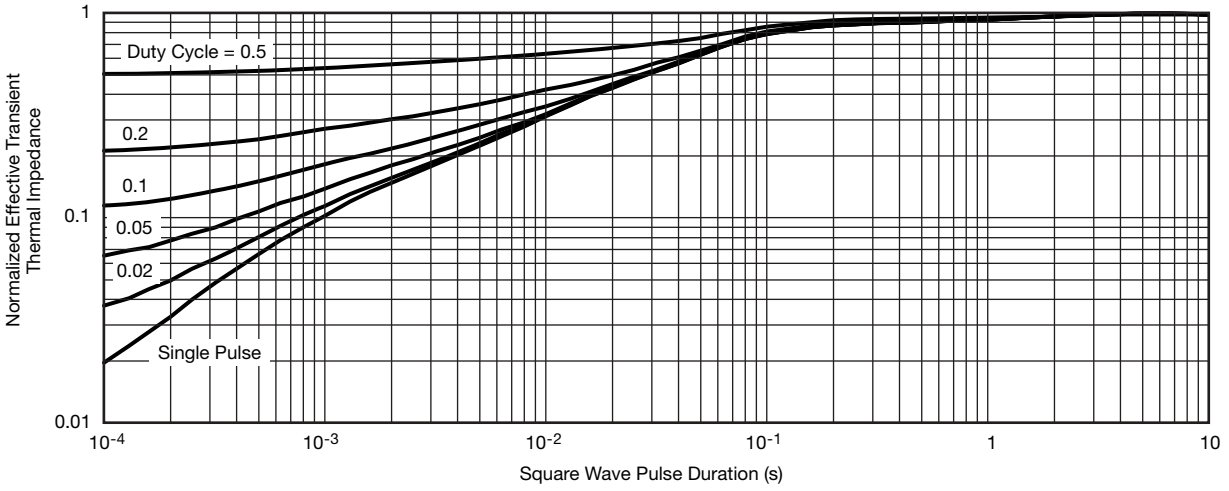
* The power dissipation P_D is based on $T_{J(max.)}$ = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

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TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient

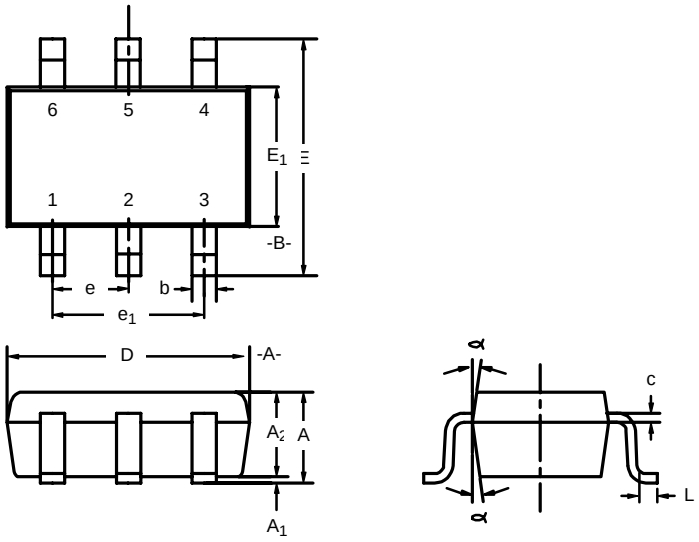


Normalized Thermal Transient Impedance, Junction-to-Foot

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?63772.

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SC-70: 6-LEADS



Dim	MILLIMETERS			INCHES		
	Min	Nom	Max	Min	Nom	Max
A	0.90	–	1.10	0.035	–	0.043
A_1	–	–	0.10	–	–	0.004
A_2	0.80	–	1.00	0.031	–	0.039
b	0.15	–	0.30	0.006	–	0.012
c	0.10	–	0.25	0.004	–	0.010
D	1.80	2.00	2.20	0.071	0.079	0.087
E	1.80	2.10	2.40	0.071	0.083	0.094
E_1	1.15	1.25	1.35	0.045	0.049	0.053
e	0.65BSC			0.026BSC		
e_1	1.20	1.30	1.40	0.047	0.051	0.055
L	0.10	0.20	0.30	0.004	0.008	0.012
α	7°Nom			7°Nom		

ECN: S-03946—Rev. B, 09-Jul-01
DWG: 5550

Single-Channel LITTLE FOOT® SC-70 6-Pin MOSFET Copper Leadframe Version Recommended Pad Pattern and Thermal Performance

INTRODUCTION

The new single 6-pin SC-70 package with a copper leadframe enables improved on-resistance values and enhanced thermal performance as compared to the existing 3-pin and 6-pin packages with Alloy 42 leadframes. These devices are intended for small to medium load applications where a miniaturized package is required. Devices in this package come in a range of on-resistance values, in n-channel and p-channel versions. This technical note discusses pin-outs, package outlines, pad patterns, evaluation board layout, and thermal performance for the single-channel version.

BASIC PAD PATTERNS

See Application Note 826, *Recommended Minimum Pad Patterns With Outline Drawing Access for Vishay Siliconix MOSFETs*, (http://www.vishay.com/doc?72286) for the basic pad layout and dimensions. These pad patterns are sufficient for the low to medium power applications for which this package is intended. Increasing the drain pad pattern yields a reduction in thermal resistance and is a preferred footprint. The availability of four drain leads rather than the traditional single drain lead allows a better thermal path from the package to the PCB and external environment.

PIN-OUT

Figure 1 shows the pin-out description and Pin 1 identification.The pin-out of this device allows the use of four pins as drain leads, which helps to reduce on-resistance and junction-to-ambient thermal resistance.

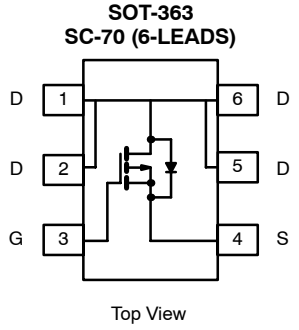


FIGURE 1.

For package dimensions see outline drawing SC-70 (6-Leads) (http://www.vishay.com/doc?71154)

EVALUATION BOARDS — SINGLE SC70-6

The evaluation board (EVB) measures 0.6 inches by 0.5 inches. The copper pad traces are the same as in Figure 2. The board allows examination from the outer pins to 6-pin DIP connections, permitting test sockets to be used in evaluation testing. See Figure 3.

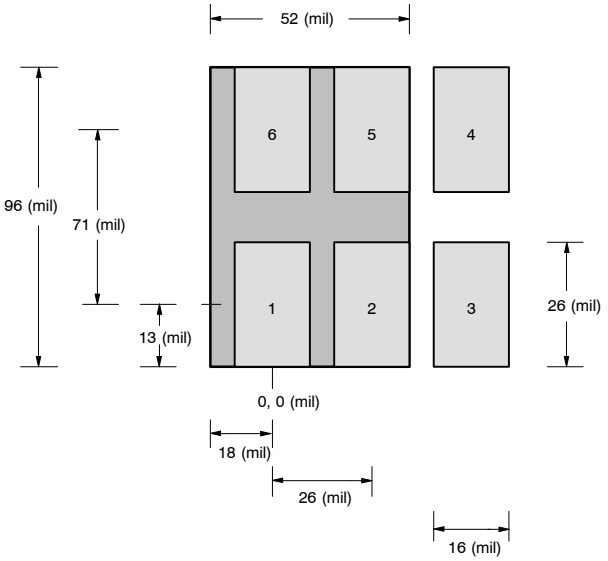


FIGURE 2. SC-70 (6 leads) Single

The thermal performance of the single 6-pin SC-70 has been measured on the EVB, comparing both the copper and Alloy 42 leadframes. This test was first conducted on the traditional Alloy 42 leadframe and was then repeated using the 1-inch^2 PCB with dual-side copper coating.

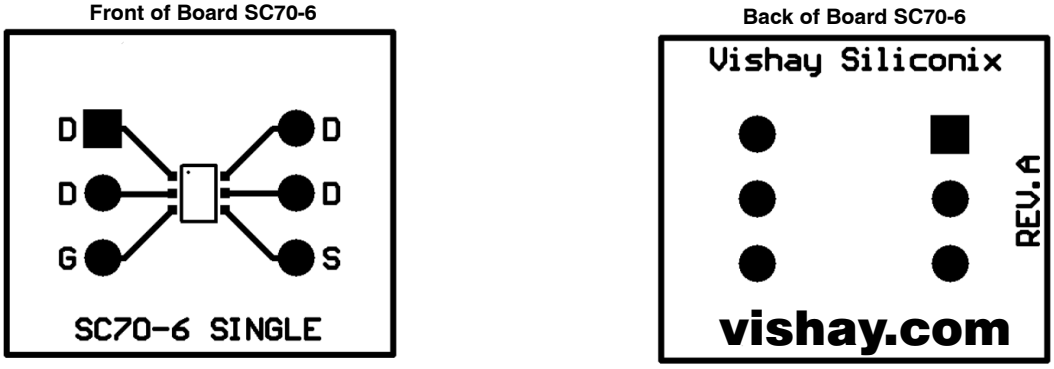


FIGURE 3.

THERMAL PERFORMANCE

Junction-to-Foot Thermal Resistance (Package Performance)

The junction to foot thermal resistance is a useful method of comparing different packages thermal performance.

A helpful way of presenting the thermal performance of the 6-Pin SC-70 copper leadframe device is to compare it to the traditional Alloy 42 version.

Thermal performance for the 6-pin SC-70 measured as junction-to-foot thermal resistance, where the “foot” is the drain lead of the device at the bottom where it meets the PCB. The junction-to-foot thermal resistance is typically 40°C/W in the copper leadframe and 163°C/W in the Alloy 42 leadframe — a four-fold improvement. This improved performance is obtained by the enhanced thermal conductivity of copper over Alloy 42.

Power Dissipation

The typical $R\theta_{JA}$ for the single 6-pin SC-70 with copper leadframe is 103°C/W steady-state, compared with 212°C/W for the Alloy 42 version. The figures are based on the 1-inch^2 FR4 test board. The following example shows how the thermal resistance impacts power dissipation for the two different leadframes at varying ambient temperatures.

ALLOY 42 LEADFRAME	
Room Ambient 25 °C	**Elevated Ambient 60 °C**
$P_D = \frac{T_{J(max)} - T_A}{R\theta_{JA}}$ $P_D = \frac{150°C - 25°C}{212°C/W}$ $P_D = 590$ mW	$P_D = \frac{T_{J(max)} - T_A}{R\theta_{JA}}$ $P_D = \frac{150°C - 25°C}{212°C/W}$ $P_D = 425$ mW

COOPER LEADFRAME	
Room Ambient 25 °C	**Elevated Ambient 60 °C**
$P_D = \frac{T_{J(max)} - T_A}{R\theta_{JA}}$ $P_D = \frac{150°C - 25°C}{124°C/W}$ $P_D = 1.01$ W	$P_D = \frac{T_{J(max)} - T_A}{R\theta_{JA}}$ $P_D = \frac{150°C - 60°C}{124°C/W}$ $P_D = 726$ mW

As can be seen from the calculations above, the compact 6-pin SC-70 copper leadframe LITTLE FOOT power MOSFET can handle up to 1 W under the stated conditions.

Testing

To further aid comparison of copper and Alloy 42 leadframes, Figure 5 illustrates single-channel 6-pin SC-70 thermal performance on two different board sizes and two different pad patterns. The measured steady-state values of $R\theta_{JA}$ for the two leadframes are as follows:

LITTLE FOOT 6-PIN SC-70		
	Alloy 42	**Copper**
1) Minimum recommended pad pattern on the EVB board V (see Figure 3.	329.7°C/W	208.5°C/W
2) Industry standard 1-inch^2 PCB with maximum copper both sides.	211.8°C/W	103.5°C/W

The results indicate that designers can reduce thermal resistance ($R\theta_{JA}$) by 36% simply by using the copper leadframe device rather than the Alloy 42 version. In this example, a 121°C/W reduction was achieved without an increase in board area. If increasing in board size is feasible, a further 105°C/W reduction could be obtained by utilizing a 1-inch^2 square PCB area.

The copper leadframe versions have the following suffix:

Single:	Si14xxEDH
Dual:	Si19xxEDH
Complementary:	Si15xxEDH

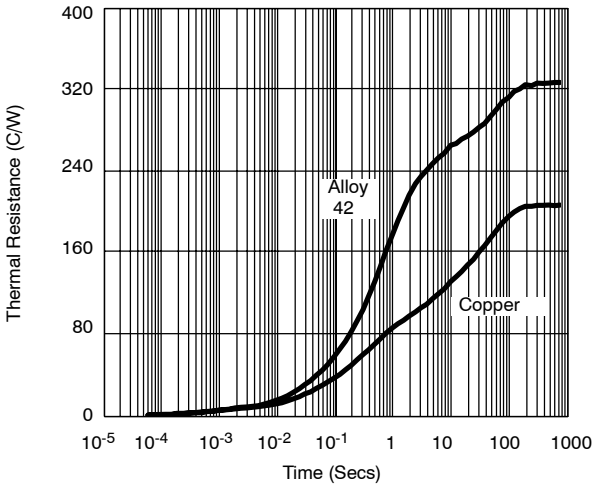


FIGURE 4. Leadframe Comparison on EVB

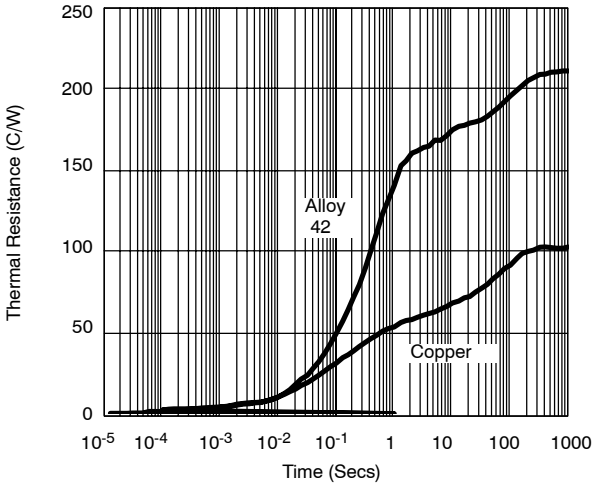
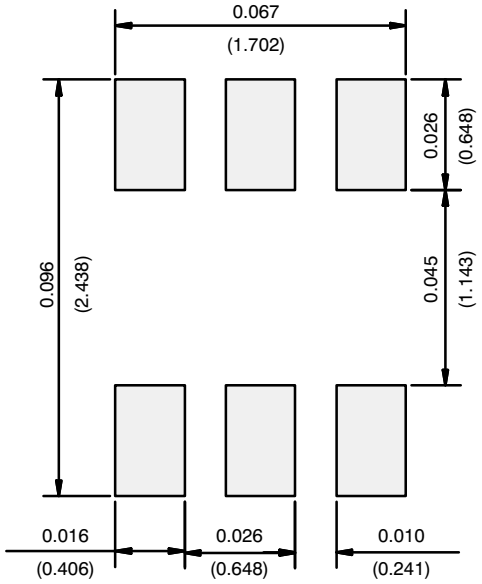


FIGURE 5. Leadframe Comparison on Alloy 42 1-inch^2 PCB

RECOMMENDED MINIMUM PADS FOR SC-70: 6-Lead



Recommended Minimum Pads
Dimensions in Inches/(mm)

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