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February 2010

# FDS9431A\_F085

# P-Channel 2.5V Specified MOSFET

# **General Description**

This P-Channel 2.5V specified MOSFET is produced using Fairchild's proprietary, high cell density, DMOS technology. This very high density process has been especially tailored to minimize on-state resistance and yet maintain superior switching performance.

# **Applications**

- DC/DC converter
- · Power management

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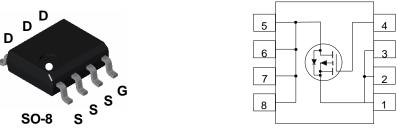
- Load switch
- Battery protection

### **Features**

- -3.5 A, -20 V.  $R_{DS(ON)} = 0.130 \Omega$  @  $V_{GS} = -4.5 V$  $R_{_{DS(ON)}} = 0.180~\Omega~$  @  $V_{_{GS}} =~-2.5~V.$
- · Fast switching speed.
- High density cell design for extremely low R<sub>DS(ON)</sub>.
- · High power and current handling capability.
- Qualified to AEC Q101
- RoHS Compliant







# **Absolute Maximum Ratings**

T<sub>A</sub>=25°C unless otherwise noted

Symbol	Parameter		Ratings	Units
$V_{DSS}$	Drain-Source Voltage		-20	V
$V_{GSS}$	Gate-Source Voltage		±8	V
I <sub>D</sub>	Drain Current - Continuous	(Note 1a)	-3.5	А
	- Pulsed		-18	
P <sub>D</sub>	Power Dissipation for Single Operation	(Note 1a)	2.5	W
		(Note 1b)	1.2	
		(Note 1c)	1.0	
T <sub>J</sub> , T <sub>stg</sub>	Operating and Storage Junction Temperature Range		-55 to +150	°C

# **Thermal Characteristics**

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	50	°C/W
R <sub>θJC</sub>	Thermal Resistance, Junction-to-Case	(Note 1)	25	°C/W

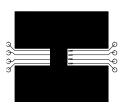
**Package Marking and Ordering Information** 

Device Marking	Device	Reel Size	Tape width	Quantity	
FDS9431A	FDS9431A FDS9431A_F085 13"		12mm	2500 units	

Symbol	Parameter	Test Conditions	Min	Тур	Max	Units
Off Char	acteristics	•		•		
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_D = -250 \mu\text{A}$	-20			V
ΔBV <sub>DSS</sub> ΔT <sub>J</sub>	Breakdown Voltage Temperature Coefficient	$I_D$ = -250 $\mu$ A,Referenced to 25°C		-28		mV/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = -16 V, V <sub>GS</sub> = 0 V			-1	μΑ
I <sub>GSSF</sub>	Gate-Body Leakage Current, Forward	V <sub>GS</sub> = 8 V, V <sub>DS</sub> = 0 V			100	nA
I <sub>GSSR</sub>	Gate-Body Leakage Current, Reverse	$V_{GS} = -8 \text{ V}, V_{DS} = 0 \text{ V}$			-100	nA
On Char	acteristics (Note 2)					
V <sub>GS(th)</sub>	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = -250 \mu A$	-0.4	-0.6	-1	V
$\Delta V_{GS(th)} \over \Delta T_J$	Gate Threshold Voltage Temperature Coefficient	I <sub>D</sub> = -250 μA,Referenced to 25°C		2		mV/°C
R <sub>DS(on)</sub>	Static Drain-Source	V <sub>GS</sub> = -4.5 V, I <sub>D</sub> = -3.5 A		0.110	0.130	Ω
	On-Resistance	$V_{GS} = -2.5 \text{ V}, I_{D} = -3.0 \text{ A}$ $V_{GS} = -4.5 \text{ V}, I_{D} = -3.5 \text{ A}$		0.140 0.155	0.180 0.220	Ω
		V <sub>GS</sub> = -4.5 V, I <sub>D</sub> = -5.5 A T <sub>.J</sub> =125°C		0.155	0.220	Ω
I <sub>D(on)</sub>	On-State Drain Current	V <sub>GS</sub> = -4.5 V, V <sub>DS</sub> =-5 V	-10			Α
<b>g</b> FS	Forward Transconductance	$V_{DS} = -5 \text{ V}, I_{D} = -3.5 \text{ A}$		6.5		S
Dvnamic	Characteristics					
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = -10 V, V <sub>GS</sub> = 0 V,		405		pF
Coss	Output Capacitance	f = 1.0 MHz		170		pF
C <sub>rss</sub>	Reverse Transfer Capacitance	7		45		pF
Switchin	g Characteristics (Note 2)					
t <sub>d(on)</sub>	Turn-On Delay Time	$V_{DD} = -5 \text{ V}, I_{D} = -1 \text{ A},$		6.5	13	ns
t <sub>r</sub>	Turn-On Rise Time	$V_{GS} = -4.5 \text{ V}, R_{GEN} = 6 \Omega$		20	35	ns
t <sub>d(off)</sub>	Turn-Off Delay Time	7		31	50	ns
t <sub>f</sub>	Turn-Off Fall Time	7		21	35	ns
Qg	Total Gate Charge	$V_{DS} = -5 \text{ V}, I_{D} = -3.5 \text{ A},$		6	8.5	nC
Q <sub>gs</sub>	Gate-Source Charge	V <sub>GS</sub> = -4.5 V		0.8		nC
Q <sub>gd</sub>	Gate-Drain Charge	7		1.3		nC
Drain-Sc	ource Diode Characteristics	and Maximum Ratings				
ls	Maximum Continuous Drain-Source				-2.1	А
V <sub>SD</sub>	Drain-Source Diode Forward	$V_{GS} = 0 \text{ V}, I_S = -2.1 \text{ A} \text{ (Note 2)}$		-0.7	-1.2	V

#### Notes

<sup>1:</sup>  $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



a) 50° C/W when mounted on a 1 in² pad of 2 oz. copper.



b) 105° C/W when mounted on a 0.04 in<sup>2</sup> pad of 2 oz. copper.

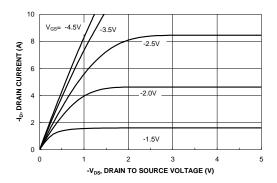


c) 125° C/W on a minimum mounting pad.

Scale 1 : 1 on letter size paper

2: Pulse Test: Pulse Width  $\leq$  300  $\mu$ s, Duty Cycle  $\leq$  2.0%

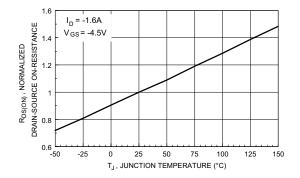
# **Typical Characteristics**



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Figure 1. On-Region Characteristics.

Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.



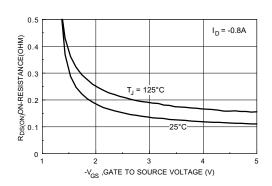
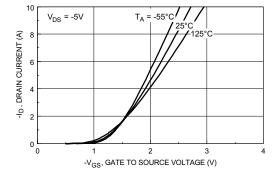


Figure 3. On-Resistance Variation with Temperature.

Figure 4. On-Resistance Variation with Gate-to-Source Voltage.



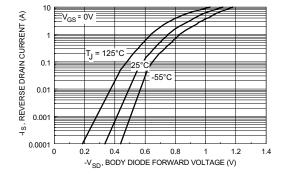


Figure 5. Transfer Characteristics.

Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

# Typical Characteristics (continued)

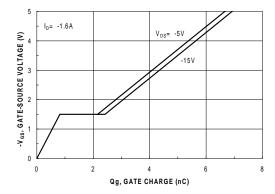
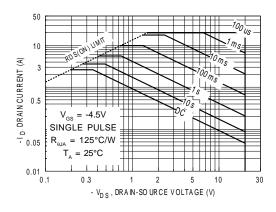


Figure 7. Gate Charge Characteristics.

Figure 8. Capacitance Characteristics.



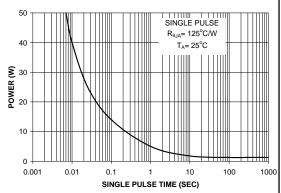


Figure 9. Maximum Safe Operating Area.

Figure 10. Single Pulse Maximum Power Dissipation.

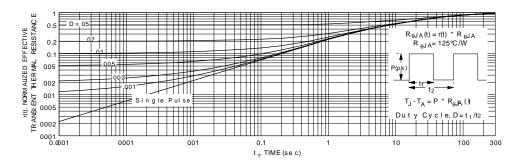


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1c. Transient themal response will change depending on the circuit board design.





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