

**SL38000ZIT Information**


For Reference Only

**Part Number** [SL38000ZIT](#)  
**Manufacturer** Silicon Labs  
**Category** Integrated Circuits (ICs)  
 Clock/Timing - Clock Generators, PLLs,  
 Frequency Synthesizers  
**Description** IC CLK 4PLL VCXO SSCG 28TSSOP  
**Package** 28-TSSOP (0.173", 4.40mm Width)  
 For the pricing/inventory/lead time, please contact  
 us  
 Website: <https://www.heisener.com>  
 E-mail: [salesdept@heisener.com](mailto:salesdept@heisener.com)


[Request a Quote](#)
**Certified Quality**

Heisener's commitment to quality has shaped our processes for sourcing, testing, shipping, and every step in between. This foundation underlies each component we sell.


**SL38000ZIT Specifications**

Manufacturer Part Number	<a href="#">SL38000ZIT</a>
Manufacturer	Silicon Labs
Category	Integrated Circuits (ICs) <a href="#">Clock/Timing - Clock Generators, PLLs, Frequency Synthesizers</a>
Package	28-TSSOP (0.173", 4.40mm Width)
Series	EProClock?
Type	-
PLL	Yes with Bypass
Input	Clock, Crystal
Output	LVC MOS
Number of Circuits	1
Ratio - Input:Output	1:11
Differential - Input:Output	No/No
Frequency - Max	200MHz
Divider/Multiplier	Yes/No
Voltage - Supply	2.97 V ~ 3.63 V
Operating Temperature	-40°C ~ 85°C
Mounting Type	Surface Mount
Package / Case	28-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	28-TSSOP

[Report errors?](#)

## SL38000ZIT Guarantees



### Quality Guarantees

We provide 90 days warranty. \*

If the items you received were not in perfect quality, we would be responsible for your refund or replacement, but the items must be returned in their original condition.



### Service Guarantees

We guarantee 100% customer satisfaction.

Our experienced sales team and tech support team back our services to satisfy all our customers.

## SL38000ZIT Payment Methods



## SL38000ZIT Shipping Methods



If you have any question about SL38000ZIT, please do not hesitate to contact us!

Website: <https://www.heisener.com>

E-mail: [salesdept@heisener.com](mailto:salesdept@heisener.com)